NEC

# MOS FIELD EFFECT TRANSISTOR
# NP36N055HLE, NP36N055ILE

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

These products are N-Channel MOS Field Effect Transistors designed for high current switching applications.

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| NP36N055HLE | TO-251(MP-3) |
| NP36N055ILE | TO-252(MP-3Z) |

### FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
- ★ $R_{DS(on)1}$ = 13 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 18 A)
- ★ $R_{DS(on)2}$ = 16 mΩ MAX. ($V_{GS}$ = 5 V, $I_D$ = 18 A)
- ★ Low $C_{iss}$ : $C_{iss}$ = 2900 pF TYP.
- Built-in gate protection diode

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C)

| | | | | |
|---|---|---|---|---|
| | Drain to Source Voltage | $V_{DSS}$ | 55 | V |
| | Gate to Source Voltage | $V_{GSS}$ | ±20 | V |
| | Drain Current (DC) | $I_{D(DC)}$ | ±36 | A |
| | Drain Current (Pulse) Note1 | $I_{D(pulse)}$ | ±144 | A |
| | Total Power Dissipation ($T_A$ = 25 °C) | $P_T$ | 1.2 | W |
| ★ | Total Power Dissipation ($T_C$ = 25 °C) | $P_T$ | 120 | W |
| ★ | Single Avalanche Current Note2 | $I_{AS}$ | 36 / 33 | A |
| ★ | Single Avalanche Energy Note2 | $E_{AS}$ | 12 / 108 | mJ |
| | Channel Temperature | $T_{ch}$ | 175 | °C |
| | Storage Temperature | $T_{stg}$ | –55 to + 175 | °C |

**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1 %

**2.** Starting $T_{ch}$ = 25 °C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V → 0 V

### THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| ★ | Channel to Case | $R_{th(ch-C)}$ | 1.25 | °C/W |
| | Channel to Ambient | $R_{th(ch-A)}$ | 125 | °C/W |



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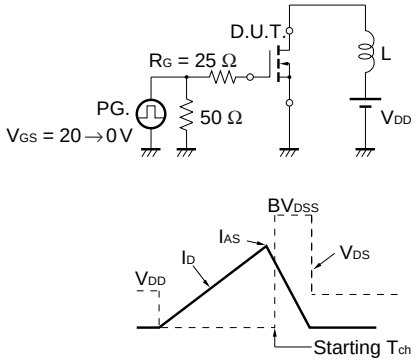
The mark ★ shows major revised points.

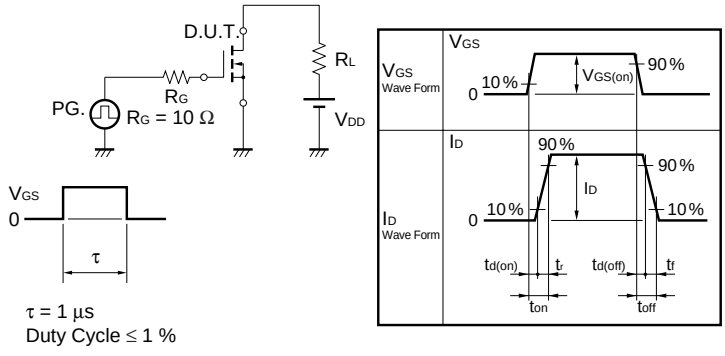
## ★ ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 18 A | | 10 | 13 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 5 V, $I_D$ = 18 A | | 12 | 16 | mΩ |
| | $R_{DS(on)3}$ | $V_{GS}$ = 4.5 V, $I_D$ = 18 A | | 13 | 18 | mΩ |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.5 | 2 | 2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 18 A | 11 | 23 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = 55 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 25 V | | 2900 | 4400 | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 370 | 560 | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 180 | 330 | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $I_D$ = 18 A | | 36 | 80 | ns |
| Rise Time | $t_r$ | $V_{GS(on)}$ = 10 V | | 320 | 800 | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $V_{DD}$ = 28 V | | 130 | 260 | ns |
| Fall Time | $t_f$ | $R_G$ = 10 Ω | | 120 | 300 | ns |
| Total Gate Charge | $Q_{G1}$ | $I_D$ = 18 A | | 53 | 80 | nC |
| | $Q_{G2}$ | $V_{DD}$ = 44 V | | 30 | 45 | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V | | 9 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | | | 15 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 36 A, $V_{GS}$ = 0 V | | 1.0 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 36 A, $V_{GS}$ = 0 V | | 42 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 60 | | nC |

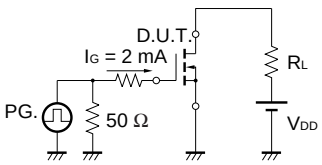
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**




**TEST CIRCUIT 2 SWITCHING TIME**

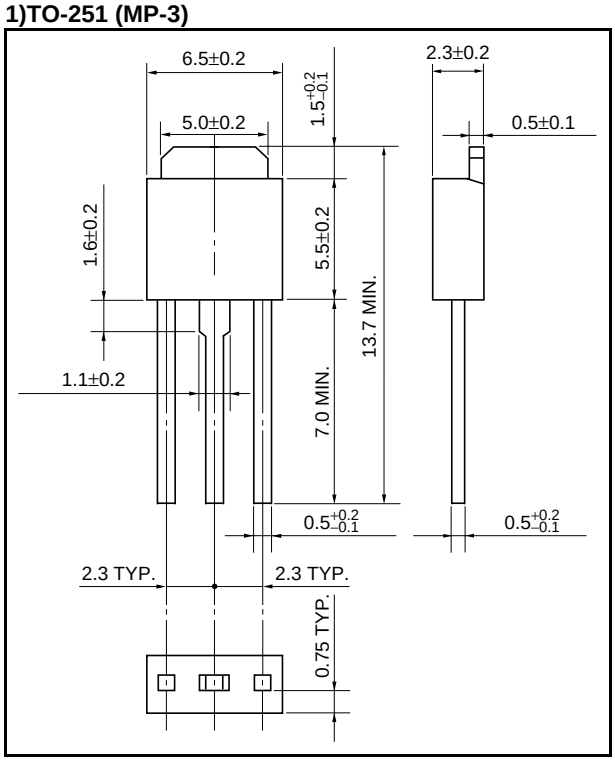



**TEST CIRCUIT 3 GATE CHARGE**

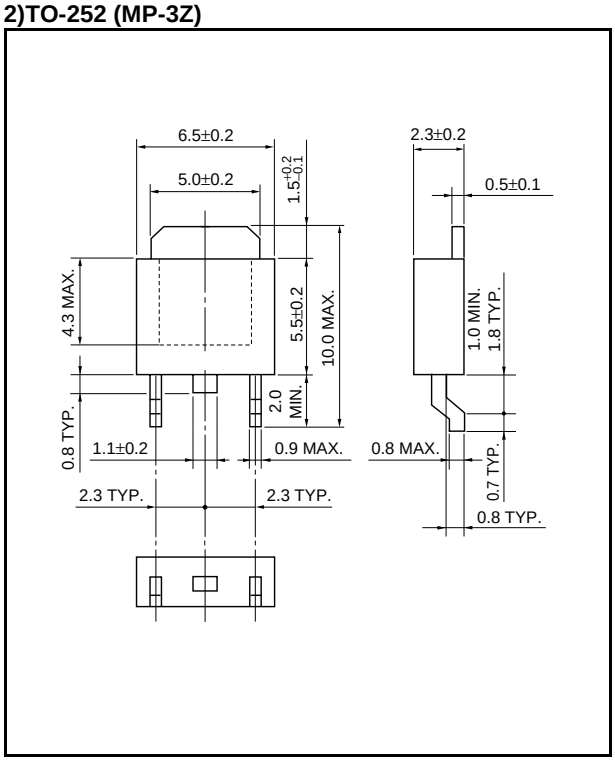


★ **PACKAGE DRAWINGS (Unit : mm)**

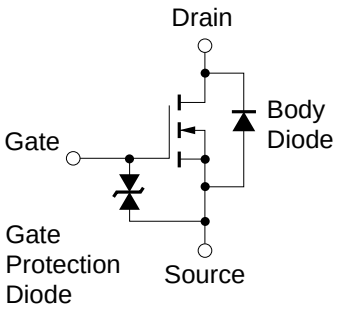
**1)TO-251 (MP-3)**




**2)TO-252 (MP-3Z)**




**EQUIVALENT CIRCUIT**




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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