NEC

MOS FIELD EFFECT TRANSISTOR

NP32N055HLE, NP32N055ILE

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP32N055HLE	TO-251
NP32N055ILE	TO-252

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

  $R_{DS(on)1}$ = 26 mΩ MAX. (V_{GS} = 10 V, I_D = 16 A)

  $R_{DS(on)2}$ = 35 mΩ MAX. (V_{GS} = 5 V, I_D = 16 A)
- Low C_{iss} : C_{iss} = 1090 pF TYP.
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	55	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±32	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±128	A
Total Power Dissipation (T_A = 25°C)	P_T	1.2	W
Total Power Dissipation (T_{ch} = 25°C)	P_T	40	W
Single Avalanche Current	I_{AS}	T.B.D.	A
Single Avalanche Energy Note2	E_{AS}	T.B.D.	mJ
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = 20 V→0 V

THERMAL RESISTANCE

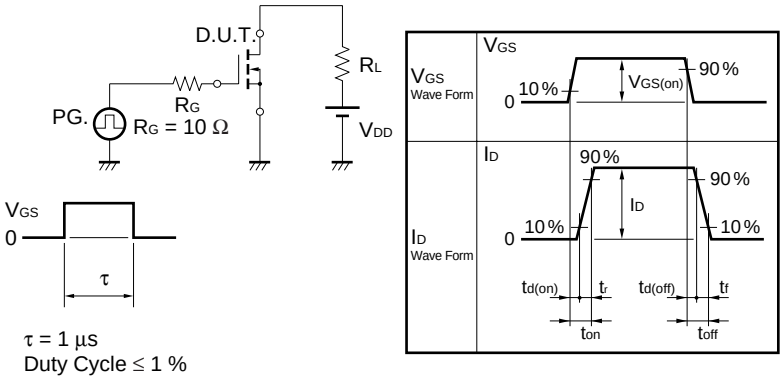
Channel to Case	$R_{th(ch-c)}$	3.75	°C/W
Channel to Ambient	$R_{th(ch-a)}$	125	°C/W

Document No. D14137EJ1V0PM00 (1st edition)
Date Published February 1999 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

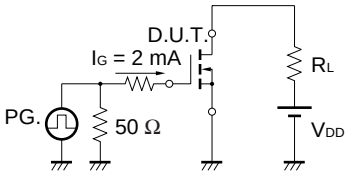
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 16 A		20.8	26	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 16 A		25	35	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 16 A		26	36	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 250 μA	1.5	2	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 16 A	7	13		S
Drain Leakage Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		1090	1640	pF
Output Capacitance	C_{oss}			240	360	pF
Reverse Transfer Capacitance	C_{rss}			99	180	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 16 A, $V_{GS(on)}$ = 10 V, V_{DD} = 28 V,		40	88	ns
Rise Time	t_r	R_G = 10 Ω		190	480	ns
Turn-off Delay Time	$t_{d(off)}$			63	130	ns
Fall Time	t_f			120	300	ns
Total Gate Charge 1	Q_{G1}	I_D = 32 A, V_{DD} = 44 V, V_{GS} = 10 V		21	32	nC
Total Gate Charge 2	Q_{G2}	I_D = 32 A, V_{DD} = 44 V, V_{GS} = 5 V		15	23	nC
Gate to Source Charge	Q_{GS}			3		nC
Gate to Drain Charge	Q_{GD}			6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 32 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 32 A, V_{GS} = 0 V, di/dt = 100A/μs		49		ns
Reverse Recovery Charge	Q_{rr}			100		nC

TEST CIRCUIT 1 SWITCHING TIME



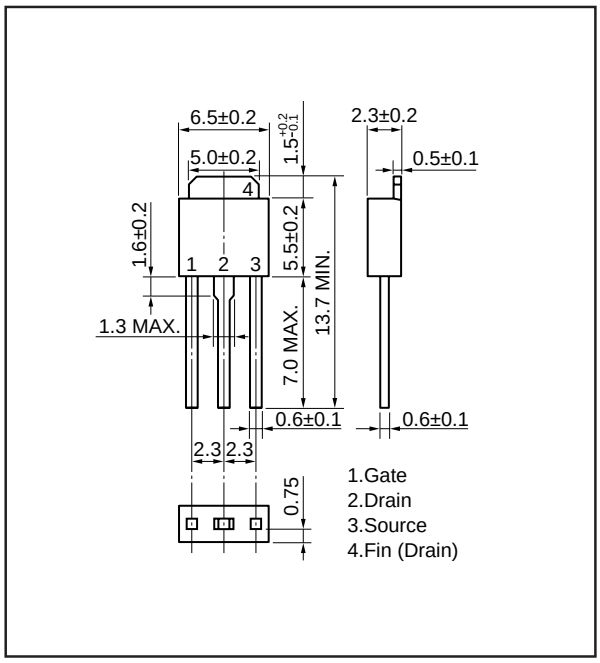
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

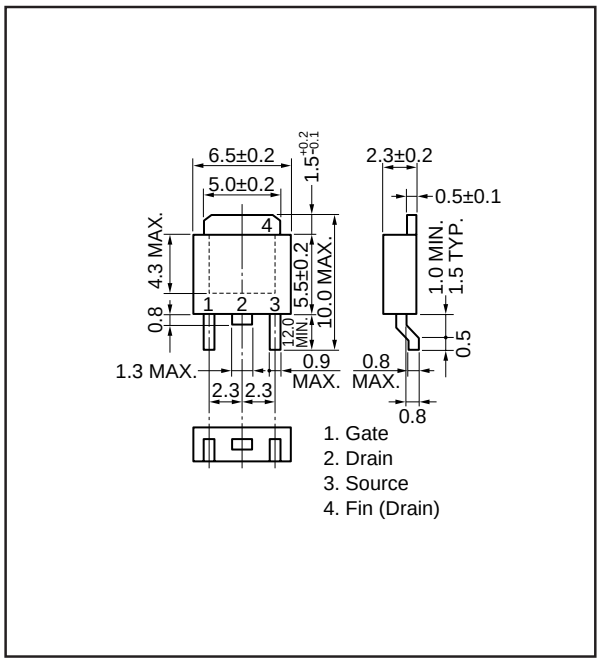


PACKAGE DRAWINGS (Unit: mm)

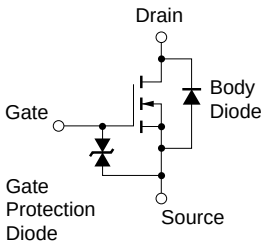
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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