NEC

MOS FIELD EFFECT TRANSISTOR
NP80N03CLE, NP80N03DLE, NP80N03ELE

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP80N03CLE	TO-220AB(MP-25)
NP80N03DLE	TO-262(MP-25 Fin Cut)
NP80N03ELE	TO-263(MP-25ZJ)

FEATURES

- Channel Temperature 175 degree rated
- Super Low On-state Resistance

★ $R_{DS(on)1}$ = 7.0 mΩ MAX. (V_{GS} = 10 V, I_D = 40 A)

★ $R_{DS(on)2}$ = 9.0 mΩ MAX. (V_{GS} = 5 V, I_D = 40 A)

★ • Low C_{iss} : C_{iss} = 2600 pF TYP.

- Built-in Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

	Drain to Source Voltage	V_{DSS}	30	V
	Gate to Source Voltage	V_{GSS}	±20	V
	Drain Current (DC) Note1	$I_{D(DC)}$	±80	A
	Drain Current (Pulse) Note2	$I_{D(pulse)}$	±320	A
	Total Power Dissipation (T_A = 25°C)	P_T	1.8	W
★	Total Power Dissipation (T_C = 25°C)	P_T	120	W
★	Single Avalanche Current	I_{AS}	50 / 40 / 9	A
★	Single Avalanche Energy Note3	E_{AS}	2.5 / 160 / 400	mJ
	Channel Temperature	T_{ch}	175	°C
	Storage Temperature	T_{stg}	–55 to +175	°C

Notes 1. Package Limit = ± 75 A

2. PW ≤ 10 μs, Duty cycle ≤ 1 %

3. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = 20 V→0 V

THERMAL RESISTANCE

★	Channel to Case	R_{th}(ch-C)	1.25	°C/W
	Channel to Ambient	R_{th}(ch-A)	83.3	°C/W

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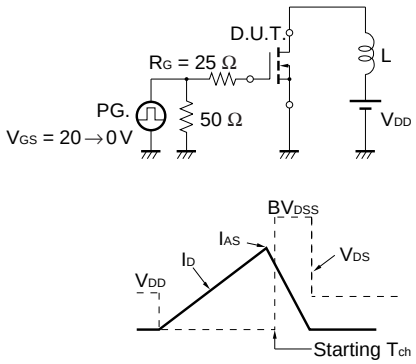
The mark ★ shows major revised points.

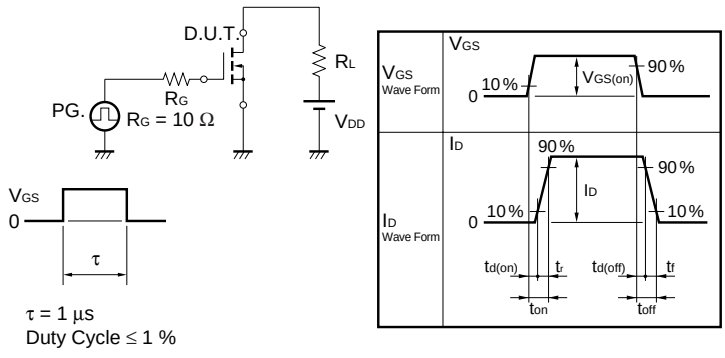
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 40 A		5.3	7.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 40 A		6.8	9.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 40 A		7.5	11	mΩ
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 40 A	20	41		S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		2600	3900	pF
Output Capacitance	C_{oss}			590	890	pF
Reverse Transfer Capacitance	C_{rss}			270	490	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 40 A, $V_{GS(on)}$ = 10 V, V_{DD} = 15 V,		140	310	ns
Rise Time	t_r	R_G = 10 Ω		3000	7500	ns
Turn-off Delay Time	$t_{d(off)}$			180	360	ns
Fall Time	t_f			450	1200	ns
Total Gate Charge 1	Q_{G1}	I_D = 80 A, V_{DD} = 24 V, V_{GS} = 10 V		48	72	nC
Total Gate Charge 2	Q_{G2}	I_D = 80 A, V_{DD} = 24 V, V_{GS} = 5 V		28	42	nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			14		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 80 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 80 A, V_{GS} = 0 V, di/dt = 100A/μs		34		ns
Reverse Recovery Charge	Q_{rr}			22		nC

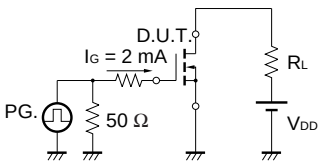
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

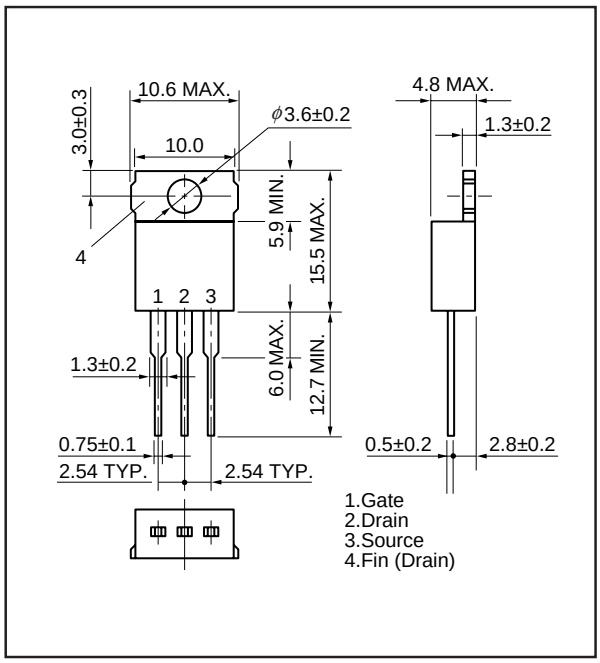


TEST CIRCUIT 3 GATE CHARGE

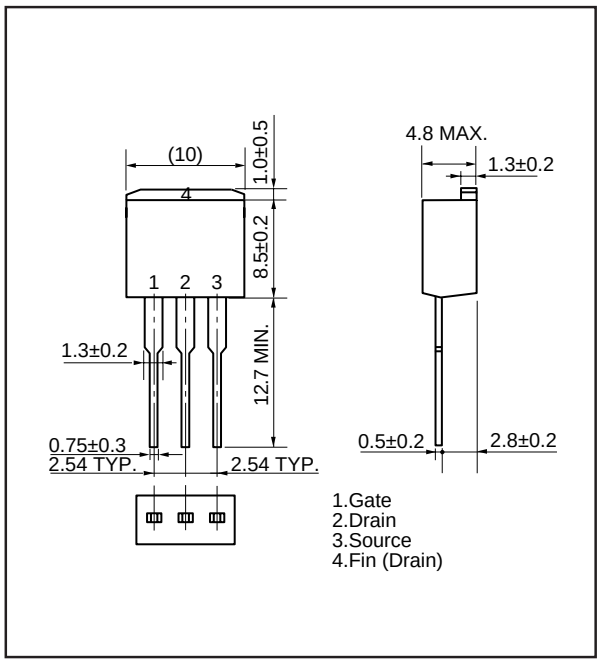


PACKAGE DRAWINGS (Unit: mm)

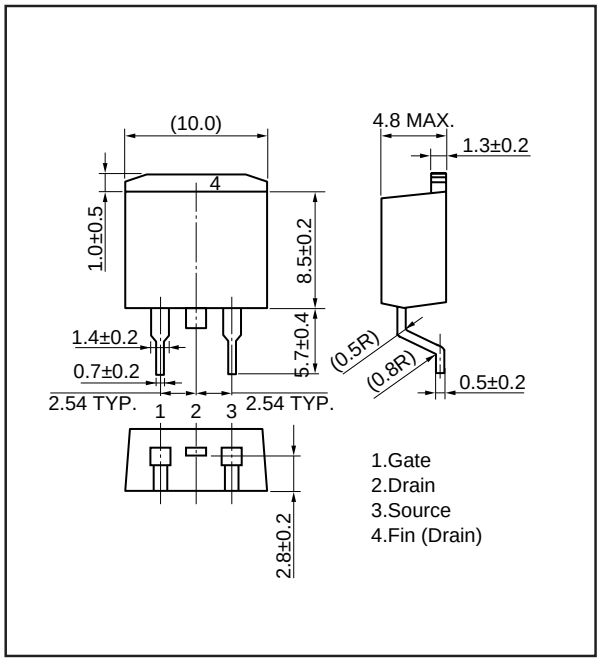
1) TO-220AB (MP-25)



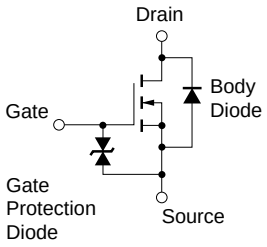
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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