

1Mb Ultra-Low Power Asynchronous CMOS SRAM

128Kx8 bit

Overview

The N01L083WC2A is an integrated memory device containing a 1 Mbit Static Random Access Memory organized as 131,072 words by 8 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The base design is the same as NanoAmp's N01L1618N1A, which is processed to operate at lower voltages. The device operates with two chip enable ($\overline{CE1}$ and $\overline{CE2}$) controls and output enable (\overline{OE}) to allow for easy memory expansion. The N01L083WC2A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to $+85^{\circ}\text{C}$ and is available in JEDEC standard packages compatible with other standard 128Kb x 8 SRAMs

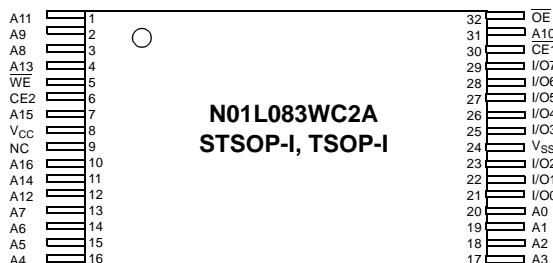
Features

- **Single Wide Power Supply Range**
2.3 to 3.6 Volts
- **Very low standby current**
2.0 μA at 3.0V (Typical)
- **Very low operating current**
2.0mA at 3.0V and 1 μs (Typical)
- **Very low Page Mode operating current**
0.8mA at 3.0V and 1 μs (Typical)
- **Simple memory control**
Dual Chip Enables ($\overline{CE1}$ and $\overline{CE2}$)
Output Enable (\overline{OE}) for memory expansion
- **Low voltage data retention**
 $V_{CC} = 1.8\text{V}$
- **Very fast output enable access time**
30ns \overline{OE} access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (V_{CC})	Speed	Standby Current (I_{SB}), Max	Operating Current (I_{CC}), Max
N01L083WC2AT	32 - TSOP I	-40°C to $+85^{\circ}\text{C}$	2.3V - 3.6V	55ns @ 2.7V 70ns @ 2.3V	20 μA	3 mA @ 1MHz
N01L083WC2AN	32 - STSOP I					

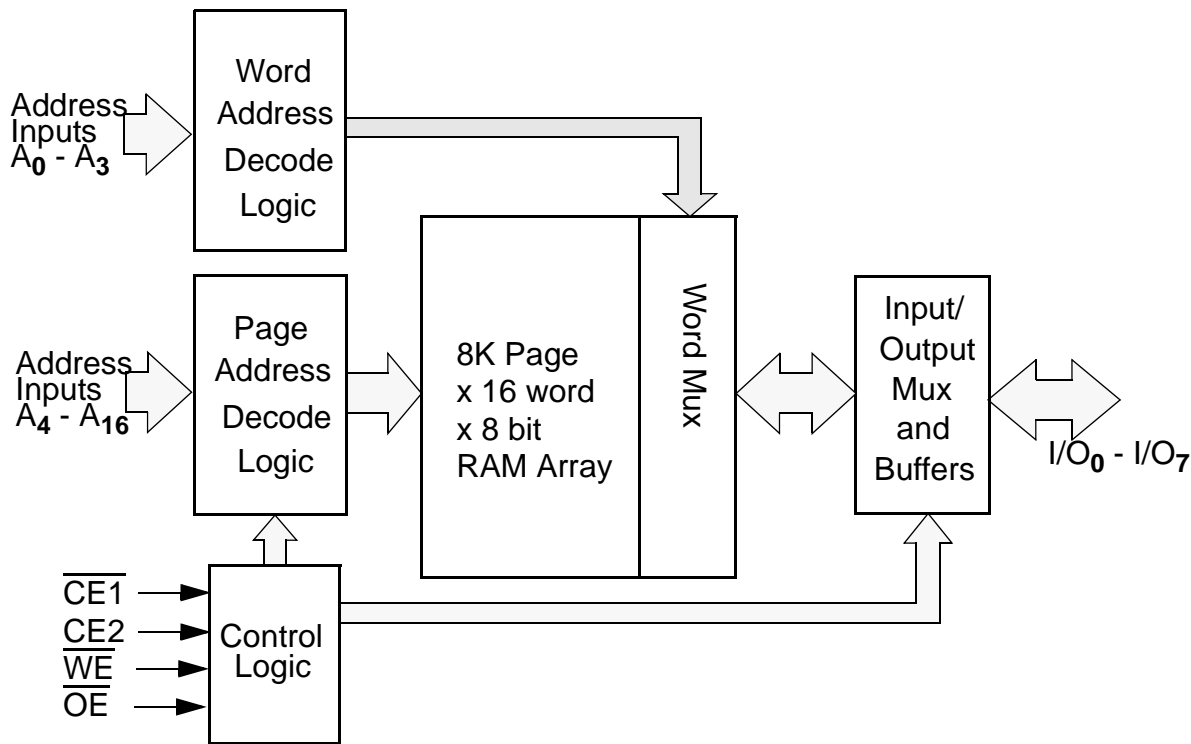
Pin Configuration



Pin Descriptions

Pin Name	Pin Function
A_0 - A_{16}	Address Inputs
\overline{WE}	Write Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Input
\overline{OE}	Output Enable Input
I/O_0 - I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected

Functional Block Diagram



Functional Description

CE1	CE2	WE	OE	I/O ₀ - I/O ₇	MODE	POWER
H	X	X	X	High Z	Standby ¹	Standby
X	L	X	X	High Z	Standby ¹	Standby
L	H	L	X ²	Data In	Write ²	Active
L	H	H	L	Data Out	Read	Active
L	H	H	H	High Z	Active	Active

1. When the device is in standby mode, control inputs (\overline{WE} and \overline{OE}), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
2. When \overline{WE} is invoked, the \overline{OE} input is internally disabled and has no effect on the circuit.

Capacitance¹

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF
I/O Capacitance	C _{I/O}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings¹

Item	Symbol	Rating	Unit
Voltage on any pin relative to V _{SS}	V _{IN,OUT}	-0.3 to V _{CC} +0.3	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.3 to 4.5	V
Power Dissipation	P _D	500	mW
Storage Temperature	T _{STG}	-40 to 125	°C
Operating Temperature	T _A	-40 to +85	°C
Soldering Temperature and Time	T _{SOLDER}	240°C, 10sec(Lead only)	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

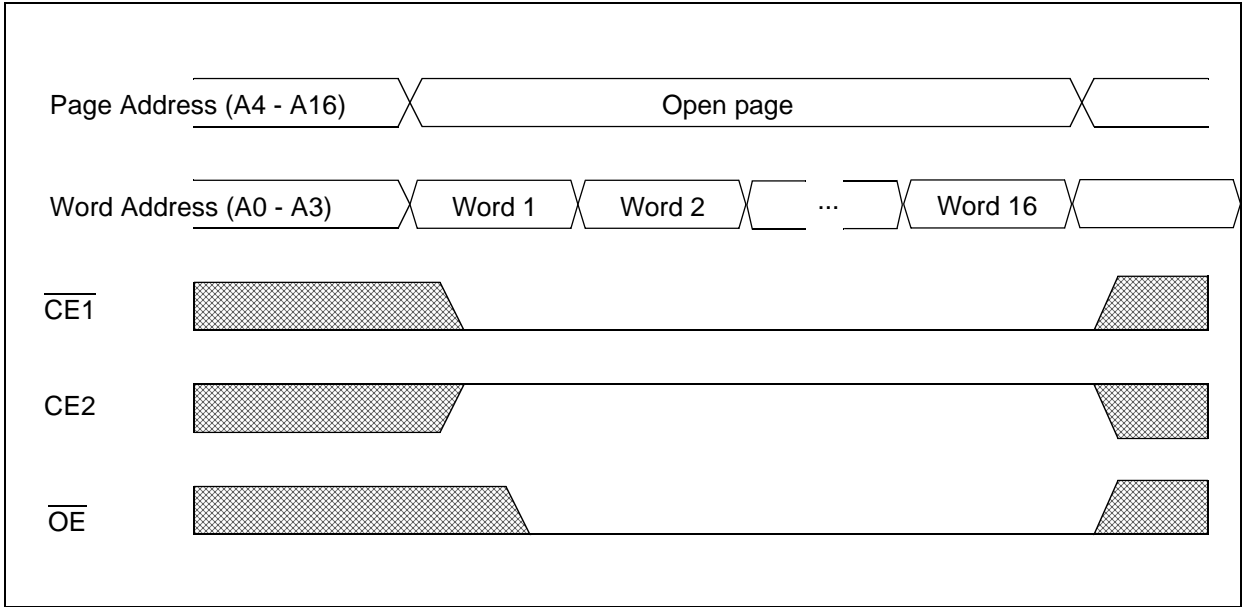
Item	Symbol	Test Conditions	Min.	Typ ¹	Max	Unit
Supply Voltage	V _{CC}		2.3	3.0	3.6	V
Data Retention Voltage	V _{DR}	Chip Disabled ³	1.8			V
Input High Voltage	V _{IH}		1.8		V _{CC} +0.3	V
Input Low Voltage	V _{IL}		-0.3		0.6	V
Output High Voltage	V _{OH}	I _{OH} = 0.2mA	V _{CC} -0.2			V
Output Low Voltage	V _{OL}	I _{OL} = -0.2mA			0.2	V
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC}			0.5	μA
Output Leakage Current	I _{LO}	\overline{OE} = V _{IH} or Chip Disabled			0.5	μA
Read/Write Operating Supply Current @ 1 μS Cycle Time ²	I _{CC1}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		2.0	3.0	mA
Read/Write Operating Supply Current @ 70 nS Cycle Time ²	I _{CC2}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		9.5	14.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time ² (Refer to Power Savings with Page Mode Operation diagram)	I _{CC3}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0,		4		mA
Read/Write Quiescent Operating Supply Current ³	I _{CC4}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0, f = 0			3.0	mA
Maximum Standby Current ³	I _{SB1}	V _{IN} = V _{CC} or 0V Chip Disabled t _A = 85°C, V _{CC} = 3.6 V		2.0	20	μA
Maximum Data Retention Current ³	I _{DR}	V _{CC} = 1.8V, V _{IN} = V _{CC} or 0 Chip Disabled, t _A = 85°C			10	μA

1. Typical values are measured at V_{CC}=V_{CC} Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

Power Savings with Page Mode Operation ($\overline{WE} = V_{IH}$)



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 8-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Load	CL = 30pF
Operating Temperature	-40 to +85 °C

Timing

Item	Symbol	2.3 - 3.6 V		2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70		55		ns
Address Access Time	t_{AA}		70		55	ns
Chip Enable to Valid Output	t_{CO}		70		55	ns
Output Enable to Valid Output	t_{OE}		35		30	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	15	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	15	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	70		55		ns
Chip Enable to End of Write	t_{CW}	50		45		ns
Address Valid to End of Write	t_{AW}	50		45		ns
Write Pulse Width	t_{WP}	40		35		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		15	ns
Data to Write Time Overlap	t_{DW}	40		35		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

The diagram shows two signal traces: Address and Data Out. The Address signal is a horizontal line that transitions from a low state to a high state. The Data Out signal is a horizontal line that transitions from a low state to a high state. The timing parameters are defined as follows:

- t_{RC} : The time interval from the rising edge of the Address signal to the rising edge of the Data Out signal.
- t_{AA} : The time interval from the falling edge of the Address signal to the falling edge of the Data Out signal.
- t_{OH} : The time interval from the falling edge of the Address signal to the falling edge of the Data Out signal.

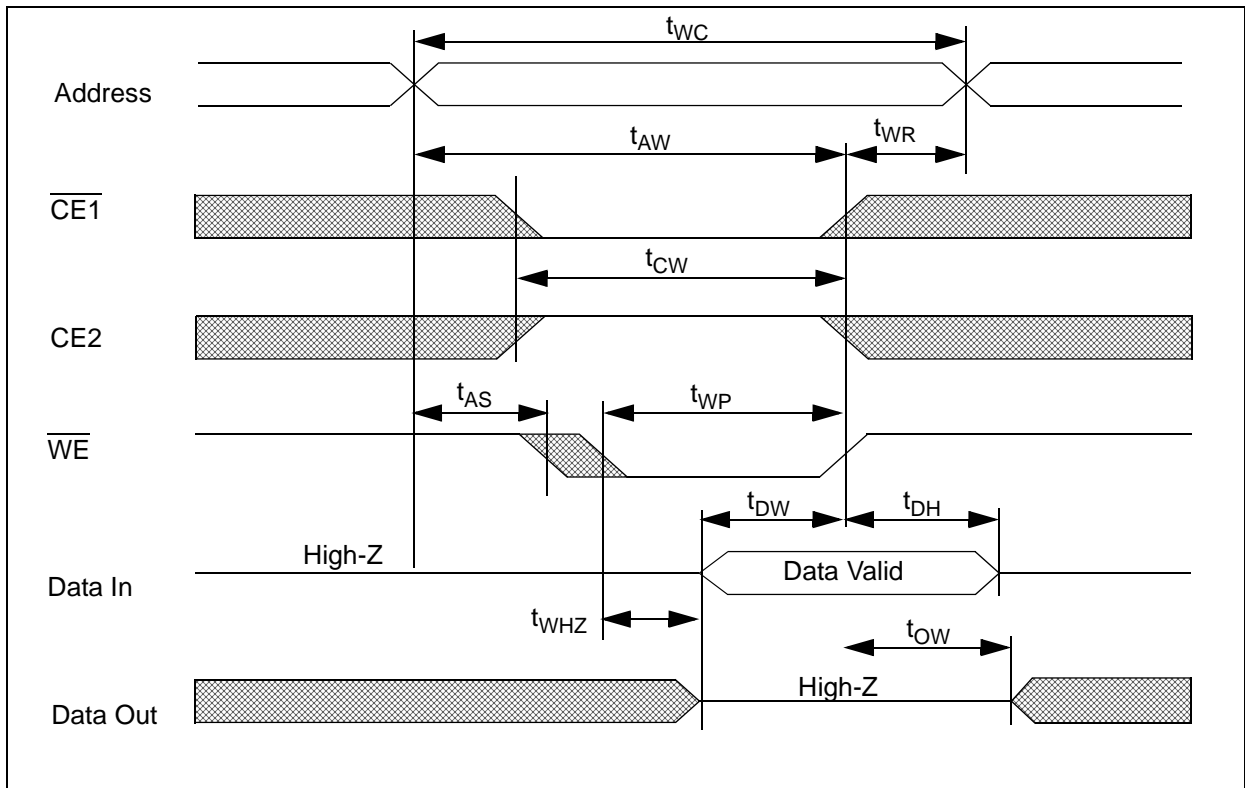
The Data Out signal is labeled "Previous Data Valid" and "Data Valid". The Data Out signal is shown as a shaded area between the rising and falling edges of the Address signal.

The diagram illustrates the timing relationships for a 2-port RAM. The signals shown are Address, $\overline{CE1}$, $\overline{CE2}$, \overline{OE} , and Data Out. The timing parameters are defined as follows:

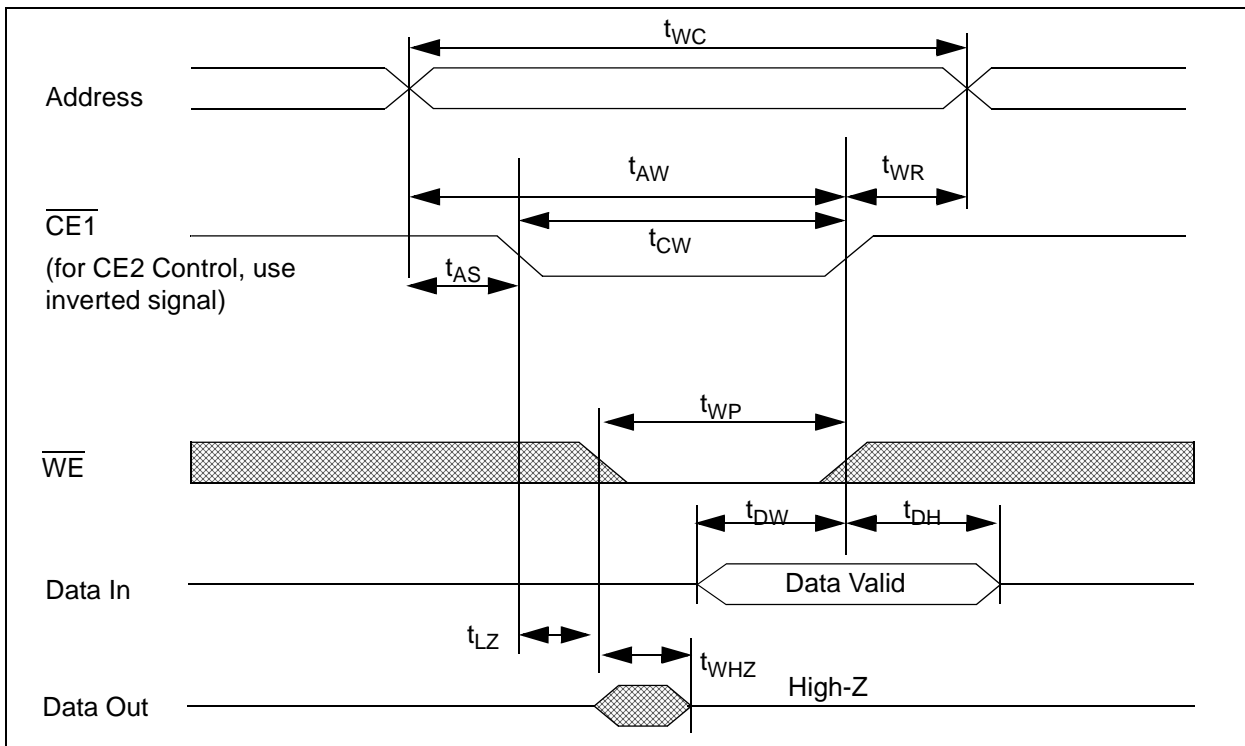
- t_{RC} : Read Cycle time, from the start of the valid address to the end of the high-impedance state of the data output.
- t_{AA} : Address Access time, from the start of the valid address to the start of the data valid period.
- t_{HZ} : High-Z time, from the end of the data valid period to the end of the high-impedance state of the data output.
- t_{CO} : Chip Output time, from the start of the valid address to the end of the data valid period.
- t_{LZ} : Low-Z time, from the start of the valid address to the start of the data valid period.
- t_{OE} : Output Enable time, from the start of the valid address to the end of the data valid period.
- t_{OHZ} : Output High-Z time, from the end of the data valid period to the end of the high-impedance state of the data output.
- t_{OLZ} : Output Low-Z time, from the start of the valid address to the start of the data valid period.

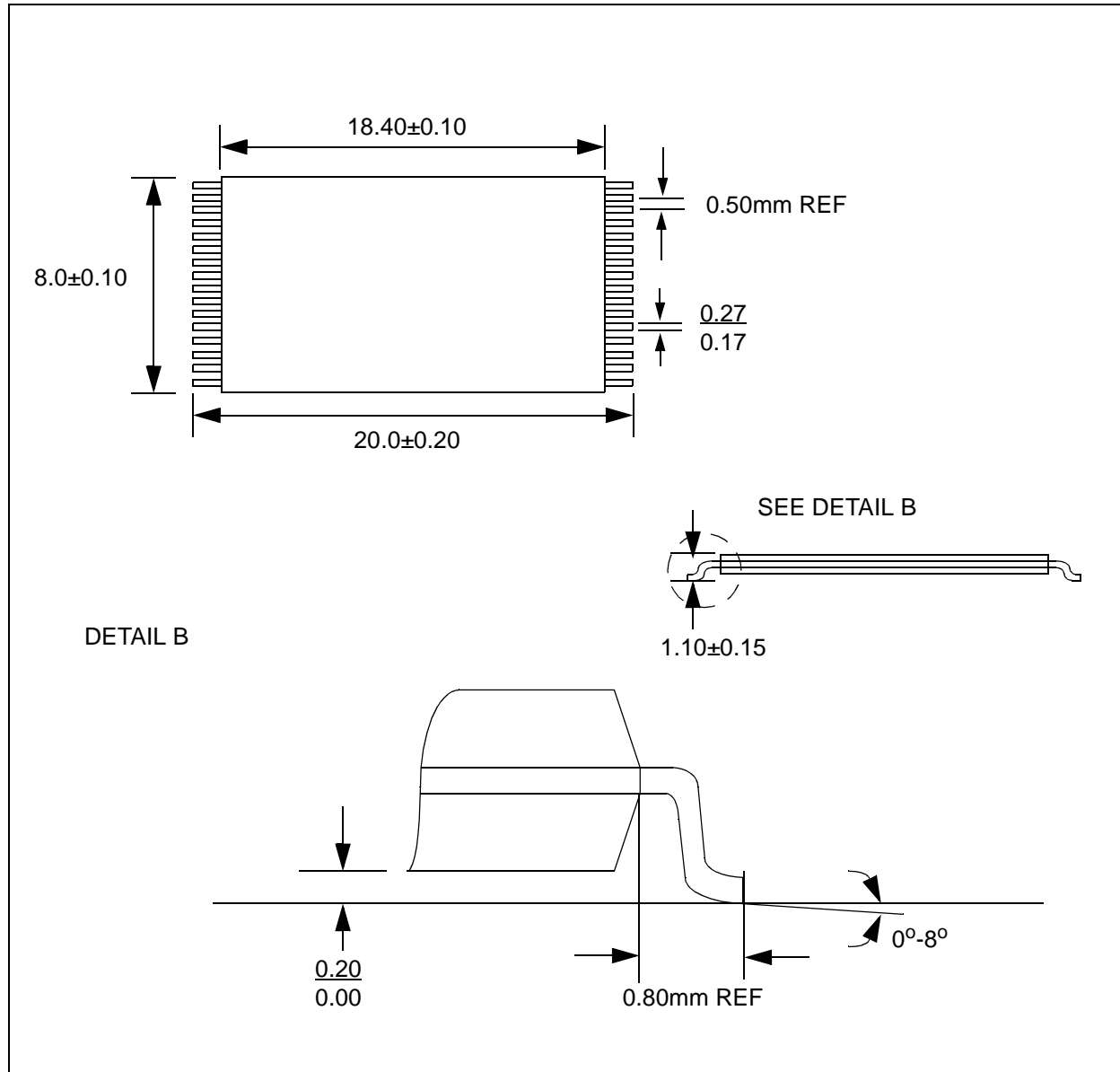
The Data Out signal is shown in a high-impedance state (High-Z) before the valid address is applied and after the data valid period ends. The data valid period is shown as a shaded area between the start and end of the data valid period.

Timing Waveform of Write Cycle ($\overline{\text{WE}}$ control)

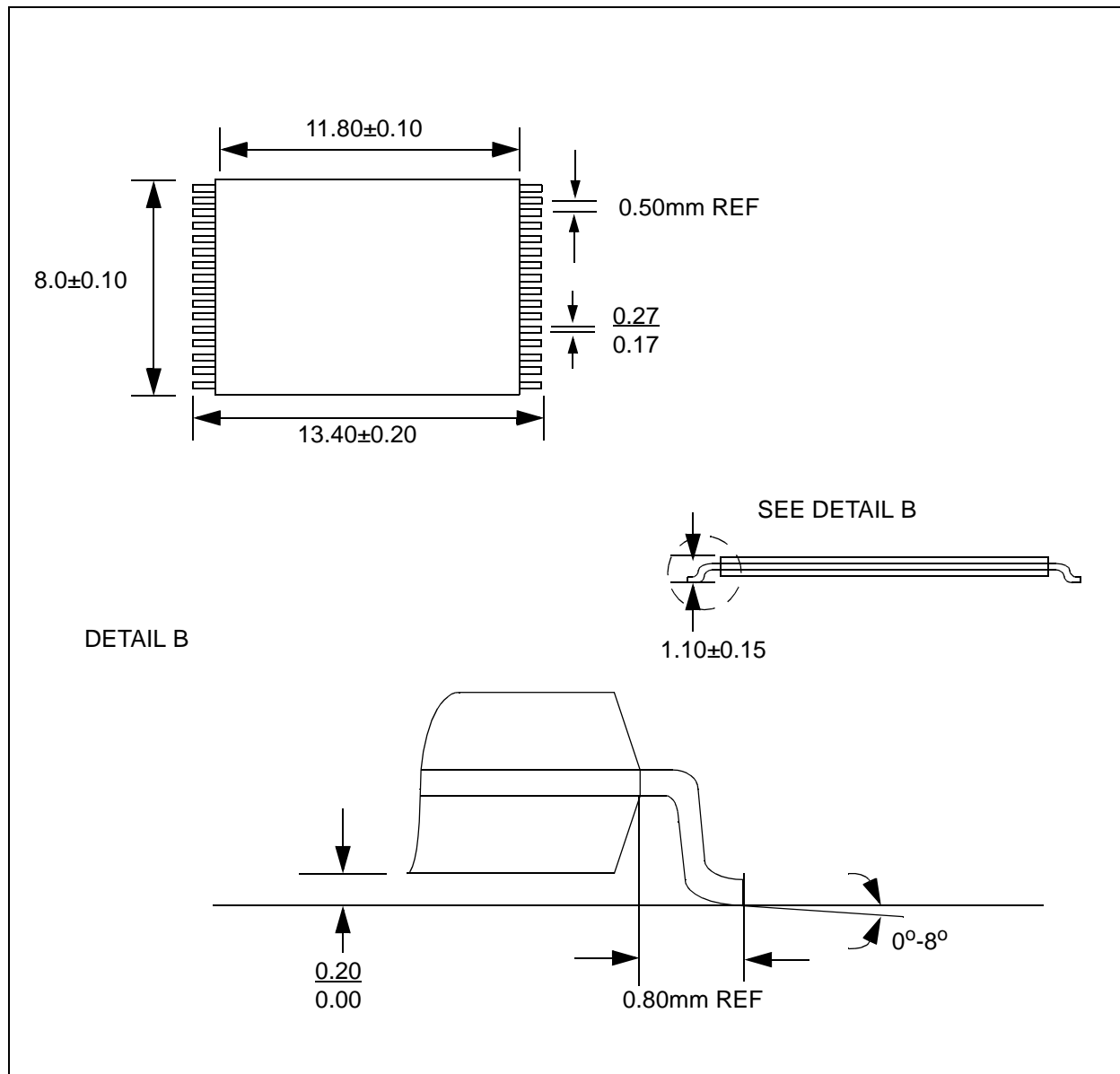


Timing Waveform of Write Cycle ($\overline{\text{CE1}}$ Control)

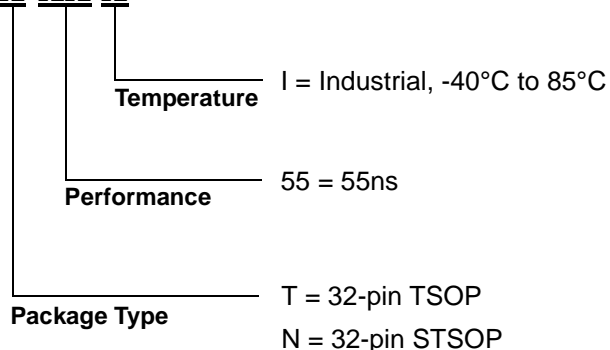


32-Lead TSOP-I Package (T32)**Note:**

1. All dimensions in millimeters
2. Package dimensions exclude molding flash

32-Lead STSOP-I Package (N32)**Note:**

1. All dimensions in millimeters
2. Package dimensions exclude molding flash

Ordering Information**N01L083WC2AX-XX X**

Note: Add -T&R following the part number for Tape and Reel. Orders will be considered in tray if not noted.

Revision History

Revision #	Date	Change Description
01	Jan 2001	Initial Advance Release
02	Mar 2001	Added Table 3: Capacitance Revised quiescent operating current, changed pin 31 to CE1, modified Pin Description and Pin Configuration, other minor edits
03	Dec. 2001	Part number change from EM128L08, modified Overview and Features, added Page Mode Operation diagram and Package diagrams, revised Operating Characteristics table, Functional Description table, Timing diagrams, and Ordering Information diagram

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