

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6455 is a bit map LCD driver to display graphics or characters.

It contains 10,400 bit display data RAM, microprocessor interface circuits, instruction decoder, 128-segment and totally 33-common (32 out of 33-driver can use as both of common and segment) drivers.

The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.

33 x 128 dot graphics or 8-character 2-line by 16 x 16 dot character with icon are displayed by NJU6455 itself.

Also, the NJU6455 can extend its display capacity to 33 x 288 dots of graphics or character display by connecting one more NJU6455.

The wide operating voltage like as 2.4 to 5.5V and low operating current are useful to apply small sized battery operated items.

■ PACKAGE OUTLINE



NJU6455C

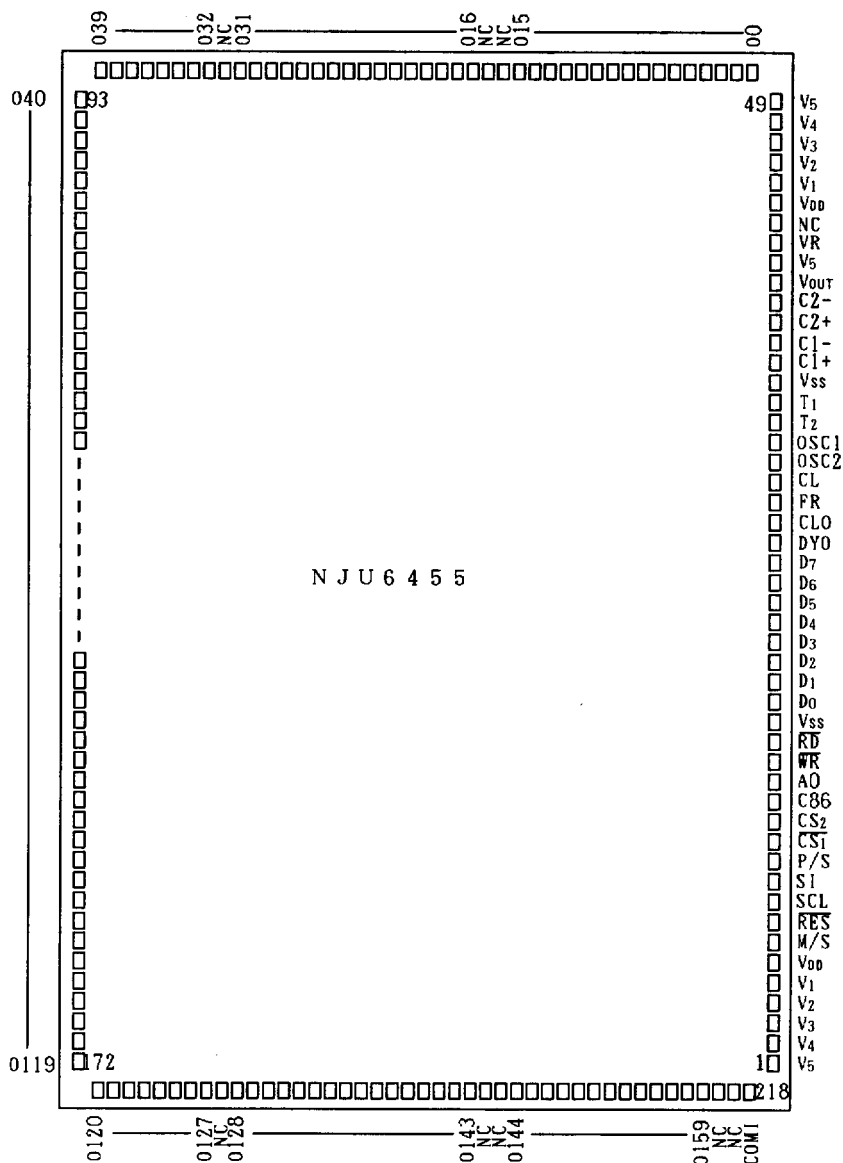
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■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 10,400 bits
- 160 LCD Drivers - 33 common(32 out of 33 can assign as segment driver) or 128-segment
- Number of Common Driver can select by the Instruction
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Extension Function (can combine with one more NJU6455)
- Programmable Duty Ratio ; 1/32 or 1/33 Duty
- Useful Instruction Set
Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Display Starting Line Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistance
- Low Power Consumption
- Incorporated CR Oscillator
- Operating Voltage --- 2.4V ~ 5.5V
- LCD Driving Voltage --- 6.0V ~ 13.5V
- Package Outline --- Chip / Bumped Chip / TCP
- C-MOS Technology



■ PAD LOCATION



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Chip Center X=0um, Y=0um
 Chip Size X=7.77mm, Y=5.09mm
 Chip Thickness 400um $\pm$ 30um
 Pad Size 40um x 100um
 Bump Height 25um TYP.
 Bump Material Au



PAD COORDINATES

Chip Size 7.33mm x 5.09mm(Chip Center X=0um,Y=0um)

PAD No.	Terminal	X=(μ m)	Y=(μ m)
1	V ₅	3335	2327
2	V ₄	3196	2327
3	V ₃	3057	2327
4	V ₂	2918	2327
5	V ₁	2778	2327
6	V _{DD}	2639	2327
7	M/S	2500	2327
8	RST	2361	2327
9	SCL	2222	2327
10	SI	2082	2327
11	P/S	1943	2327
12	CS ₁	1804	2327
13	CS ₂	1665	2327
14	C86	1526	2327
15	A0	1386	2327
16	WR	1247	2327
17	RD	1108	2327
18	V _{SS}	969	2327
19	D ₀	830	2327
20	D ₁	690	2327
21	D ₂	551	2327
22	D ₃	412	2327
23	D ₄	273	2327
24	D ₅	134	2327
25	D ₆	-6	2327
26	D ₇	-145	2327
27	DYO	-284	2327
28	CLO	-423	2327
29	FR	-563	2327
30	CL	-702	2327
31	OSC ₂	-841	2327
32	OSC ₁	-980	2327
33	T ₂	-1119	2327
34	T ₁	-1259	2327
35	V _{SS}	-1398	2327
36	C1 ⁺	-1537	2327
37	C1 ⁻	-1676	2327
38	C2 ⁺	-1815	2327
39	C2 ⁻	-1955	2327
40	V _{OUT}	-2094	2327
41	V ₅	-2233	2327
42	VR	-2372	2327
43	NC	-2511	2327
44	V _{DD}	-2651	2327
45	V ₁	-2790	2327
46	V ₂	-2929	2327
47	V ₃	-3068	2327
48	V ₄	-3207	2327
49	V ₅	-3347	2327
50	O ₀	-3444	1597

PAD No.	Terminal	X=(μ m)	Y=(μ m)
51	O ₁	-3444	1517
52	O ₂	-3444	1437
53	O ₃	-3444	1357
54	O ₄	-3444	1277
55	O ₅	-3444	1197
56	O ₆	-3444	1117
57	O ₇	-3444	1037
58	O ₈	-3444	957
59	O ₉	-3444	877
60	O ₁₀	-3444	797
61	O ₁₁	-3444	717
62	O ₁₂	-3444	637
63	O ₁₃	-3444	557
64	O ₁₄	-3444	477
65	O ₁₅	-3444	397
66	NC	-3444	317
67	NC	-3444	237
68	O ₁₆	-3444	157
69	O ₁₇	-3444	77
70	O ₁₈	-3444	-3
71	O ₁₉	-3444	-83
72	O ₂₀	-3444	-163
73	O ₂₁	-3444	-243
74	O ₂₂	-3444	-323
75	O ₂₃	-3444	-403
76	O ₂₄	-3444	-483
77	O ₂₅	-3444	-563
78	O ₂₆	-3444	-643
79	O ₂₇	-3444	-723
80	O ₂₈	-3444	-803
81	O ₂₉	-3444	-883
82	O ₃₀	-3444	-963
83	O ₃₁	-3444	-1043
84	NC	-3444	-1123
85	O ₃₂	-3444	-1203
86	O ₃₃	-3444	-1283
87	O ₃₄	-3444	-1363
88	O ₃₅	-3444	-1443
89	O ₃₆	-3444	-1523
90	O ₃₇	-3444	-1603
91	O ₃₈	-3444	-1683
92	O ₃₉	-3444	-1763
93	O ₄₀	-3146	-2324
94	O ₄₁	-3066	-2324
95	O ₄₂	-2986	-2324
96	O ₄₃	-2906	-2324
97	O ₄₄	-2826	-2324
98	O ₄₅	-2746	-2324
99	O ₄₆	-2666	-2324
100	O ₄₇	-2586	-2324

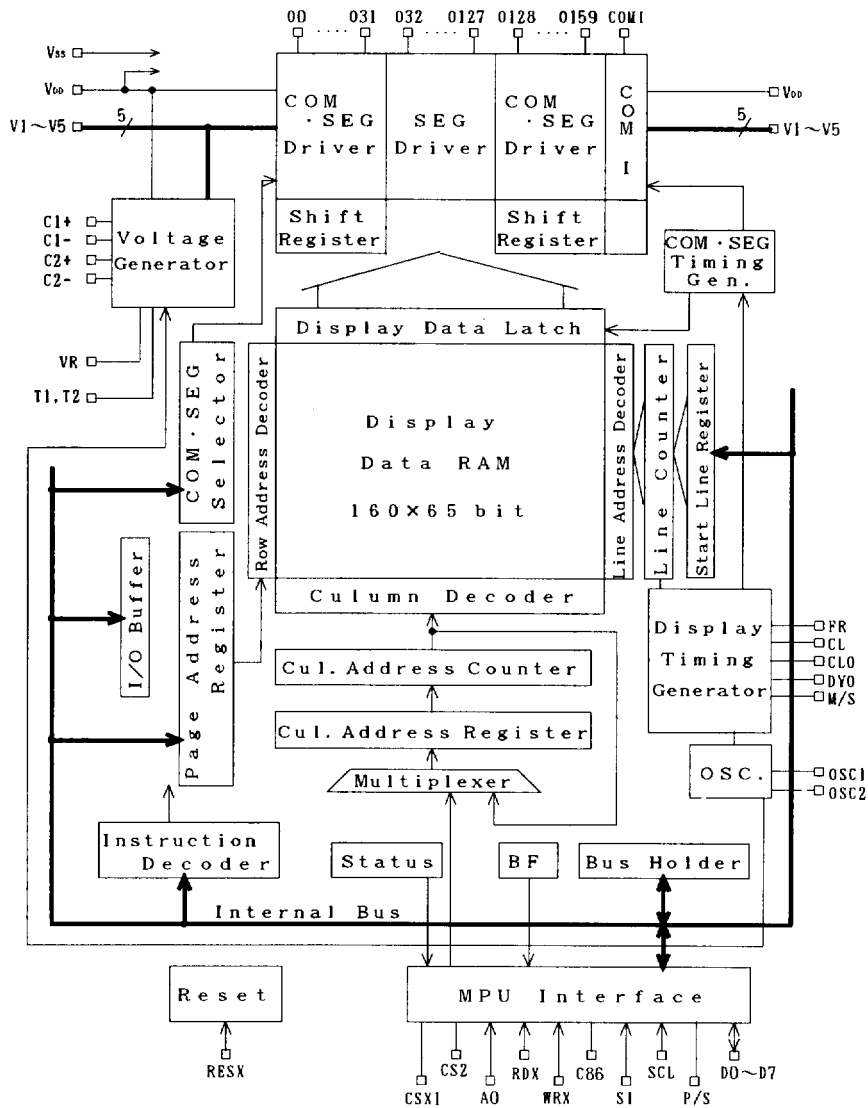
PAD No.	Terminal	X=(μ m)	Y=(μ m)
101	O ₄₈	-2506	-2324
102	O ₄₉	-2426	-2324
103	O ₅₀	-2346	-2324
104	O ₅₁	-2266	-2324
105	O ₅₂	-2186	-2324
106	O ₅₃	-2106	-2324
107	O ₅₄	-2026	-2324
108	O ₅₅	-1946	-2324
109	O ₅₆	-1866	-2324
110	O ₅₇	-1786	-2324
111	O ₅₈	-1706	-2324
112	O ₅₉	-1626	-2324
113	O ₆₀	-1546	-2324
114	O ₆₁	-1466	-2324
115	O ₆₂	-1386	-2324
116	O ₆₃	-1306	-2324
117	O ₆₄	-1226	-2324
118	O ₆₅	-1146	-2324
119	O ₆₆	-1066	-2324
120	O ₆₇	-986	-2324
121	O ₆₈	-906	-2324
122	O ₆₉	-826	-2324
123	O ₇₀	-746	-2324
124	O ₇₁	-666	-2324
125	O ₇₂	-586	-2324
126	O ₇₃	-506	-2324
127	O ₇₄	-426	-2324
128	O ₇₅	-346	-2324
129	O ₇₆	-266	-2324
130	O ₇₇	-186	-2324
131	O ₇₈	-106	-2324
132	O ₇₉	-26	-2324
133	O ₈₀	54	-2324
134	O ₈₁	134	-2324
135	O ₈₂	214	-2324
136	O ₈₃	294	-2324
137	O ₈₄	374	-2324
138	O ₈₅	454	-2324
139	O ₈₆	534	-2324
140	O ₈₇	614	-2324
141	O ₈₈	694	-2324
142	O ₈₉	774	-2324
143	O ₉₀	854	-2324
144	O ₉₁	934	-2324
145	O ₉₂	1014	-2324
146	O ₉₃	1094	-2324
147	O ₉₄	1174	-2324
148	O ₉₅	1254	-2324
149	O ₉₆	1334	-2324
150	O ₉₇	1414	-2324



PAD No.	Terminal	X=(μ m)	Y=(μ m)
151	O ₉₈	1494	-2324
152	O ₉₉	1574	-2324
153	O ₁₀₀	1654	-2324
154	O ₁₀₁	1734	-2324
155	O ₁₀₂	1814	-2324
156	O ₁₀₃	1894	-2324
157	O ₁₀₄	1974	-2324
158	O ₁₀₅	2054	-2324
159	O ₁₀₆	2134	-2324
160	O ₁₀₇	2214	-2324
161	O ₁₀₈	2294	-2324
162	O ₁₀₉	2374	-2324
163	O ₁₁₀	2454	-2324
164	O ₁₁₁	2534	-2324
165	O ₁₁₂	2614	-2324
166	O ₁₁₃	2694	-2324
167	O ₁₁₄	2774	-2324
168	O ₁₁₅	2854	-2324
169	O ₁₁₆	2934	-2324
170	O ₁₁₇	3014	-2324
171	O ₁₁₈	3094	-2324
172	O ₁₁₉	3174	-2324
173	O ₁₂₀	3444	-1763
174	O ₁₂₁	3444	-1683
175	O ₁₂₂	3444	-1603
176	O ₁₂₃	3444	-1523
177	O ₁₂₄	3444	-1443
178	O ₁₂₅	3444	-1363
179	O ₁₂₆	3444	-1283
180	O ₁₂₇	3444	-1203
181	NC	3444	-1123
182	O ₁₂₈	3444	-1043
183	O ₁₂₉	3444	-963
184	O ₁₃₀	3444	-883

PAD No.	Terminal	X=(μ m)	Y=(μ m)
185	O ₁₃₁	3444	-803
186	O ₁₃₂	3444	-723
187	O ₁₃₃	3444	-643
188	O ₁₃₄	3444	-563
189	O ₁₃₅	3444	-483
190	O ₁₃₆	3444	-403
191	O ₁₃₇	3444	-323
192	O ₁₃₈	3444	-243
193	O ₁₃₉	3444	-163
194	O ₁₄₀	3444	-83
195	O ₁₄₁	3444	-3
196	O ₁₄₂	3444	77
197	O ₁₄₃	3444	157
198	NC	3444	237
199	NC	3444	317
200	O ₁₄₄	3444	397
201	O ₁₄₅	3444	477
202	O ₁₄₆	3444	557
203	O ₁₄₇	3444	637
204	O ₁₄₈	3444	717
205	O ₁₄₉	3444	797
206	O ₁₅₀	3444	877
207	O ₁₅₁	3444	957
208	O ₁₅₂	3444	1037
209	O ₁₅₃	3444	1117
210	O ₁₅₄	3444	1197
211	O ₁₅₅	3444	1277
212	O ₁₅₆	3444	1357
213	O ₁₅₇	3444	1437
214	O ₁₅₈	3444	1517
215	O ₁₅₉	3444	1597
216	NC	3444	1677
217	NC	3444	1757
218	COMI	3444	1837

■ BLOCK DIAGRAM



TERMINAL DESCRIPTION

No.	Symbol	I/O	F u n c t i o n																				
6,44	V _{DD}	Power	Power Supply:VDD=5V. Less than 4.5V should be use when voltage tripler using.																				
18,35	V _{SS}	Power	GND :VSS=0V																				
5,45 4,46 3,47 2,48 1,49,41	V ₁ V ₂ V ₃ V ₄ V ₅	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ When M/S="H" and internal power supply are on, internal circuits generated and supply following LCD bias voltage to V ₁ ~ V ₄ terminals. <table><tr><td>Term.</td><td>V₁</td><td>V₂</td><td>V₃</td><td>V₄</td></tr><tr><td>Volt.</td><td>V₅ +5.7/6.7V_{LCD}</td><td>V₅ +4.7/6.7V_{LCD}</td><td>V₅ +2/6.7V_{LCD}</td><td>V₅ +1/6.7V_{LCD}</td></tr></table> (V _{LCD} =V _{DD} -V ₅)	Term.	V ₁	V ₂	V ₃	V ₄	Volt.	V ₅ +5.7/6.7V _{LCD}	V ₅ +4.7/6.7V _{LCD}	V ₅ +2/6.7V _{LCD}	V ₅ +1/6.7V _{LCD}										
Term.	V ₁	V ₂	V ₃	V ₄																			
Volt.	V ₅ +5.7/6.7V _{LCD}	V ₅ +4.7/6.7V _{LCD}	V ₅ +2/6.7V _{LCD}	V ₅ +1/6.7V _{LCD}																			
36 37 38 39	C1 ⁺ C1 ⁻ C2 ⁺ C2 ⁻	O	Step up capacitor connecting terminals. In case of tripler operation, connect the capacitor between C1 ⁺ and C1 ⁻ , C2 ⁺ and C2 ⁻ . In case of doubler operation, connect the capacitor between C2 ⁺ and C2 ⁻ , connect C2 ⁺ to C1 ⁺ , and C1 ⁻ should be open.																				
40	V _{OUT}	O	Step up voltage output terminal. Connect the capacitor between this terminal and V _{SS} .																				
42	VR	I	Voltage adjust terminal. V ₅ level is adjusted by external bleeder resistance al connect between V _{DD} and V5 terminal.																				
34,33	T ₁ ,T ₂	I	LCD bias voltage control terminals. ※ Don't Care <table><tr><td>T₁</td><td>T₂</td><td>Step up cir.</td><td>Voltage Adj.</td><td>V/F Cir.</td></tr><tr><td>L</td><td>※</td><td>Available</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr></table>	T ₁	T ₂	Step up cir.	Voltage Adj.	V/F Cir.	L	※	Available	Available	Available	H	L	Not Avail.	Available	Available	H	H	Not Avail.	Not Avail.	Available
T ₁	T ₂	Step up cir.	Voltage Adj.	V/F Cir.																			
L	※	Available	Available	Available																			
H	L	Not Avail.	Available	Available																			
H	H	Not Avail.	Not Avail.	Available																			
19 ~ 26	D ₀ ~ D ₇	I/O	Tri-state bilateral Data I/O terminal when 8-bit parallel operation.																				
15	A0	I	Connect to the Address bus of MPU. The data on the D ₀ to D ₇ is distinguished Display data or Instruction by this signal. <table><tr><td>A0</td><td>H</td><td>L</td></tr><tr><td>Dist.</td><td>Display Data</td><td>Instruction</td></tr></table>	A0	H	L	Dist.	Display Data	Instruction														
A0	H	L																					
Dist.	Display Data	Instruction																					
8	RES	I	Reset terminal. When the RES signal goes to "L", the initialization is performed. Reset operation is executing during "L" state of RES.																				
12 13	CS ₁ CS ₂	I	Chip select terminal. Data I/O is available by following setting. <table><tr><td>Terminal</td><td>CS₁</td><td>CS₂</td></tr><tr><td>State</td><td>"L"</td><td>"H"</td></tr></table>	Terminal	CS ₁	CS ₂	State	"L"	"H"														
Terminal	CS ₁	CS ₂																					
State	"L"	"H"																					
17	RD (E)	I	<When interface with 80 type MPU> RD signal of 80 type MPU input terminal. Active "L". During this signal "L", the data bus becomes as output terminal. <When interface with 68 type MPU> Enable clock of 68 type MPU input terminal. Active "H".																				

No.	Symbol	I/O	F u n c t i o n																								
16	WR (R/W)	I	<When interface with 80 type MPU> Connect the 80 type MPU WR signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal. <When interface with 68 type MPU> Read/write control signal of 68 type MPU input terminal. <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	State	Read	Write																		
R/W	H	L																									
State	Read	Write																									
14	C86	I	Select the MPU interface type. <table><tr><td>C86</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr></table>	C86	H	L	Status	68 Type	80 Type																		
C86	H	L																									
Status	68 Type	80 Type																									
10	SI	I	Serial data input terminal when serial data interface.																								
9	SCL	I	Serial data clock signal input terminal when serial data interface. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.																								
11	P/S	I	Serial or parallel interface select terminal. <table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr><tr><td>"H"</td><td>CS₁, CS₂</td><td>A₀</td><td>D₀ ~ D₇</td><td>RD, WR</td><td>—</td></tr><tr><td>"L"</td><td>CS₁, CS₂</td><td>A₀</td><td>SI</td><td>Write only</td><td>SCL</td></tr></table> *RAM data and status read operation is impossible when select the serial interface. - When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L". - When select the serial interface (P/S="L"), RD and WR must be fix "H" or "L", and D₀ ~ D₇ becomes to the high impedance state.	P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK	"H"	CS ₁ , CS ₂	A ₀	D ₀ ~ D ₇	RD, WR	—	"L"	CS ₁ , CS ₂	A ₀	SI	Write only	SCL						
P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK																						
"H"	CS ₁ , CS ₂	A ₀	D ₀ ~ D ₇	RD, WR	—																						
"L"	CS ₁ , CS ₂	A ₀	SI	Write only	SCL																						
7	M/S	I	Select the Master or Slave operation. <table><tr><td>M/S</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Master</td><td>Slave</td></tr></table> The function of oscillator, internal power supply, FR, OSC₁ and OSC₂ change by the M/S setting. <table><tr><td>Status</td><td>OSC</td><td>Power S</td><td>FR</td><td>OSC₁</td><td>OSC₂</td></tr><tr><td>Master</td><td>Available</td><td>Available</td><td>Out</td><td>In</td><td>Out</td></tr><tr><td>Slave</td><td>Not Avail</td><td>Not Avail</td><td>In</td><td>NC</td><td>In</td></tr></table>	M/S	H	L	State	Master	Slave	Status	OSC	Power S	FR	OSC ₁	OSC ₂	Master	Available	Available	Out	In	Out	Slave	Not Avail	Not Avail	In	NC	In
M/S	H	L																									
State	Master	Slave																									
Status	OSC	Power S	FR	OSC ₁	OSC ₂																						
Master	Available	Available	Out	In	Out																						
Slave	Not Avail	Not Avail	In	NC	In																						
32 31	OSC ₁ OSC ₂	I I/O	Oscillator Resistance connecting terminals. - In case of Master mode operation Oscillation resistance R_f connecting between OSC₁ and OSC₂. OSC₂ is output terminal of internal oscillator. - In case of slave mode operation. OSC₂ is a input terminal of the oscillation signal. OSC₁ must be open. *Fix the CL terminal to V_{ss} level when use internal oscillator for display clock.																								



No.	Symbol	I/O	F u n c t i o n																																	
30	CL	I	Display clock input terminal. This signal latch the display data. The line counter increment at the rise edge and the LCD waveform renew at the fall edge. *When the display clock input from outside, fix the OSC ₁ terminal to V _{DD} and the OSC ₂ terminal to V _{SS} . then reset by RES signal.																																	
28	CLO	O	Display clock output terminal. Display clock output only in Master mode. In case of slave mode, this terminal put on high impedance state.																																	
29	FR	I/O	Alternate signal for LCD input/output terminal. If the two NJU6455 using as a master and slave, connect both FR terminal each other. <table><tr><td>M/S</td><td>H</td><td>L</td></tr><tr><td>FR</td><td>Output</td><td>Input</td></tr></table>	M/S	H	L	FR	Output	Input																											
M/S	H	L																																		
FR	Output	Input																																		
27	DYO	O	Common timing synchronization signal output terminal. Connect to DIO terminal each other.																																	
50 ~ 65 68 ~ 83 85 ~ 180 182 ~ 197 200 ~ 215	O ₀ ~ O ₁₆ O ₁₆ ~ O ₃₁ O ₃₂ ~ O ₁₂₇ O ₁₂₈ ~ O ₁₄₃ O ₁₄₄ ~ O ₁₅₉	O	LCD drive output terminals. • Both as a Common and Segment output terminals : O ₀ to O ₃₁ , O ₁₂₈ to O ₁₅₉ • Segment exclusive output terminals : O ₃₂ to O ₁₂₇ *Common or Segment in Common and Segment output terminals is set by the instruction. • Segment output terminal Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM. <table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V₂</td></tr><tr><td>L</td><td>V₅</td><td>V₃</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V₂</td><td>V_{DD}</td></tr><tr><td>L</td><td>V₃</td><td>V₅</td></tr></table> • Common Output Terminal Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data. <table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V₅</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V₁</td></tr><tr><td>L</td><td>V₄</td></tr></table>	RAM Data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅	Scan data	FR	Output Voltage	H	H	V ₅	L	V _{DD}	L	H	V ₁	L	V ₄
RAM Data	FR	Output Voltage																																		
		Normal	Reverse																																	
H	H	V _{DD}	V ₂																																	
	L	V ₅	V ₃																																	
L	H	V ₂	V _{DD}																																	
	L	V ₃	V ₅																																	
Scan data	FR	Output Voltage																																		
H	H	V ₅																																		
	L	V _{DD}																																		
L	H	V ₁																																		
	L	V ₄																																		
210	COMI	O	Icon common exclusive output terminal. Icon common exclusive output when Icon Display instruction execution. <table><tr><td></td><td>Icon Display ON</td><td>Icon Display OFF</td></tr><tr><td>State</td><td>COM₃₂</td><td>V₁ or V₄</td></tr></table>		Icon Display ON	Icon Display OFF	State	COM ₃₂	V ₁ or V ₄																											
	Icon Display ON	Icon Display OFF																																		
State	COM ₃₂	V ₁ or V ₄																																		

(Terminals 43, 66, 67, 84, 181, 198, 199, 216, 217 are NC)



■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction except the status read are inhibited.

The busy flag output from D₇ terminal when status read instruction is executed.

If enough cycle time over than t_{cyc} is kept, no need to check the busy flag and it realized high performance for the MPU.

(1-2) Display Start Line Register

The Display Start Line Register is a pointer register which indicate the address in the Display Data RAM corresponded with COM₀. (normally it display the top line in the LCD Panel). This register can use for scroll the screen, change the display page and so on. The Display Start Line Set instruction set the display start address of the Display Data RAM represented in 6-bit to this register. When Icon Display Instruction is executed, the icon display RAM address set automatically as a last display line as shown in Fig. 1. During Icon Display Instruction do not executed, the icon display RAM address do not selected.

(1-3) Line Counter

The Display Start Address stored in the Display Start Line Register is set to the Line Counter when the FR signal changing. The Line Counter count up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

(1-4) Column Address Counter

The column address counter is 8-bit presetable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to (A0)_H when the Display Data Read/Write instruction is executed.

The count up is stop at (A0)_H, do not count up non existing address of over than (A0)_H by the count lock function. This count lock is released by new column address set.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-5) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "8"(D3="H" and D2=D1=D0="L") is Icon exclusive RAM area, the data only for the D0 is valid.

(1-6) Display Data RAM

Display Data RAM consists of 10,400 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM output 160-bit parallel data addressed by the line counter, and these data are set in to the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize rewriting.

The relation between column address and segment output can inverse by the Address Inverse Instruction A DC as shown in Fig. 1.

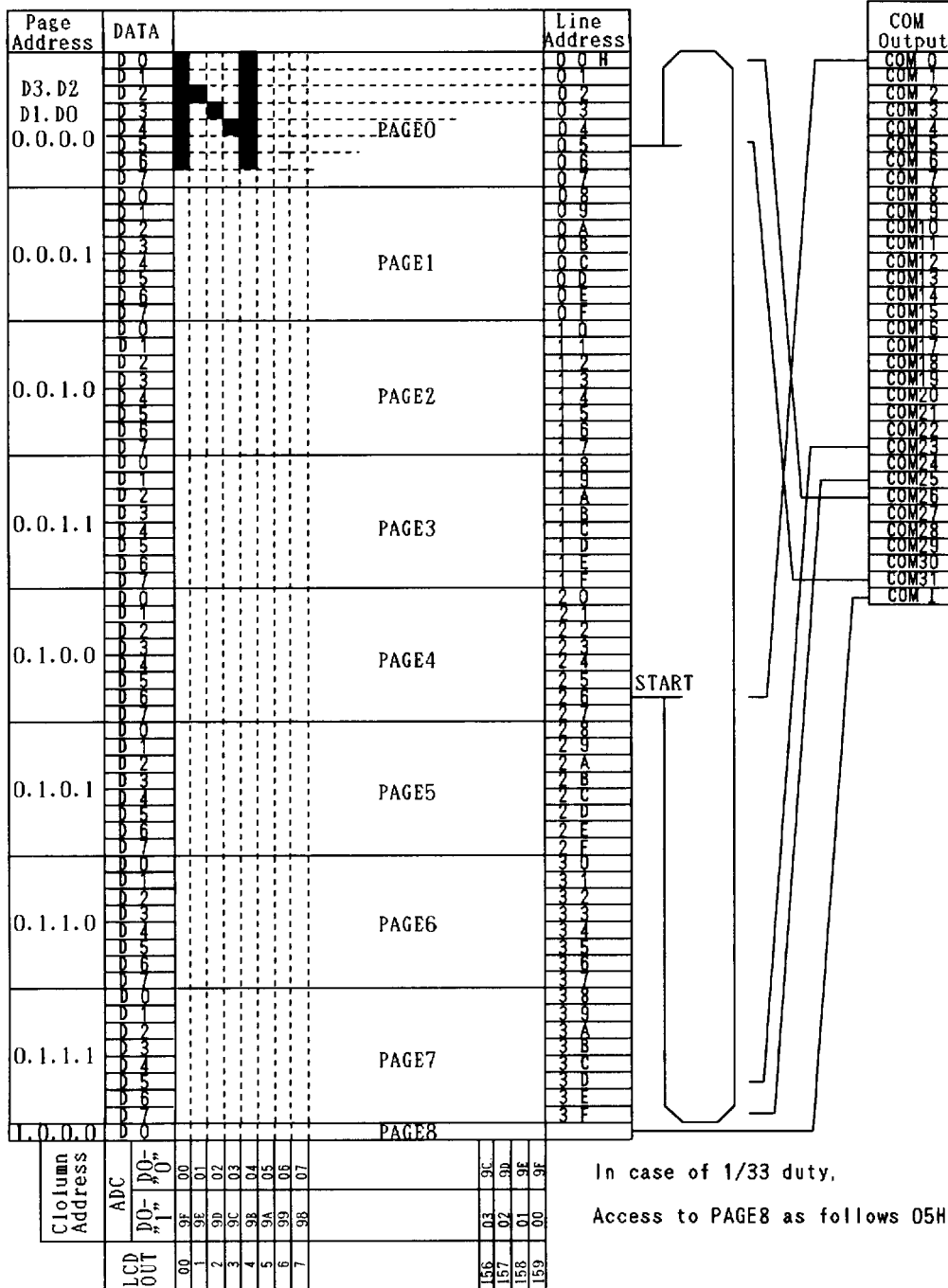


Fig.1 Correspondence with Display Data RAM and Address
(For example the Display start line is 26th)

(1-7) Common and Segment Driver Assignment

NJU6455 incorporates 160 LCD driver and 1 Icon exclusive LCD driver. For easy assembly, 64 LCD driver can assign as both of Common and Segment driver and 96 LCD drivers are fixed as a segment driver.

Can assign as both of Common and Segment Driver — O_0 to O_{31} and O_{128} to O_{159}

Assign only to Segment Driver — O_{32} to O_{127}

When the Output Assignment Register Set instruction which select one assignment from case 1 to case 4, is executed, each LCD driver is fixed its function automatically as shown below table 1;

Table 1

ADC (D ₀)	L	0 →	→ 159
	H	159 ←	← 0
		Column Address	
		Display Data RAM	

Case	Status Register				LCD Driver Assignment															
	D ₃	D ₂	D ₁	D ₀	O ₀	O ₁₅	O ₁₆	O ₃₁	O ₃₂	O ₁₂₇	O ₁₂₈	O ₁₄₃	O ₁₄₄	O ₁₅₉						
1	0	*	1	1	COM ₃₁ ← COM ₀				SEG ₁₂₈											
	1	*	1	1	COM ₀ → COM ₃₁				SEG ₁₂₈											
2	0	*	1	0	SEG ₁₂₈								COM ₀ → COM ₃₁							
	1	*	1	0	SEG ₁₂₈								COM ₃₁ ← COM ₀							
3	0	*	0	1	COM ₁₅ ← 0				SEG ₁₂₈								COM ₁₅ → 31			
	1	*	0	1	COM ₁₆ → 31				SEG ₁₂₈								COM ₁₅ ← 0			
4	*	*	0	0	SEG ₁₆₀															

(* : Don't Care)

Though the MCU can access to whole column address space of the Display RAM, but the column address are which assign as the Common Driver can not to use for the data display area, or, display(segment) data store address must be control by the MCU software. Icon display is regardless with this function, therefore Icon Display Instruction must be executed when Icon display needed. In this time, the Icon display Driver COM₁ is fixed to COM₃₂ regardless the other Common Driver assignment. Case1 through Case4 is selected by setting the lower two bits of D₀ and D₁, and the Common Driver scanning order is also set by "1", or "0" written into D₃ in same time.

Master/Slave operation and LCD Driver assignment function are independent completely, therefor in the multi-chip application the Common driving function can assign either one of Master or Slave chip.

(1-8) Reset Circuits

The NJU6455 performs following initialization when the RST input is put on the "L" level.

Initialization

- ① Display Off
- ② Normal Display(Non-inverse display)
- ③ Icon Display Reset
- ④ ADC Select : Normal (ADC Instruction D₀="1")
- ⑤ Read Modify Write Mode Off
- ⑥ Internal Power supply(Step up) circuits Off
- ⑦ Clear the serial interface register
- ⑧ Set the 1st line to the Display Start Register
- ⑨ Set the address (00)_H to the Column Address Counter
- ⑩ Set the page "0" to the Page Address Register
- ⑪ Select the Case 4 of the LCD Driver Assignment
- ⑫ Set the EVR register to (00)_H

The RES terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Example". The reset signal require over than 10us RES="L" level input as shown in "Electrical Characteristics".

After 1us from the rise edge of RES signal, the normal operation is starting.



In case of the internal power supply(Step up) circuits do not use, the $\overline{\text{RES}}$ terminal must be "L" when external power supply turn on. $\overline{\text{RES}}$ ="L" input reset internal register and set above default, but oscillation circuits and output terminals like as OSC2, FR, CLO, DYO, and D0 through D7 are no influence.

No initialization by $\overline{\text{RES}}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{\text{RES}}$ when power turns on. By the reset Instruction performs only ⑧ through ⑫ mentioned in above.

The noise into the $\overline{\text{RES}}$ terminal should be cared when of the application design to avoid the error function.

(1-9) LCD Driving

(a) LCD Driving Circuits

NJU6455 incorporate 160 LCD Drivers like as 96 Segment exclusive drivers, 64 both of Common and Segment drivers and 1 Icon exclusive driver. Both of Common and Segment drivers incorporate the shift register which scan the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 160-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch circuits are generated from display clock(CL). The line address is renewed by synchronizing with display clock and 160 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock and Driving Signal FR. The Frame Signal FR has a function to generate the 2 frame alternative driving method wave form for the LCD panel, and synchronizing the line counter and common timing generator to the master LSI. Therefore, the FR signal must be 50% duty ratio clock signal which synchronized with the frame signal. When NJU6455 use as a slave, the FR terminal change to the input terminal.

(e) Common Timing Generation

The common timing and Common synchronizing signal(DYO) is generated by display clock. And the divided signal of oscillation signal is output from CLO terminal. The DYO output "H" pulse just one display clock before to the synchronized signal (FR) changing(refer to Fig.2). The DYO outputs regardless the Master or Slave. When the Slave selection, the duty setting must be adjust to the Master. In case of the Multi-chip application, the FR signal must supply from Master chip. The status of FR, CLO, and DYO are as follows;

Table 2

Ope. Mode	FR	CLO	DYO
Master	Output	CL Out	Output
Slave	Input	HZ	Output

* HZ indicate High impedance state.

5

Waveform of Display Timing

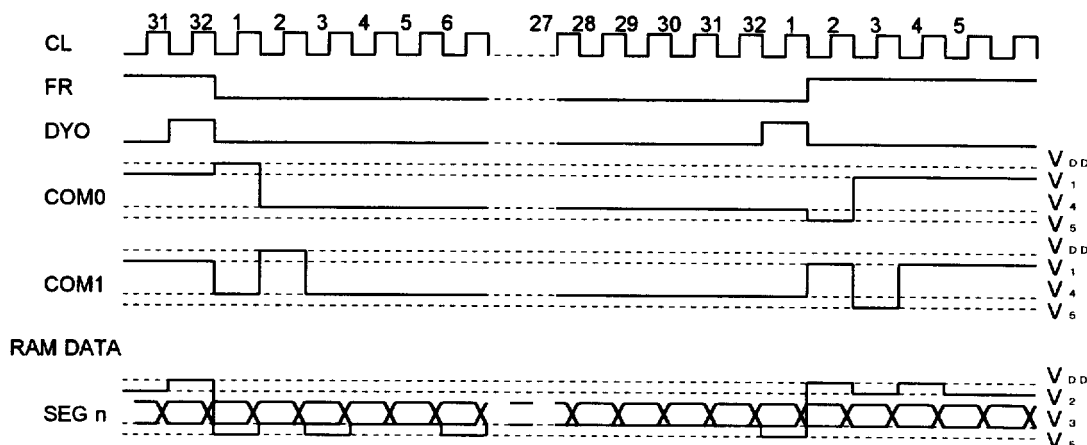


Fig. 2

(f) Oscillation Circuits

The Oscillation Circuits which required external oscillating resistance R_f , is a low power CR oscillator and it is used for display timing signal source, the clock for step up circuits for LCD driving. The oscillation is available only for the Master operation. When the oscillation signal use for the display clock, connect the CL terminal to V_{SS} . In case of the oscillation circuits do not use, connect the OSC₁ to V_{DD} , OSC₂ to the V_{SS} . The oscillation circuits output divided by 8 and output from CLO terminal as a display clock.

(g) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Follower.

Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the multi-chip or large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable values of the capacitors connecting to the V₁ to V₅ terminals, the step up circuit and the feedback resistors for V₅ operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display pattern. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V₁, V₂, V₃, V₄, and V₅ for the LCD supply from outside, terminals C1⁺, C1⁻, C2⁺, C2⁻, and VR are open. The status of internal power supply can select by T₁ and T₂ terminal. The external power supply can be used together with some of internal power supply function.

Table 3.

(※ Don't Care)

T1	T2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term
L	※	O	O	O	-		
H	L	x	O	O	V _{OUT}	OPEN	
H	H	x	x	O	V ₆ = V _{OUT}	OPEN	OPEN

When (T₁, T₂)=(H, L), the terminal for step up circuits of C1⁺, C1⁻, C2⁺, C2⁻ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T₁, T₂)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from outside due to the Step up circuits and Voltage adjust circuits are stop its operation.


(2) Instruction

The NJU6455 distinguish the signal on the data bus by combination of A0 and R/W(RD,WR). Normally, the busy check is not required as the NJU6455 is operating so first because of the decode of the instruction and execution are performed only depend on the internal timing which not depend on the external clock. In case of serial interface, the data input from D₇ terminal serially.

The Table. 4 shows the instruction codes of the NJU6455.

Table 4. Instruction Code

Instruction		Code												Description
		A0	R	W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD Display ON/OFF 0:OFF 1:ON	
(2)	Display Start Line Set	0	1	0	0	1	Display Start Address						Determine the Display Line Correspond to the COM .	
(3)	Page Address Set	0	1	0	1	0	1	1	Page Address				Set the page of DD RAM to the Page Add. Register	
(4)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.	
(5)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.	
(6)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status	
(7)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM	
(8)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM	
(9)	ADC Select	0	1	0	1	0	1	0	0	0	0	0	Set the DD RAM vs Segment 0:Normal 1:Inverse	
(10)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0	Inverse the On and Off Display 0:Normal 1:Inverse	
(11)	Whole Display On	0	1	0	1	0	1	0	0	1	0	0	Whole Display Turns On 0:Normal 1:Whole Disp. On	
(12)	Icon Display	0	1	0	1	0	1	0	1	0	1	0	Set the Duty Ratio 0:No Icon 1:With Icon	
(13)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading	
(14)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode	
(15)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits	
(16)	Output Assignment Register Set	0	1	0	1	1	0	0	Assignment Data				Set the COM and SEG driver assignment to the Register	
(17)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0	0:Int. Power Supply Off 1:Int. Power Supply On	
(18)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turned on	
(19)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V5 output level to the EVR register	
(20)	Power Save (Dual Command)	0	1	0	1	0	1	0	1	1	1	0	Set the Power save Mode	
		0	1	0	1	0	1	0	0	1	0	1		

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	1	1	D ₀

D₀: Display Off

1: Display On

(b) Display Start Line

This instruction set the line address as shown Fig. 1. The selected line in the Display Data RAM correspond to the COM₀ which display at the top of LCD panel. The display area is set automatically from the selected line to the line which increase the number of duty ratio. Therefore, the smooth scroll for vertical direction by changing the start line address on by one or page switching are available by this instruction.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁

A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
							⋮
1	1	1	1	1	1	0	3E
1	1	1	1	1	1	1	3F

(c) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 8 is a Icon display data area which available only for the D₀.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	1	A ₃	A ₂	A ₁	A ₀

A ₃	A ₂	A ₁	A ₀	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8



(d) Column Address

When MPU access the Display Data RAM, page address set(refer(c) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting. After writing 1page data ,page address setting is required due to page address doesn't increase automatically.

The increment of the column address is stopped by the address of (A0)_H automatically, but the page address is no change even if the column address increase to (A0)_H and stop. In this time the page address is no change.

	A0	$\overline{RD}$	$\overline{WR}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Higher Order	0	1	0	0	0	0	1	A ₇	A ₆	A ₅	A ₄
Lower Order	0	1	0	0	0	0	0	A ₃	A ₂	A ₁	A ₀

A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
1	0	0	1	1	1	1	1	9F

(e) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	$\overline{WR}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.

The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.

0 :Counterclockwise Output(Inverse) Column Address 160-n ↔ Segment Driver n

1 :Clockwise Output (Normal) Column Address n ↔ Segment Driver n

(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.

0 : Whole Display "On"

1 : Whole Display "Off"

(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by RST signal or reset instruction.

0 : —

1 : Initialization Period

(f) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0		WRITE DATA							

(g) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data can not be readout.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0		READ DATA							

(h) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0		1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)

1: Counterclockwise Output (Inverse)

(i) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0		1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"

1: Inverse RAM data "0" correspond to "On"

(j) Whole Display On

This instruction executes the all pixel turns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0		1	0	1	0	0	1	0	D

D 0: Normal Display

1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (s) Power Save) .



(k) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COM1 terminal operate as COM₃₂ and output the icon display data stored in D₀ of Display Data RAM page 8(refer to the Fig. 4). The icon display in the multi-chip operation of NJU6455, both of master and slave chip must be set this instruction.

A0		RD		WR		D ₇ D ₀					
0	1	0	0	1	0	1	0	1	0	1	D

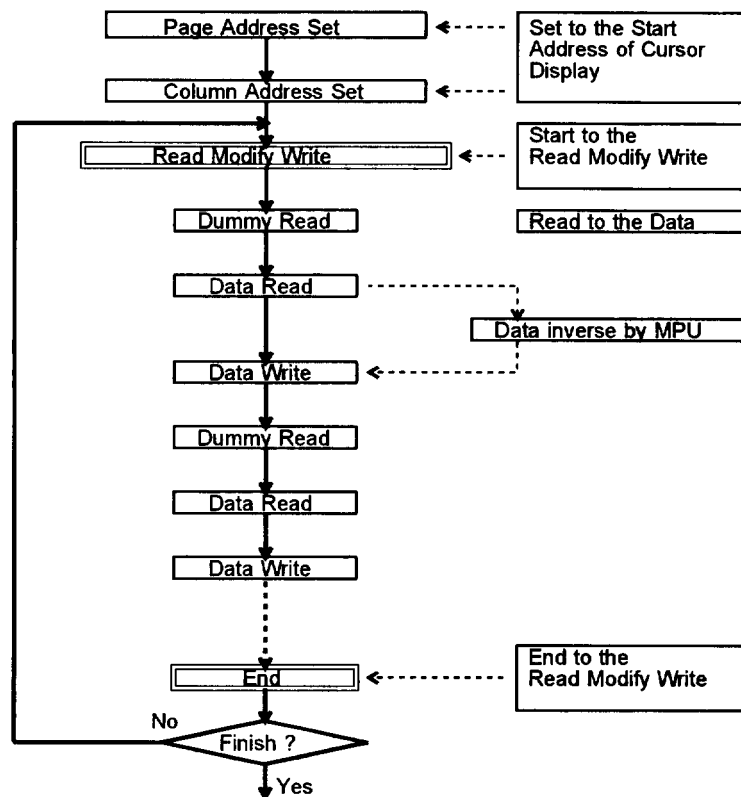
(l) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

A0		RD		WR		D ₇ D ₀					
0	1	0	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

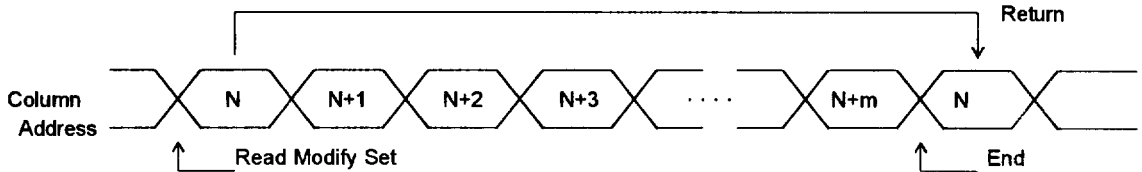
(m) Sequence of inverse display



(n) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇ D ₀							
0	1	0	1	1	1	0	1	1	1	0



(o) Reset

This instruction executes the following initialization.

Initialization

- ① Set the 1st line in the Display Start Line Register.
- ② Set the Address (00)_H to the Column Address Counter.
- ③ Set the page 0 to the Page Register.
- ④ Set the case 4 of Output Assignment
- ⑤ Set (00)_H to the EVR Register for the contrast control

In this time, there are no influence to the Display Data RAM.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇ D ₀							
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{\text{RES}}$ terminal must be required for the initialization when the power turns on. Substitution of Reset Instruction for the reset signal input to the $\overline{\text{RES}}$ terminal is not allowed.

(p) Output Assignment Register

This instruction set the function both of common and segment terminal and its assignment by the A₀ and A₁.

And the bit A₂ set the Common Driver scanning order as explain in "(1-7) Common and Segment Driver Assignment" of Functional Description.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇ D ₀							
0	1	0	1	1	0	0	A ₂	A ₁	A ₀	

A₂: Set the Common Driver scanning order

A ₂	A ₁	A ₀	Status	Number of COM and SEG
*	0	0	Case4	SEG ₁₆₀
*	0	1	Case3	SEG ₁₂₈ , COM ₃₂
*	1	0	Case2	
*	1	1	Case1	

(*:Don't Care)

For more detail, Please refer to the explanation of (1-7) "Common and Segment output assignment."



(q) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

A0	$\overline{\text{RD}}$	$\frac{\text{R/W}}{\text{WR}}$	$\text{D}_7 \text{ } \text{D}_0$							
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off

1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using. In case of the multi-chip application of the NJU6455, external power supply is recommended due to the heavy LCD capacitive load. When the NJU6455 set to the slave chip, the Internal Power Supply should be Off.

(r) LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 ~ V4 and output LCD driving waveform through the COM/SEG terminals.

A0	$\overline{\text{RD}}$	$\frac{\text{R/W}}{\text{WR}}$	$\text{D}_7 \text{ } \text{D}_0$							
0	1	0	1	1	1	0	1	1	0	1

(s) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instruction execute, the internal Electrical Variable Resistor(EVR) to change the V5 output voltage generate one voltage state from 16 voltage state. The range of V5 output level can be adjusted by the external resistance. For more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	$\overline{\text{RD}}$	$\frac{\text{R/W}}{\text{WR}}$	$\text{D}_7 \text{ } \text{D}_0$							
0	1	0	1	0	0	0	A ₃	A ₂	A ₁	A ₀

A ₃	A ₂	A ₁	A ₀	V _{LCD}
0	0	0	0	Low
:	:	:	:	
1	1	1	1	High

$$V_{\text{LCD}} = V_{\text{DD}} - V_5$$

When EVR don't use, set the EVR register to (0, 0, 0, 0).

(t) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mode and the operating current is reduced as same as stand by current. The internal status in the Power Save Mode is as follows;

- ① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
- ② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
- ③ Stop the external clock input. Then the terminal OSC₂ becomes floating status.
- ④ Keeping the display data and operating mode as before the power save mode.
- ⑤ All of LCD driving bias voltage fixed to the V_{DD} level.

*1 Power save mode requires dual-instruction. After the second instruction "whole Display ON", the power save mode starts.

*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.

*3 Until "LCD driving voltage set" execution, NJU6455 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.

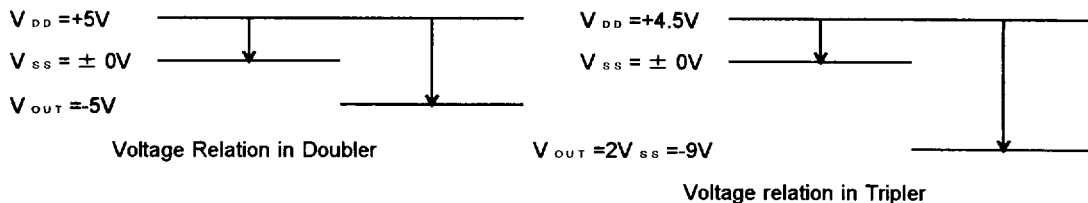
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.

*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage (V_{DD} common) of the voltage $V_{DD} - V_{SS}$ is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT} . In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT} , then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_S through the voltage adjust circuits. The output voltage of V_S is adjusted by changing the R_a and R_b within the range of $|V_S| < |V_{OUT}|$. The output voltage can be calculated by the following formula.

$$V_S = V_{DD} - (1 + R_b/R_a) \cdot V_{REG} \quad \text{..... ①}$$

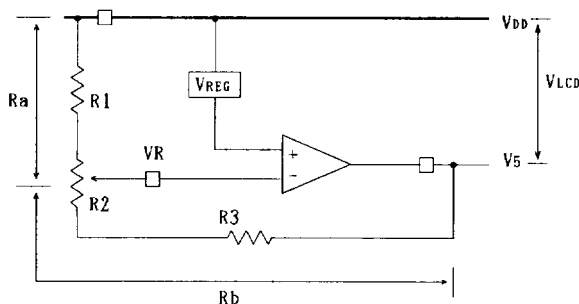


Fig. 3

Where, the V_{REG} is a constant voltage in the NJU6455 like as $V_{REG} \approx 2.5$.

To adjust the output voltage from V_S , connect the variable resistance among VR , V_{DD} and V_S as shown in Fig. 3. When fine tuning for V_S is needed, combine with the fixed resistance of $R1$, $R3$ and variable resistance of $R2$ is recommended as shown in Fig. 3.

Design example for $R1$, $R2$ and $R3$

- $R1 + R2 + R3 = 5M \Omega$ (Determined by the current flown between $V_{DD} - V_S$)
- Variable voltage range by the $R2$. $-2.5 \sim -4.5V$ ($V_{DD} - V_S \rightarrow 7V \sim 9V$)
(Determined by the LCD electrical characteristics)

$R1$, $R2$ and $R3$ are calculated by above conditions and the formula of ① to mentioned below; (reference)

$$R1 = 1.388M \Omega$$

$$R2 = 0.388M \Omega$$

$$R3 = 3.214M \Omega$$

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.

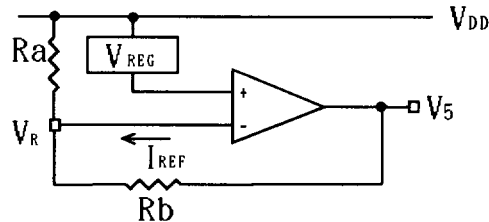
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_s which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 4 bits data into the EVR resistor and determine the one output voltage status out of 16 prefixed voltage status.

When execute the EVR function, set the T1 and T2 except the "H, H" and execute the Internal Power Supply On instruction.

[External parts constants setting example when EVR function using / reference]



(1) Determine the V_s voltage range controlled by EVR.

LCD Driving Voltage $V_{DD} - V_s$ 7 ~ 9V

The range of V_s 2V

(2) Determine the R_b .

$R_b = [\text{The range of } V_s] / I_{REF}$ (16 status $I_{REF} \approx 2.5 \mu A$ constant current)

$R_b = 2V / 2.5 \mu A = 0.8M \Omega$ *Ta=25 °C $V_{DD} - V_{OUT} = 9V$

(3) Adjust the R_a

$$R_a = \frac{V_{REG}}{([LCD \text{ Driving Voltage}] - V_{REG}) / R_b}$$

$$R_a = \frac{2.5 V}{(7V - 2.5V) / 0.8M \Omega} = 0.44M \Omega$$

(4) Adjust the R_a

Adjust the R_a to good contrast of LCD display after the (D_3, D_2, D_1, D_0) of EVR register set to (1, 0, 0, 0) or (0, 1, 1, 1). When the EVR using, R_a use a variable resistance and contrast adjustment mentioned in (4) for each chip is required due to the I_{REF} is simple constant current source.

When the EVR function does not use, the (D_3, D_2, D_1, D_0) of EVR register set to (0, 0, 0, 0) by the RES signal or the EVR Register Set instruction.

(d) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_5 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 4, five capacitor are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitor C_2 determine by combine with the actual LCD panel.

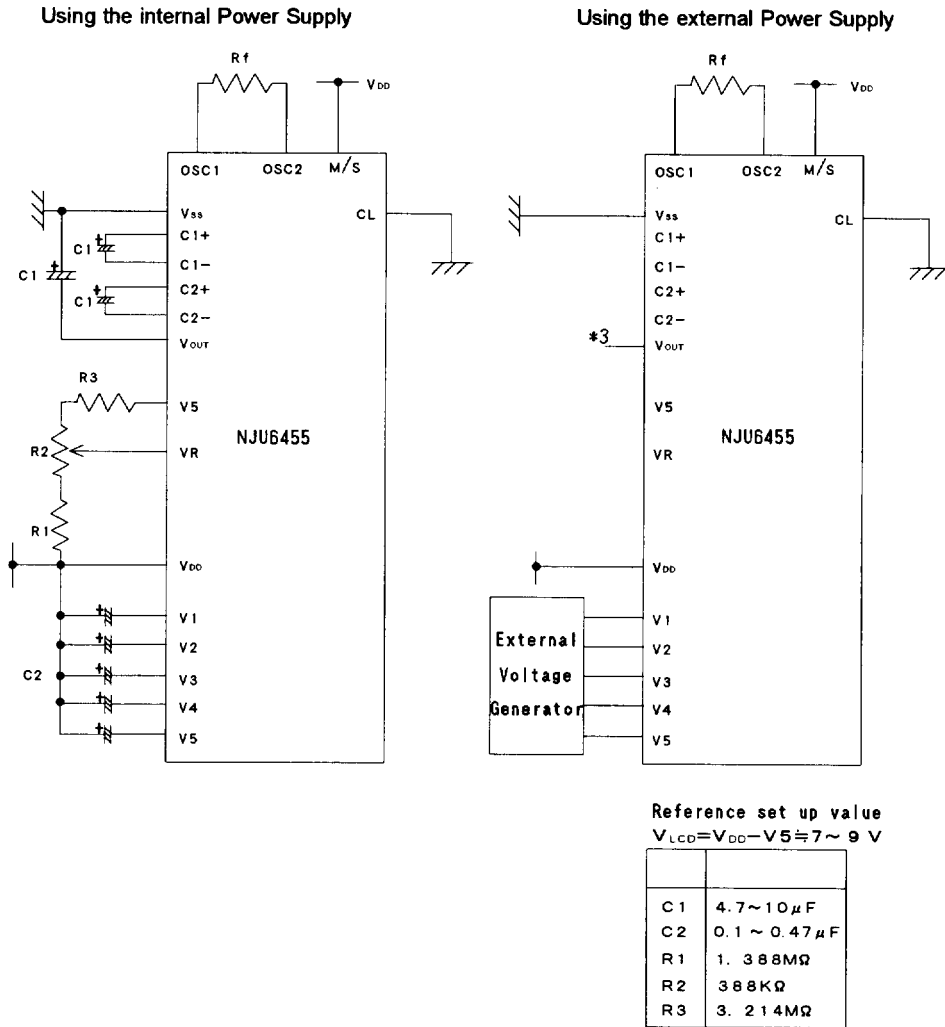


Fig. 4

- *1 To avoid the malfunction, use a short wiring for the feed back resistance R_f of oscillation circuits.
- *2 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.
- *3 Following connection of V_{OUT} is required when external power supply using.
 - When $V_{SS} > V_5$ -- $V_{OUT} = V_5$
 - When $V_{SS} \leq V_5$ -- $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6455 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out is impossible.

Table 5

P/S	Type	$\overline{CS1}$	CS2	A0	RD	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS1}$	CS2	A0	RD	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS1}$	CS2	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6455 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in table 6.

Table 6

C86	Type	$\overline{CS1}$	CS2	0	RD	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS1}$	CS2	0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS1}$	CS2	0	RD	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6455 discriminate the signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$, $\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	RD	WR	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to $\overline{CS1}$ ="L" and CS2="H", and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7 to D_0 . and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

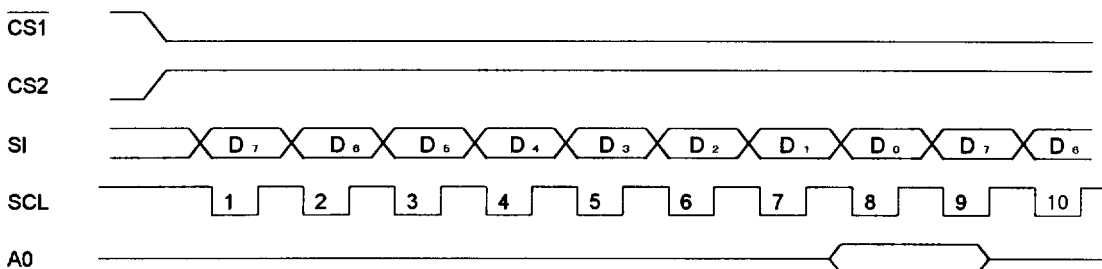


Fig. 5

(5-5) Access to the Display Data RAM and Internal Register.

The NJU6455 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

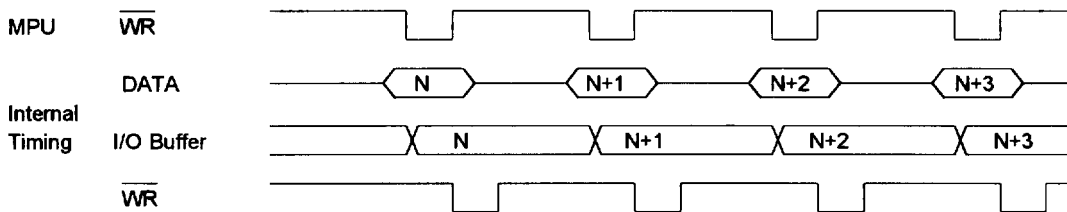
For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at next data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6455 is available because of the limitation of a access time of NJU6455 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting.

Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

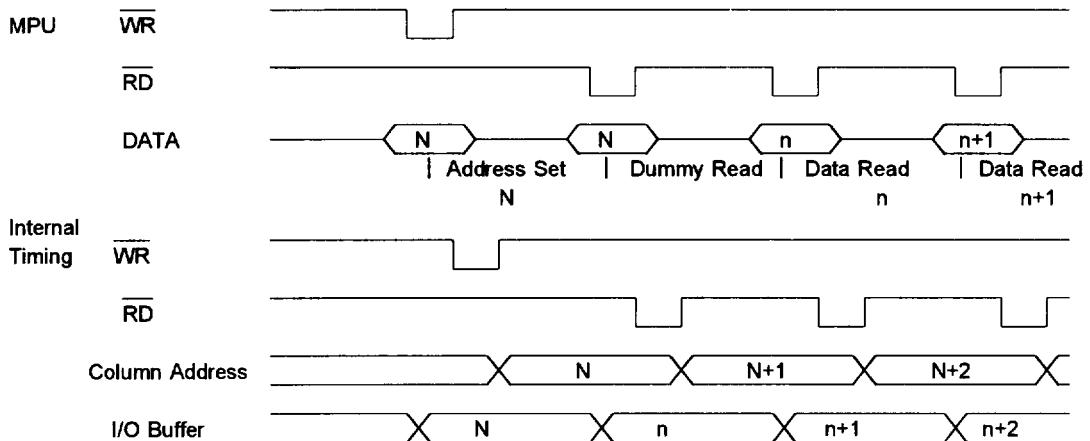


Fig.6

(5-6) Chip Select

CS1, CS2 are Chip Select terminals. The Chip Select is executed by the setting of $\overline{CS1}$ ="L" and $CS2$ ="H". Only the select mode, the interface with MPU is available. In the non select period, the $D_0 \sim D_7$ are high impedance and A_0 , $\overline{RD}$, $\overline{WR}$, SI and SCL input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of $CS1$ and $CS2$.

ABSOLUTE MAXIMUM RATINGS

(Ta=25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V _{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler)	V
Supply Voltage (2)	V _S	V _{DD} -13.5 ~ V _{DD} +0.3	V
Supply Voltage (3)	V ₁ ~ V ₄	V _S ~ V _{DD} +0.3	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Operating Temperature	T _{opr}	- 30 ~ + 80	°C
Storage Temperature	T _{stg}	- 55 ~ + 125(Chip) - 55 ~ + 100(TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V_S ; V_{DD} > V_{SS} ≥ V_{OUT} must be maintained.

Note 4) Decoupling capacitor should be connected between VDD and VSS due to the stabilized operation for voltage converter.

ELECTRICAL CHARACTERISTICS (1)

(V_{DD} =5V ± 10%, V_{SS} =0V, Ta=-20 ~ +75 °C)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V _{DD}		4.5	5.0	5.5	V	5
	Available			2.4		5.5		
Operating Voltage(2)	Recommend	V _S		V _{DD} -13.5		V _{DD} -3.5	V	
	Available			V _{DD} -13.5				
	Available	V ₁ , V ₂	V _{LCD} =V _{DD} -V _S	V _{DD} -0.6xV _{LCD}		V _{DD}		
	Available	V ₃ , V ₄		V _S		V _{DD} -0.4xV _{LCD}		
Input Voltage	1	V _{IHC1}	A0...D ₇ ~ D ₇ , RD,WR,CS ₁ , CS ₂ ,CL,FR, M/S,RES,C86 SI,SCL,P/S Terminals	0.7xV _{DD}		V _{DD}	V	
		V _{IHC2}		V _{DD} =2.7V	0.8xV _{DD}	V _{DD}		
	2	V _{ILC1}		V _{SS}		0.3xV _{DD}		
		V _{ILC2}		V _{DD} =2.7V	V _{SS}	0.2xV _{DD}		
Output Voltage	1	V _{OHC11}	D ₀ ~ D ₇ , FR CLO,DYO Terminals	I _{OH} =-1mA	0.8xV _{DD}	V _{DD}	V	
		V _{OHC12}		I _{OH} =-120uA V _{DD} =2.7V	0.8xV _{DD}	V _{DD}		
		V _{OHC21}	OSC ₂ Terminal	I _{OH} =-0.5mA	0.8xV _{DD}	V _{DD}		
		V _{OHC22}		I _{OH} =-50uA V _{DD} =2.7V	0.8xV _{DD}	V _{DD}		
	2	V _{OLC11}	D ₀ ~ D ₇ , FR CLO,DYO Terminals	I _{OL} = 1mA	V _{SS}	0.2xV _{DD}		
		V _{OLC12}		I _{OL} = 120uA V _{DD} =2.7V	V _{SS}	0.2xV _{DD}		
		V _{OLC21}	OSC ₂ Terminal	I _{OL} = 0.5mA	V _{SS}	0.2xV _{DD}		
		V _{OLC22}		I _{OL} = 50uA V _{DD} =2.7V	V _{SS}	0.2xV _{DD}		

5

ELECTRICAL CHARACTERISTICS (2)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Input Leakage Current		I_{LI}	$\overline{AO}, \overline{RD}, \overline{WR}, \overline{CS_1}, \overline{CS_2}, \overline{CL}, M/S, RES, C86, SI, SCL, P/S, T1, T2$ Terminals	-1.0		1.0	μA	6
		I_{LO}	$D_0 \sim D_7, FR$ Terminals	-3.0		3.0		
Driver On-resistance		R_{ON1}	$T_a = 25^\circ C$ $V_{LCD} = 13.5V$		2.0	3.0	$k\Omega$	7
		R_{ON2}			3.0	4.5		
Stand-by Current		I_{DD0}	$M/S = V_{SS}, OSC_2 = FR = V_{DD}$		0.05	5.0	μA	8
Operating Current		I_{DD11}	Display $V_{LCD} = 8.0V$ $f_{CL} = 4kHz$		13	20	μA	9
		I_{DD12}		$R_f = 1M\Omega$	28	45		10
		I_{DD13}	Display $V_{LCD} = 8.0V$ $V_{DD} = 2.7V$ $f_{CL} = 4kHz$		12	18		9
		I_{DD14}		$R_f = 1M\Omega$	16	25		10
		I_{DD21}	Accessing $f_{cyc} = 200kHz$ $V_{DD} = 2.7V$		350	500		11
		I_{DD22}			170	240		11
Input Terminal Capacitance		C_{IN}	$T_a = 25^\circ C, \overline{AO}, \overline{RD}, \overline{WR}, \overline{CS_1}, \overline{CS_2}, \overline{CL}, M/S, RES, C86, SI, SCL, P/S, T1, T2, D_1$ to D_7		10		pF	
Oscillation Frequency		f_{osc}	$R_f = 1M\Omega \pm 2\%$ $T_a = 25^\circ C$ $V_{DD} = 5.0V$	15	18	21	kHz	
			$V_{DD} = 2.7V$	11	16	21		
Voltage Tripler	Input Voltage	V_{DD1}	$V_{DD} - V_{SS}$	2.4		5.5	V	12
		V_{DD2}	$V_{DD} - V_{SS}$, used Tripler	2.4		4.5		
	Output Volt.	V_{OUT}	$V_{SS} - V_{LCD}$, used Tripler	-9.0			V	
	On-resistance	R_{TRI}	$V_{DD} = 3V; C = 4.7\mu F$ used Tripler		650	1000	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"	$V_{DD} - 13.5$		$V_{DD} - 5.0$	V	13
	Voltage Follower	V_S	Voltage Adjustment Circuit "OFF"	$V_{DD} - 13.5$		$V_{DD} - 5.0$	V	13
	Operating Current	I_{OUT1}	$V_{DD} = 4.5V, V_{LCD} = 8V$		58	2.0	mA	14
		I_{OUT2}	COM/SEG Term.Open, No Access		23	1.0		
		I_{OUT3}	Display check. pattern		21	0.8		
	Voltage Reg.	V_{REG}	$V_{DD} - V_{OUT} = 9V; T_a = 25^\circ C$	T.B.D	2.5	T.B.D	V	15
	Reference Current	I_{REF}	$V_{DD} - V_{OUT} = 9V; T_a = 25^\circ C$	T.B.D	2.5	T.B.D	μA	

Note 5) NJU6455 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 and FR terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,10,11,14) Apply to current after "LCD Driving Voltage Set".

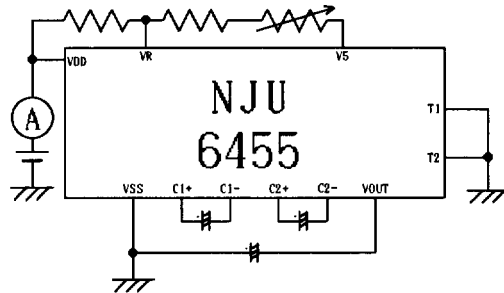
- Note 9) Apply to the external display clock operation in no access from the MPU and no use inter-nal power supply circuits.
- Note 10) Apply to the internal CR oscillator operation in no access from the MPU and no use inter-nal power supply circuits.
- Note 11) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DDIX} .
- Note 12) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.
- Note 13) LCD driving voltage V_S can be adjusted within the voltage follower operating range.
- Note 14) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T1	T2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT} , V_S)

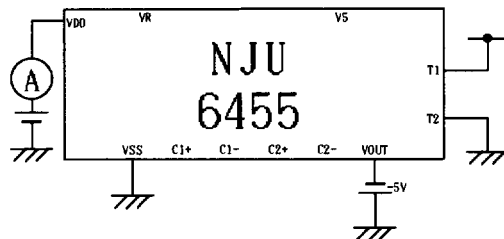
* = Don't Care

Note 15) Apply to the precision of Voltage on each EVR steps.

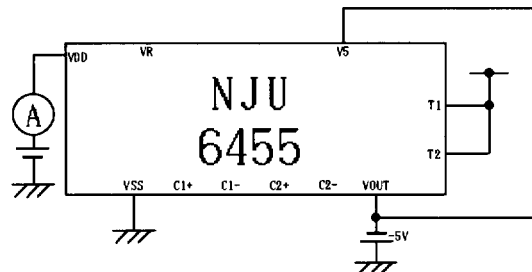
MEASUREMENT BLOCK DIAGRAM : I_{OUT1}



: I_{OUT2}



: I_{OUT3}



ELECTRICAL CHARACTERISTICS (3)

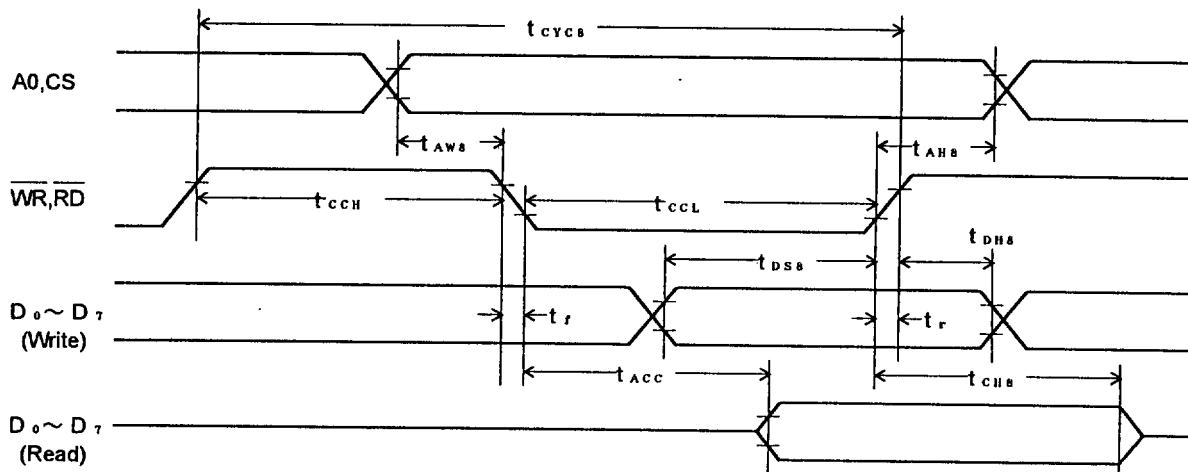
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	RES Terminal	1.0			us	16
Reset "L" Level Pulse Width	t_{RW}		10			us	17

Note 16) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.

Note 17) Specified minimum pulse width of RES signal. Over than t_{RW} "L" input should be required for correct reset operation.

BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)


 $(V_{DD} = 5.0V \pm 10\%, T_a = -20 \sim 75^\circ C)$

PARAMETER	SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	$A0, \overline{CS}_1, \overline{CS}_2$	t_{AHB}	10		
Address Set Up Time	Terminals	t_{AWB}	10		
System Cycle Time		t_{CYCB}	180		
Control	$\overline{WR}, \overline{RD}$	$t_{CCL}(W)$	25		
Pulse Width	Terminals	$t_{CCL}(R)$	80		
	"H"	t_{CCH}	70		
Data Set Up Time	$D_0 \sim D_7$	t_{DSB}	60		
Data Hold Time	Terminals	t_{DHB}	10		
RD Access Time		t_{ACCB}	70		
Output Disable Time		t_{OHB}	30	CL=100pF	
Rise Time, Fall Time	$\overline{CS}_1, \overline{CS}_2, \overline{WR}, \overline{RD}, A0, D_0 \sim D_7$	t_r, t_f	15		ns

 $(V_{DD} = 2.7V \sim 4.5V, T_a = -20 \sim 75^\circ C)$

PARAMETER	SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	$A0, \overline{CS}_1, \overline{CS}_2$	t_{AHB}	25		
Address Set Up Time	Terminals	t_{AWB}	25		
System Cycle Time		t_{CYCB}	450		
Control	$\overline{WR}, \overline{RD}$	$t_{CCL}(W)$	50		
Pulse Width	Terminals	$t_{CCL}(R)$	200		
	"H"	t_{CCH}	220		
Data Set Up Time	$D_0 \sim D_7$	t_{DSB}	120		
Data Hold Time	Terminals	t_{DHB}	35		
RD Access Time		t_{ACCB}	140		
Output Disable Time		t_{OHB}	35	CL=100pF	
Rise Time, Fall Time	$\overline{CS}_1, \overline{CS}_2, \overline{WR}, \overline{RD}, A0, D_0 \sim D_7$	t_r, t_f	15		ns

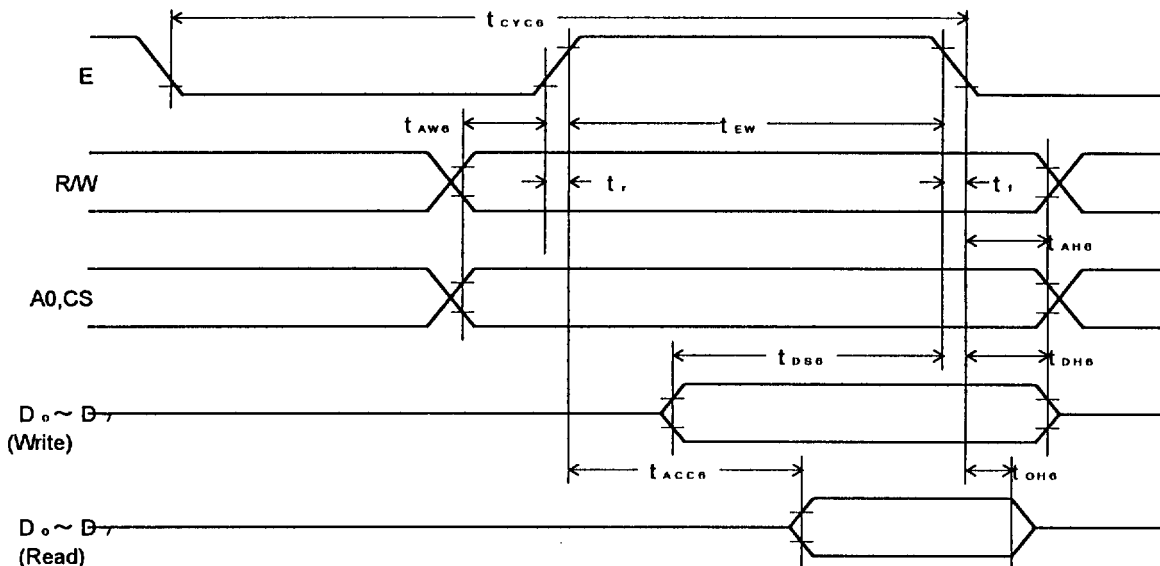
Note 18) Rise time(t_r) and fall time(t_f)

of input signal should be less than 15ns.

Note 19) Each timing is specified bas

ed on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Read/Write operation sequence (68 Type MPU)


 $(V_{DD} = 5.0V \pm 10\%, T_a = -20 \sim 75^\circ C)$

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS ₁ , CS ₂ ,	t _{AH0}	10			ns
Address Set Up Time	R/W	t _{AW0}	10			
System Cycle Time	Terminals	t _{CVCS}	180			
Enable	E Terminal	t _{EW}	100			
Pulse Width			25			
Data Set Up Time	D ₀ ~D ₇ ,	t _{DS0}	60		CL=100pF	
Data Hold Time		t _{DH0}	20			
Access Time	Terminals	t _{ACC0}		70		
Output Disable Time		t _{OH0}	0	25		
Rise Time, Fall Time	A0, CS ₁ , CS ₂ , R/W, E, D ₀ ~D ₇ , Terminals	t _r , t _f		15		

 $(V_{DD} = 2.7V \sim 4.5V, T_a = -20 \sim 75^\circ C)$

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS ₁ , CS ₂ ,	t _{AH0}	25			ns
Address Set Up Time	R/W	t _{AW0}	25			
System Cycle Time	Terminals	t _{CVCS}	450			
Enable	E Terminal	t _{EW}	200			
Pulse Width			50			
Data Set Up Time	D ₀ ~D ₇ ,	t _{DS0}	120		CL=100pF	
Data Hold Time		t _{DH0}	40			
Access Time	Terminals	t _{ACC0}		140		
Output Disable Time		t _{OH0}	0	45		
Rise Time, Fall Time	A0, CS ₁ , CS ₂ , R/W, E, D ₀ ~D ₇ , Terminals	t _r , t _f		15		

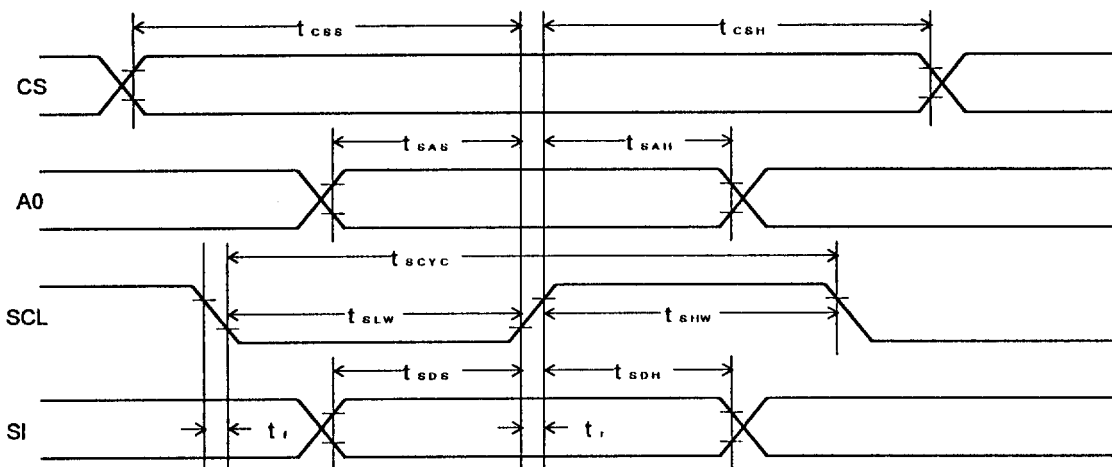
Note 20) t_{CVCS} indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.

Note 21) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 22) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.



• Read/Write operation sequence (Serial Interface)



($V_{DD} = 5.0V \pm 10\%$, $T_a = -20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle		t_{SCYC}	500			
SCL "H" pulse width	SCL Terminal	t_{SHW}	150			
SCL "L" pulse width	SCL Terminal	t_{SLW}	150			
Address Set Up Time	A0 Terminal	t_{SAS}	120			
Address Hold Time	A0 Terminal	t_{SAH}	200			
Data Set Up Time	SI Terminal	t_{SDS}	120			
Data hold Time	SI Terminal	t_{SDH}	50			
CS-SCL Time	$\overline{CS}_1, \overline{CS}_2$ Terminals	t_{CSS}	30			
		t_{CSH}	400			
Rise Time, Fall Time	SCL, A0, $\overline{CS}_1$, $\overline{CS}_2$, SI, Terminals	t_r, t_f		15		ns

5

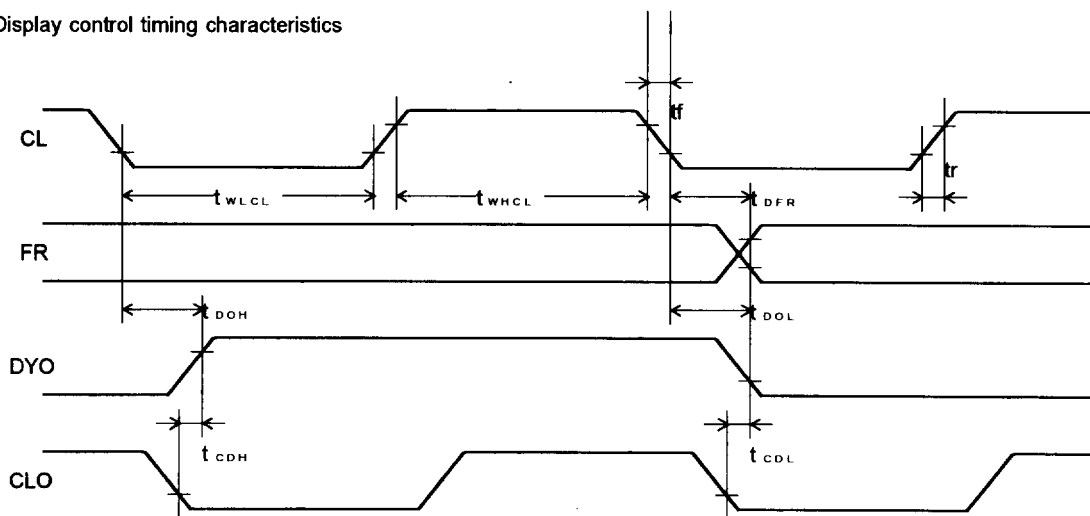
($V_{DD} = 2.7V \sim 4.5V$, $T_a = -20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle		t_{SCYC}	1000			
SCL "H" pulse width	SCL Terminal	t_{SHW}	300			
SCL "L" pulse width	SCL Terminal	t_{SLW}	300			
Address Set Up Time	A0 Terminal	t_{SAS}	250			
Address Hold Time	A0 Terminal	t_{SAH}	400			
Data Set Up Time	SI Terminal	t_{SDS}	250			
Data hold Time	SI Terminal	t_{SDH}	100			
CS-SCL Time	$\overline{CS}_1, \overline{CS}_2$ Terminals	t_{CSS}	60			
		t_{CSH}	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS}_1$, $\overline{CS}_2$, SI, Terminals	t_r, t_f		15		ns

Note 23) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 24) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Display control timing characteristics



Input Timing

($V_{DD} = 5.0V \pm 10\%$, $T_a = -20 \sim 75^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
"L" level Pulse Width	t_{WLCL}	35				μs
"H" level Pulse Width	t_{WHCL}	35				
Rise Time	t_r		30			ns
Fall Time	t_f		30			
FR Delay Time	t_{DFR}	-1.0		1.0		μs

($V_{DD} = 2.7V \sim 4.5V$, $T_a = -20 \sim 75^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
"L" level Pulse Width	t_{WLCL}	35				μs
"H" level Pulse Width	t_{WHCL}	35				
Rise Time	t_r		40			ns
Fall Time	t_f		40			
FR Delay Time	t_{DFR}	-1.0		1.0		μs

Output Timing

($V_{DD} = 5.0V \pm 10\%$, $T_a = -20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
FR Delay Time	FR Terminal	t _{DFR}		60	150	CL=50pF	ns
DY0 "H" Delay Time	DY0 Terminal	t _{DOH}		70	160		
DY0 "L" Delay Time		t _{DOL}		70	160		
CLO-DY0 "H" Delay Time	CLO Terminal	t _{CDH}		40	100	Note 26	
CLO-DY0 "L" Delay Time		t _{CDL}		40	100		

($V_{DD} = 2.7V \sim 4.5V$, $T_a = -20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
FR Delay Time	FR Terminal	t _{DFR}		120	240	CL=50pF	ns
DY0 "H" Delay Time	DY0 Terminal	t _{DOH}		140	250	Note 26	
DY0 "L" Delay Time		t _{DOL}		140	250		
CLO-DY0 "H" Delay Time	CLO Terminal	t _{CDH}		100	200		
CLO-DY0 "L" Delay Time		t _{CDL}		100	200		

Note 25) The FR Delay Time of input timing is applied to the slave operation.

The FR Delay Time of output timing is applied to the master operation.

Note 26) The CLO "H,L" Delay Time are applied to the master operation only.

Note 27) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

■ LCD DRIVING WAVEFORM

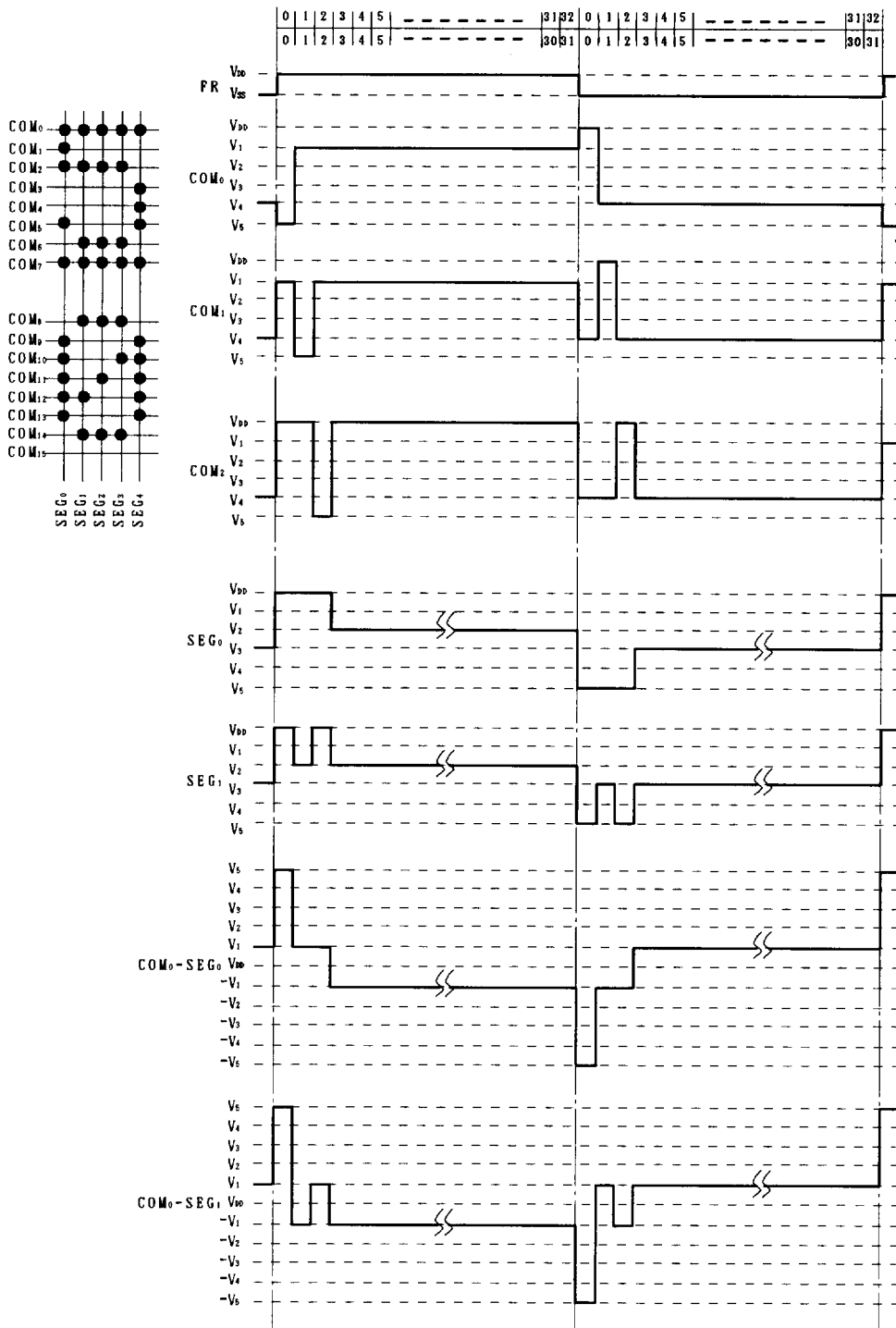


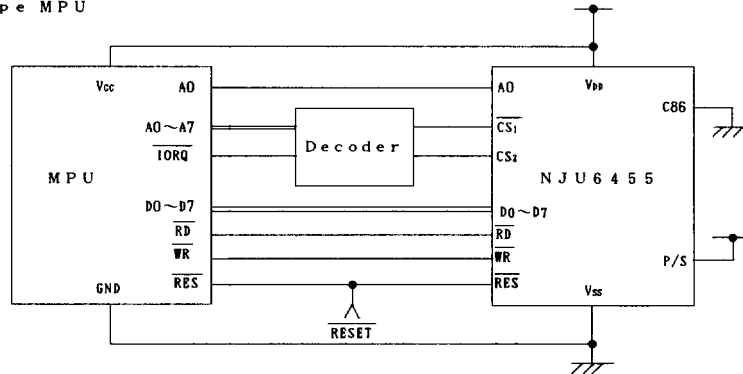
Fig.7

■ APPLICATION CIRCUIT

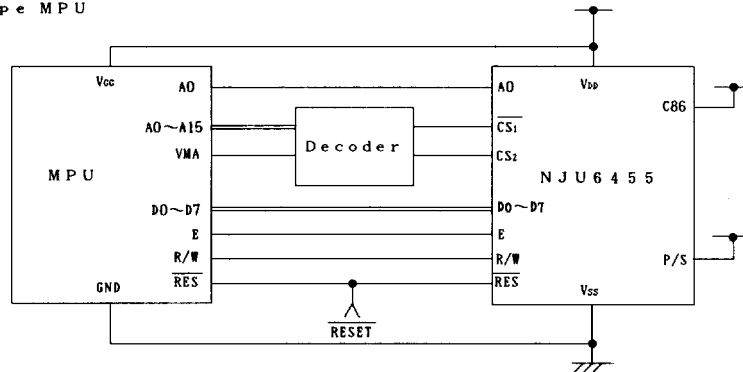
(1) Microprocessor Interface Examples

The NJU6455 can interface both of 80 type and 68 type MPU by the serial format directly. Therefore minimum wiring for the MPU interface is available. In case of multi-chip application, these can connect with MPU respectively and select the each chip by the chip select signal.

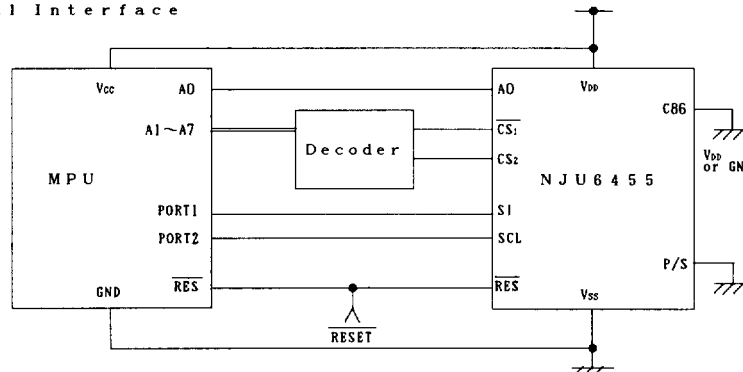
● 80 Type MPU



● 68 Type MPU



● Serial Interface

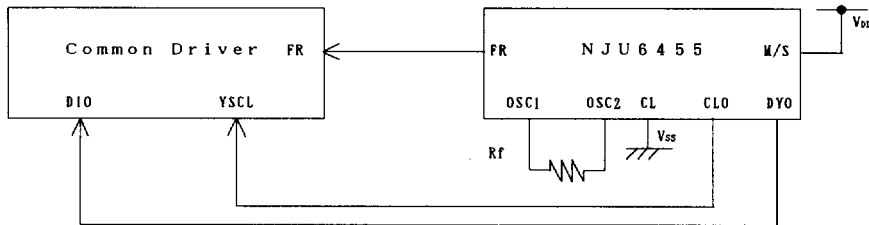




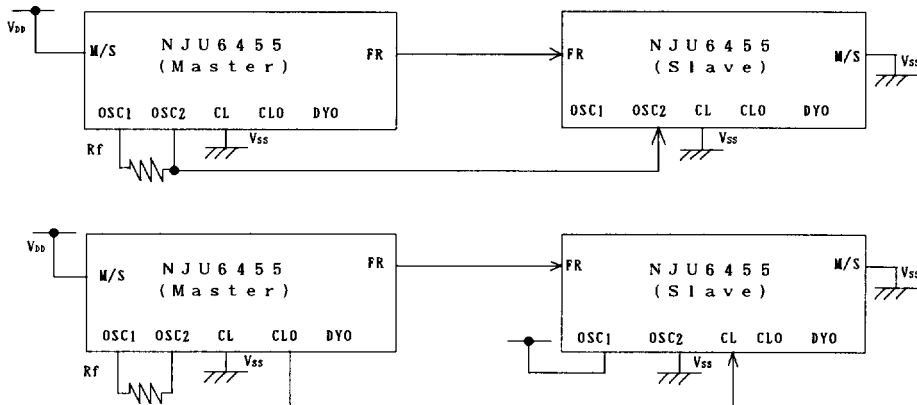
(2) Connection between LCD Drivers

By the multi-chip application, NJU6455 can expand total display capacity. And common exclusive driver also can connect with the NJU6455

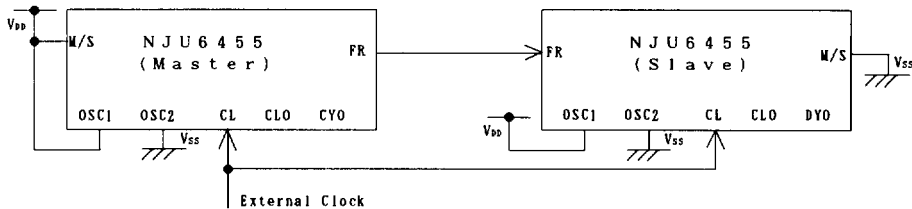
● NJU6455 - Common Driver



● NJU6455 - NJU6455 (Using OSC Circuit)



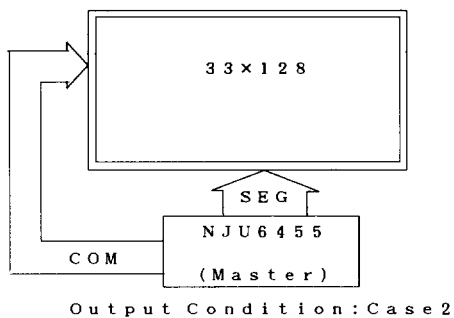
● NJU6455 - NJU6455 (External Clock)



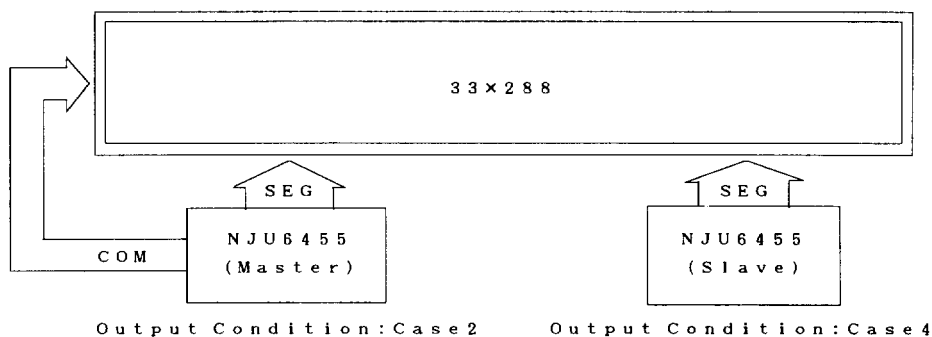


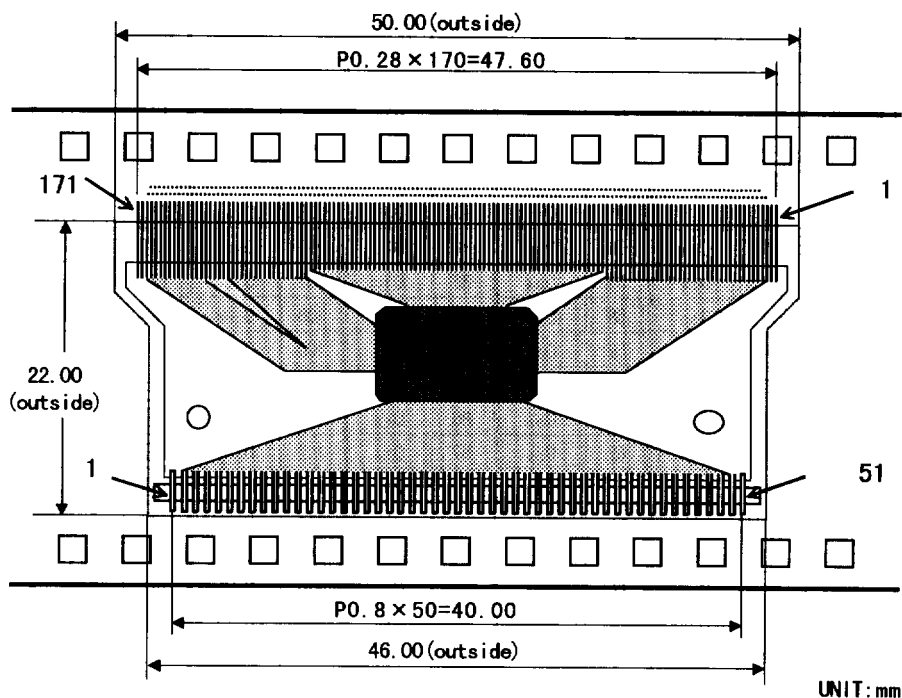
(3)LCD Panel Interface Examples

●1 Chip Construction



●2 Chip Construction



■ PACKAGE INFORMATION (NJU6455H01)

5
■ SPECIFICATION

Name	Material	Thickness
Base Film	UPILEX	$75 \pm 8 \mu\text{m}$
Adhesive	Epoxi type	$19 \pm 4 \mu\text{m}$
Conductor Layer	Electrolysis Copper Foil	$35 \pm 5 \mu\text{m}$
Plating	Sn	$0.3 \pm 0.1 \mu\text{m}$
Resist	Epoxi type	$20 \pm 15 \mu\text{m}$
Sealing Material	Epoxi type	—
Bump	Au (Gold)	—
Thickness of TCP		0.8mm (Max)

■ PIN CONFIGURATION (NJU6455H01)

OUTPUT TERMINALS

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	DUMMY	26	O ₂₃	51	O ₄₈	76	O ₇₃	101	O ₉₈	126	O ₁₂₃	151	DUMMY
2	DUMMY	27	O ₂₄	52	O ₄₉	77	O ₇₄	102	O ₉₉	127	O ₁₂₄	152	DUMMY
3	O ₀	28	O ₂₅	53	O ₅₀	78	O ₇₅	103	O ₁₀₀	128	O ₁₂₅	153	O ₁₄₄
4	O ₁	29	O ₂₆	54	O ₅₁	79	O ₇₆	104	O ₁₀₁	129	O ₁₂₆	154	O ₁₄₅
5	O ₂	30	O ₂₇	55	O ₅₂	80	O ₇₇	105	O ₁₀₂	130	O ₁₂₇	155	O ₁₄₆
6	O ₃	31	O ₂₈	56	O ₅₃	81	O ₇₈	106	O ₁₀₃	131	O ₁₂₈	156	O ₁₄₇
7	O ₄	32	O ₂₉	57	O ₅₄	82	O ₇₉	107	O ₁₀₄	132	O ₁₂₉	157	O ₁₄₈
8	O ₅	33	O ₃₀	58	O ₅₅	83	O ₈₀	108	O ₁₀₅	133	O ₁₃₀	158	O ₁₄₉
9	O ₆	34	O ₃₁	59	O ₅₆	84	O ₈₁	109	O ₁₀₆	134	O ₁₃₁	159	O ₁₅₀
10	O ₇	35	O ₃₂	60	O ₅₇	85	O ₈₂	110	O ₁₀₇	135	O ₁₃₂	160	O ₁₅₁
11	O ₈	36	O ₃₃	61	O ₅₈	86	O ₈₃	111	O ₁₀₈	136	O ₁₃₃	161	O ₁₅₂
12	O ₉	37	O ₃₄	62	O ₅₉	87	O ₈₄	112	O ₁₀₉	137	O ₁₃₄	162	O ₁₅₃
13	O ₁₀	38	O ₃₅	63	O ₆₀	88	O ₈₅	113	O ₁₁₀	138	O ₁₃₅	163	O ₁₅₄
14	O ₁₁	39	O ₃₆	64	O ₆₁	89	O ₈₆	114	O ₁₁₁	139	O ₁₃₆	164	O ₁₅₅
15	O ₁₂	40	O ₃₇	65	O ₆₂	90	O ₈₇	115	O ₁₁₂	140	O ₁₃₇	165	O ₁₅₆
16	O ₁₃	41	O ₃₈	66	O ₆₃	91	O ₈₈	116	O ₁₁₃	141	O ₁₃₈	166	O ₁₅₇
17	O ₁₄	42	O ₃₉	67	O ₆₄	92	O ₈₉	117	O ₁₁₄	142	O ₁₃₉	167	O ₁₅₈
18	O ₁₅	43	O ₄₀	68	O ₆₅	93	O ₉₀	118	O ₁₁₅	143	O ₁₄₀	168	O ₁₅₉
19	O ₁₆	44	O ₄₁	69	O ₆₆	94	O ₉₁	119	O ₁₁₆	144	O ₁₄₁	169	COM1
20	O ₁₇	45	O ₄₂	70	O ₆₇	95	O ₉₂	120	O ₁₁₇	145	O ₁₄₂	170	DUMMY
21	O ₁₈	46	O ₄₃	71	O ₆₈	96	O ₉₃	121	O ₁₁₈	146	O ₁₄₃	171	DUMMY
22	O ₁₉	47	O ₄₄	72	O ₆₉	97	O ₉₄	122	O ₁₁₉	147	DUMMY		
23	O ₂₀	48	O ₄₅	73	O ₇₀	98	O ₉₅	123	O ₁₂₀	148	DUMMY		
24	O ₂₁	49	O ₄₆	74	O ₇₁	99	O ₉₆	124	O ₁₂₁	149	DUMMY		
25	O ₂₂	50	O ₄₇	75	O ₇₂	100	O ₉₇	125	O ₁₂₂	150	DUMMY		

INPUT TERMINALS

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	DUMMY	11	SI	21	D ₁	31	FR	41	C2 ⁻	51	DUMMY		
2	V ₅	12	P/S	22	D ₂	32	CL	42	V _{OUT}				
3	V ₄	13	CS ₁	23	D ₃	33	OSC ₂	43	V ₅				
4	V ₃	14	CS ₂	24	D ₄	34	OSC ₁	44	VR				
5	V ₂	15	C86	25	D ₅	35	T ₂	45	V _{DD}				
6	V ₁	16	AQ	26	D ₆	36	T ₁	46	V ₁				
7	V _{DD}	17	WR	27	D ₇	37	V _{SS}	47	V ₂				
8	M/S	18	RD	28	DY0	38	C1 ⁺	48	V ₃				
9	RES	19	V _{SS}	29	CL0	39	C1 ⁻	49	V ₄				
10	SCL	20	D ₀	30	DUMMY	40	C2 ⁺	50	V ₅				