

NLAS325

Dual SPST Analog Switch, Low Voltage, Single Supply

The NLAS325 is a dual SPST (Single Pole, Single Throw) switch, similar to 1/2 a standard 4066. The device permits the independent selection of 2 analog/digital signals. Available in the Ultra-Small 8 package.

The use of advanced 0.6 μ CMOS process, improves the R_{ON} resistance considerably compared to older higher voltage technologies.

- On Resistance is 20 Ω Typical at 5.0 V
- Matching is < 1 Ω Between Sections
- 2 – 6 V Operating Range
- Ultra Low < 5 pC Charge Injection
- Ultra Low Leakage < 1 nA at 5.0 V, 25 C
- Wide Bandwidth > 200 MHz, –3 dB
- CMOS/TTL Compatible
- 2000 V ESD (HBM)
- Ron Flatness $\pm 6 \Omega$ at 5.0 V
- US8 Package
- Independent Enables; One Positive, One Negative

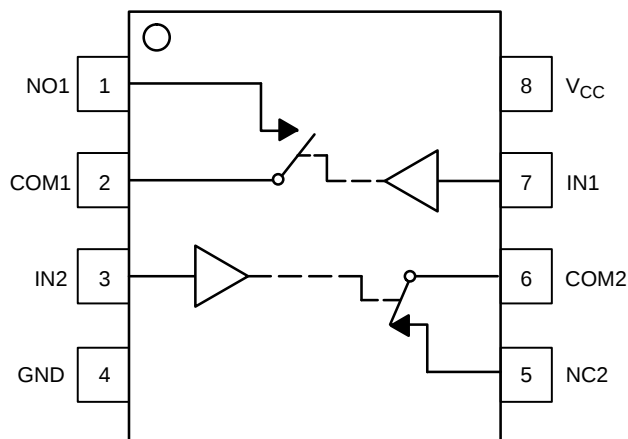


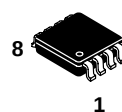
Figure 1. Pinout



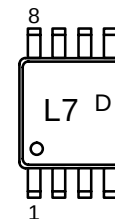
ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAM



US8
US SUFFIX
CASE 493



L7 = Device Code
D = Date Code

PIN ASSIGNMENT

1	NO1
2	COM1
3	IN2
4	GND
5	NC2
6	COM2
7	IN1
8	VCC

FUNCTION TABLE

On/Off Enable Input	Analog Switch 1	Analog Switch 2
L	Off	On
H	On	Off

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _I	DC Input Voltage	− 0.5 to + 7.0	V
V _O	DC Output Voltage	− 0.5 to + 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	− 50	mA
I _{OK}	DC Output Diode Current V _O < GND	− 50	mA
I _O	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Ground Pin	± 100	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance (Note 1)	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	Digital Select Input Voltage	GND	5.5	V
V _{IS}	Analog Input Voltage (NC, NO, COM)	GND	V _{CC}	V
T _A	Operating Temperature Range	− 55	+ 125	°C
t _r , t _f	Input Rise or Fall Time, SELECT V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

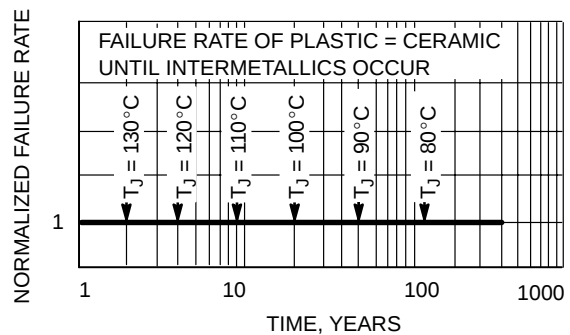


Figure 2. Failure Rate vs. Time Junction Temperature

NLAS325

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				– 55°C to 25°C	< 85°C	< 125°C	
V _{IH}	Minimum High-Level Input Voltage, Select Inputs		2.0	1.5	1.5	1.5	V
			2.5	1.9	1.9	1.9	
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V _{IL}	Maximum Low-Level Input Voltage, Select Inputs		2.0	0.5	0.5	0.5	V
			2.5	0.6	0.6	0.6	
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I _{IN}	Maximum Input Leakage Current, Select Inputs	V _{IN} = 5.5 V or GND	0 V to 5.5 V	± 0.2	± 2.0	± 2.0	μA
I _{CC}	Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	5.5	4.0	4.0	8.0	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				– 55°C to 25°C	< 85°C	< 125°C	
R _{ON}	Maximum “ON” Resistance (Figures 16 – 22)	V _{IN} = V _{IL} or V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 10.0 mA	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
R _{FLAT (ON)}	ON Resistance Flatness (Figures 16 – 22)	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{IS} = 1 V, 2 V, 3.5 V	4.5	4	4	5	Ω
I _{NC(OFF)} I _{NO(OFF)}	NO or NC Off Leakage Current (Figure 8)	V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 1.0 V _{COM} 4.5 V	5.5	1	10	100	nA
I _{COM(ON)}	COM ON Leakage Current (Figure 8)	V _{IN} = V _{IL} or V _{IH} V _{NO} 1.0 V or 4.5 V with V _{NC} floating or V _{NO} 1.0 V or 4.5 V with V _{NO} floating V _{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V _{CC} (V)	V _{IS} (V)	Guaranteed Maximum Limit						Unit	
					−55°C to 25°C			< 85°C		< 125°C		
					Min	Typ*	Max	Min	Max	Min		Max
t _{ON}	Turn-On Time (Figures 11 and 12)	R _L = 300 Ω, C _L = 35 pF (Figures 4 and 5)	2.5	2.0	5	23	35	5	38	5	41	ns
			3.0	2.0	5	16	24	5	27	5	30	
			4.5	3.0	2	11	16	2	19	2	22	
			5.5	3.0	2	9	14	2	17	2	20	
t _{OFF}	Turn-Off Time (Figures 11 and 12)	R _L = 300 Ω, C _L = 35 pF (Figures 4 and 5)	2.5	2.0	1	7	12	1	15	1	18	ns
			3.0	2.0	1	5	10	1	13	1	16	
			4.5	3.0	1	4	6	1	9	1	12	
			5.5	3.0	1	3	5	1	8	1	11	
t _{BBM}	Minimum Break-Before-Make Time	V _{IS} = 3.0 V (Figure 3) R _L = 300 Ω, C _L = 35 pF	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		

*Typical Characteristics are at 25°C.

		Typical @ 25, V _{CC} = 5.0 V	pF
C _{IN}	Maximum Input Capacitance, Select Input	8	
C _{NO} or C _{NC}	Analog I/O (switch off)	10	
C _{COM}	Common I/O (switch off)	10	
C _(ON)	Feedthrough (switch on)	20	

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V_{CC} V	Typical	Unit
				25°C	
BW	Maximum On-Channel –3dB Bandwidth or Minimum Frequency Response (Figure 10)	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 6)	3.0	145	MHz
			4.5	170	
			5.5	175	
V_{ONL}	Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 6)	3.0	–2	dB
			4.5	–2	
			5.5	–2	
V_{ISO}	Off-Channel Isolation (Figure 9)	$f = 100$ kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 6)	3.0	–93	dB
			4.5	–93	
			5.5	–93	
Q	Charge Injection Select Input to Common I/O (Figure 14)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0 \Omega$, $C_L = 1000$ pF $Q = C_L * \Delta V_{OUT}$ (Figure 7)	3.0	1.5	pC
			5.5	3.0	
THD	Total Harmonic Distortion THD + Noise (Figure 13)	$F_{IS} = 20$ Hz to 100 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 5.0$ V _{PP} sine wave	5.5	0.1	%
VCT	Channel-to-Channel Crosstalk	$f = 100$ kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 6)	5.5	–90	dB
			3.0	–90	

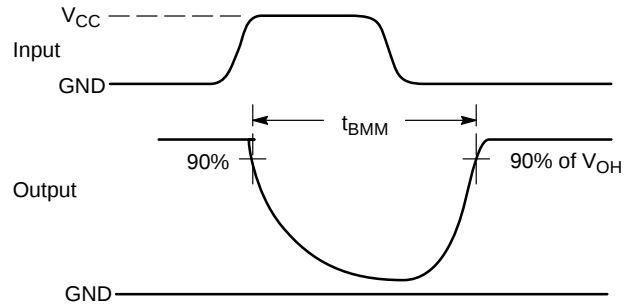
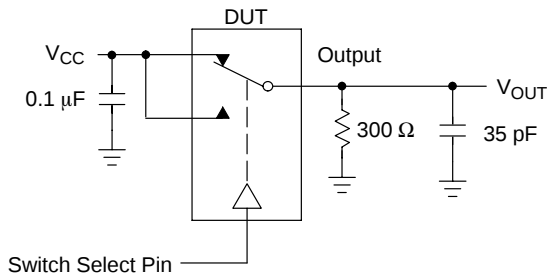


Figure 3. t_{BMM} (Time Break-Before-Make)

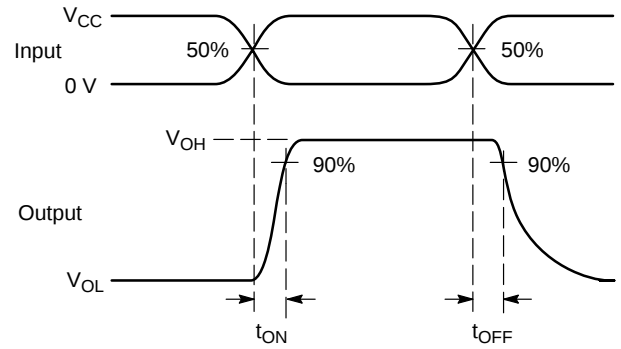
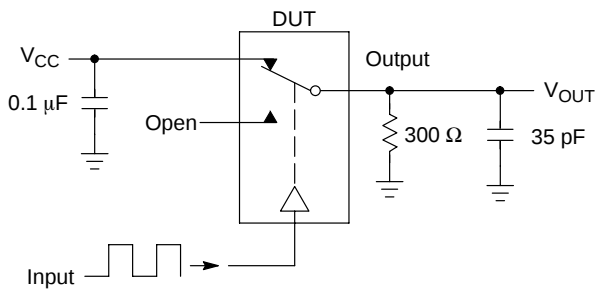


Figure 4. t_{ON}/t_{OFF}

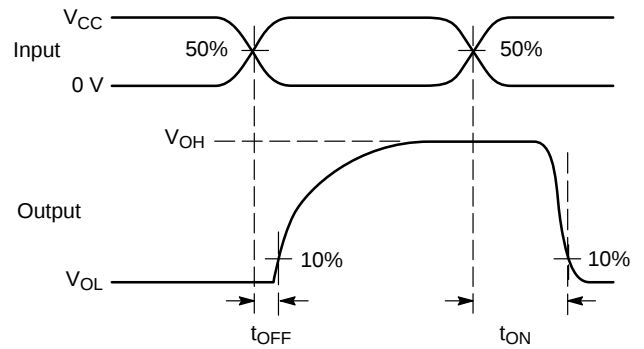
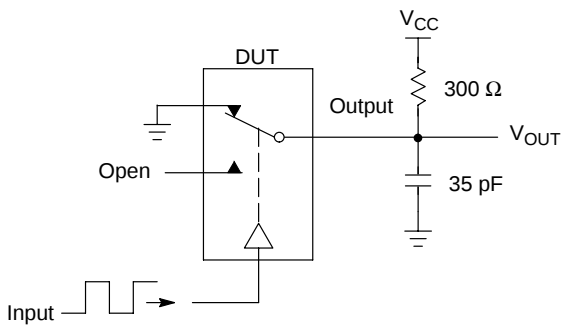
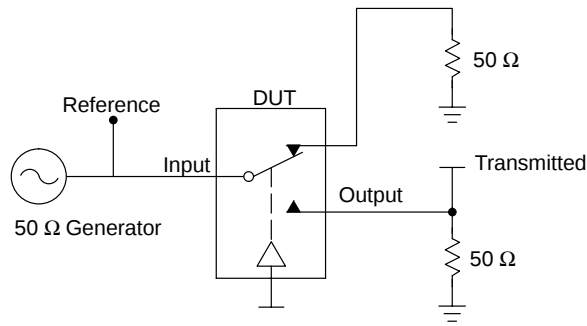


Figure 5. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

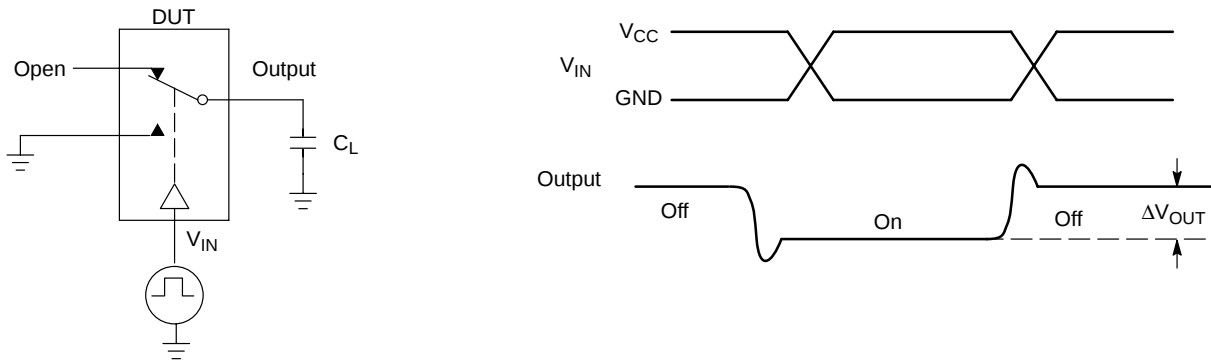


Figure 7. Charge Injection: (Q)

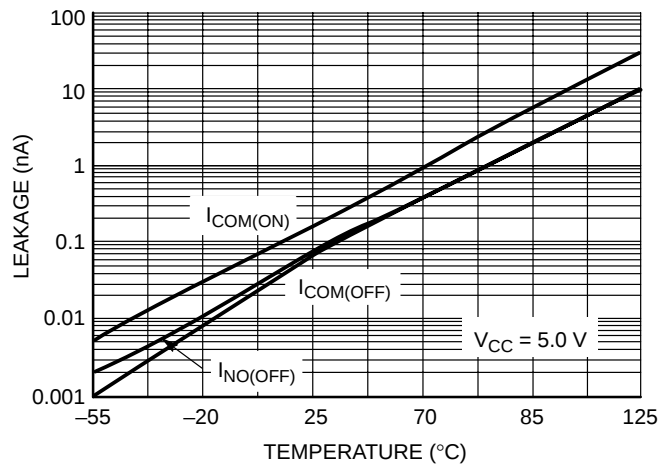


Figure 8. Switch Leakage vs. Temperature

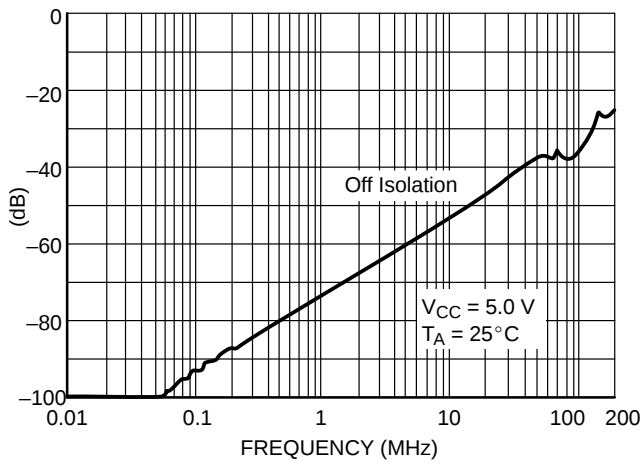


Figure 9. Off-Channel Isolation

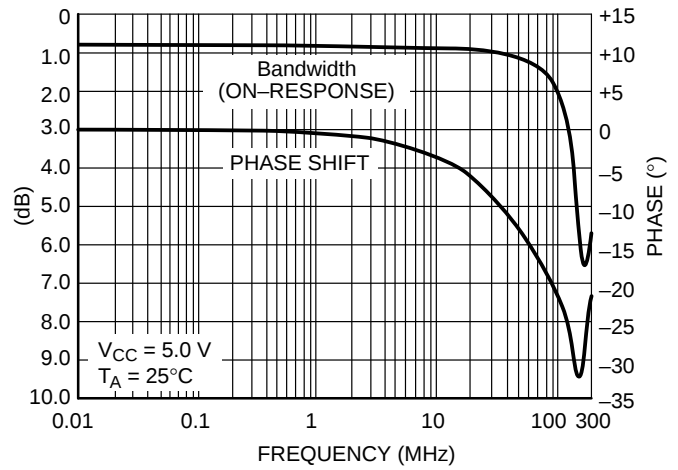


Figure 10. Typical Bandwidth and Phase Shift

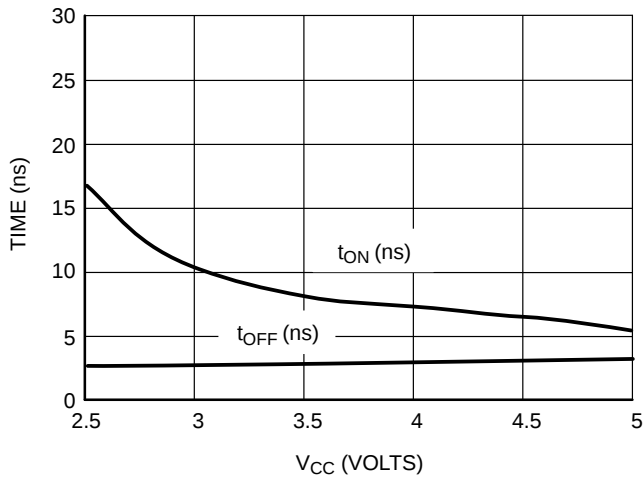


Figure 11. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

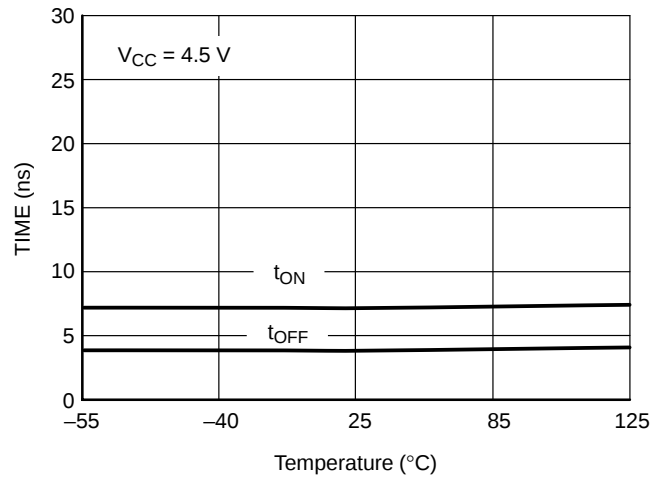


Figure 12. t_{ON} and t_{OFF} vs. Temp

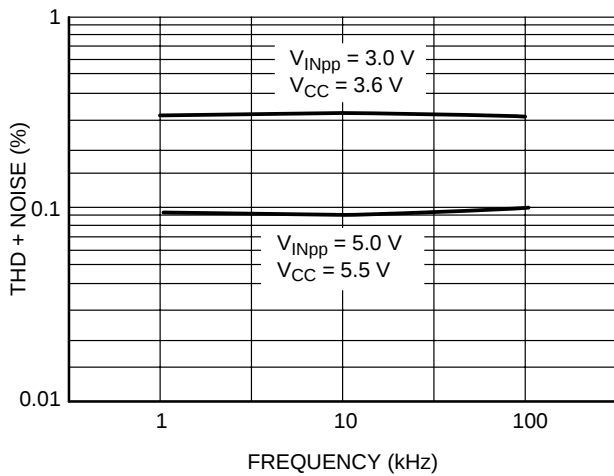


Figure 13. Total Harmonic Distortion Plus Noise vs. Frequency

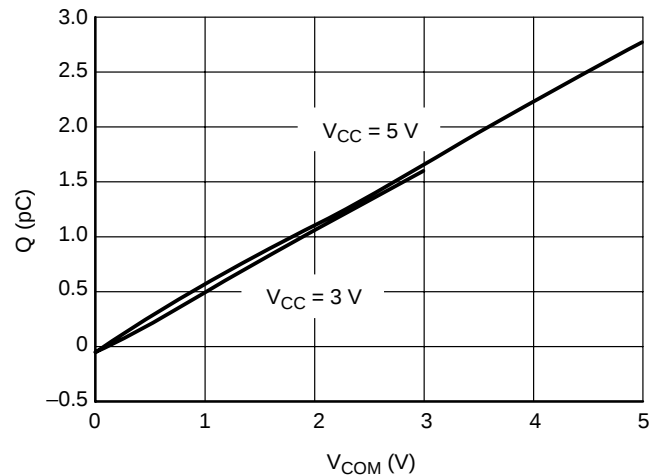


Figure 14. Charge Injection vs. COM Voltage

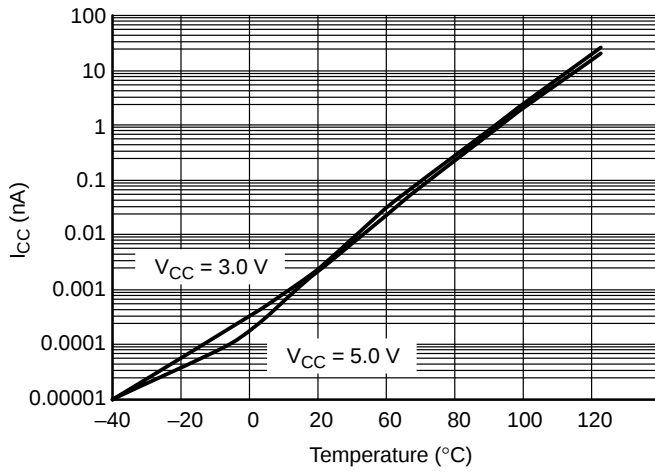


Figure 15. I_{CC} vs. Temp, $V_{CC} = 3\text{ V}$ & 5 V

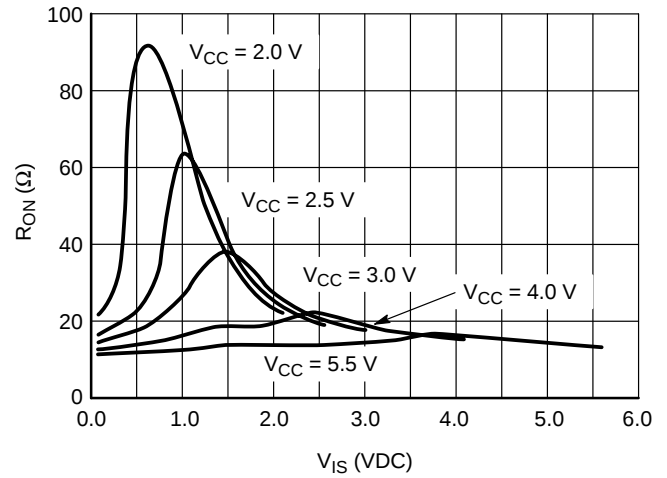


Figure 16. R_{ON} vs. V_{CC} , Temp = 25°C

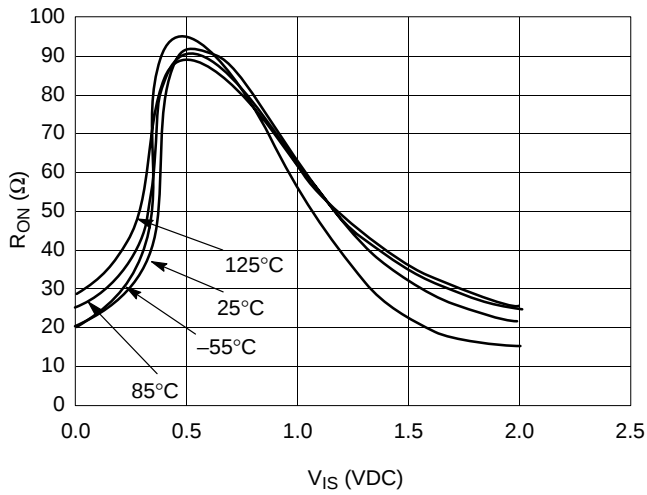


Figure 17. R_{ON} vs. Temp, $V_{CC} = 2.0\text{ V}$

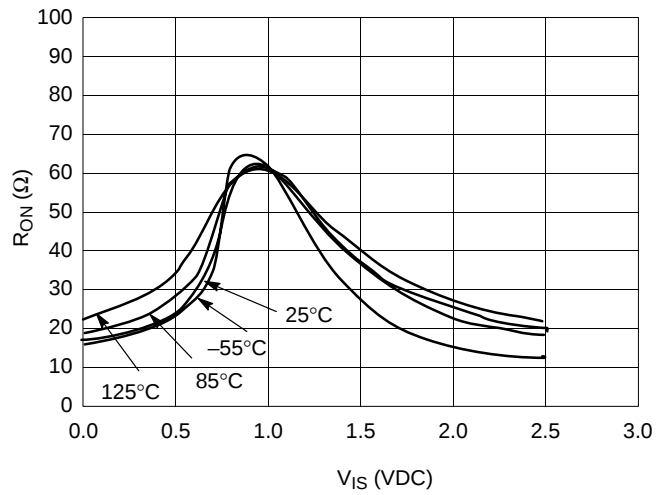


Figure 18. R_{ON} vs. Temp, $V_{CC} = 2.5\text{ V}$

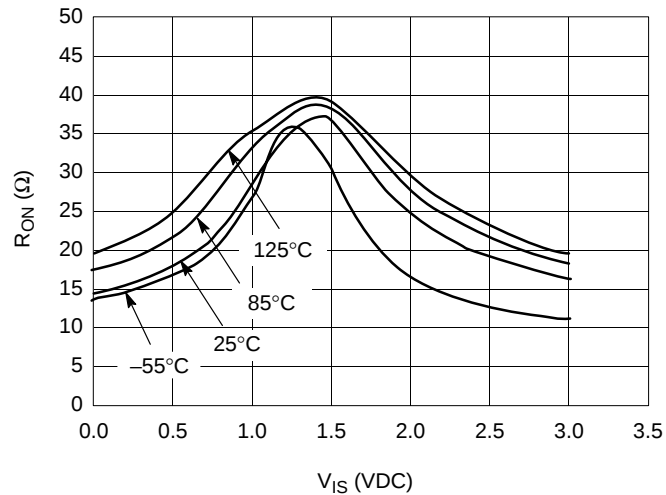


Figure 19. R_{ON} vs. Temp, $V_{CC} = 3.0\text{ V}$

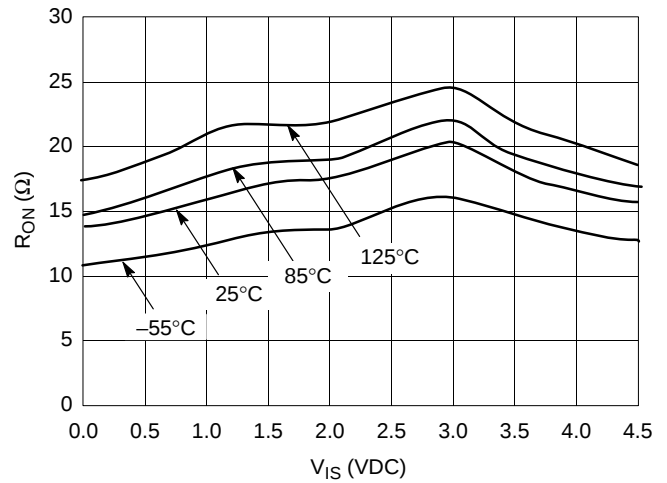


Figure 20. R_{ON} vs. Temp, $V_{CC} = 4.5\text{ V}$

NLAS325

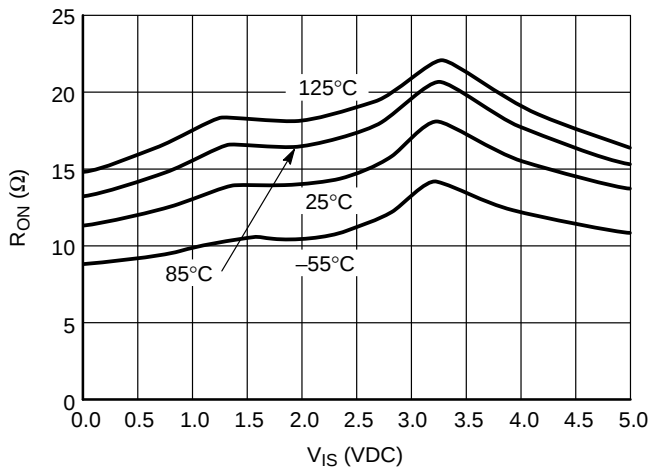


Figure 21. R_{ON} vs. Temp, $V_{CC} = 5.0$ V

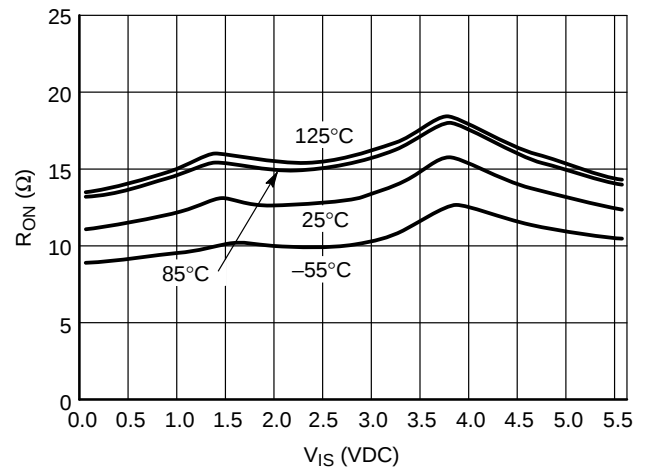


Figure 22. R_{ON} vs. Temp, $V_{CC} = 5.5$ V

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature				Package Type	Tape and Reel Size
	Circuit Indicator	Technology	Device Function	Package Suffix		
NLAS325US	NL	AS	325	US	US8	178 mm (7") 3000 Unit

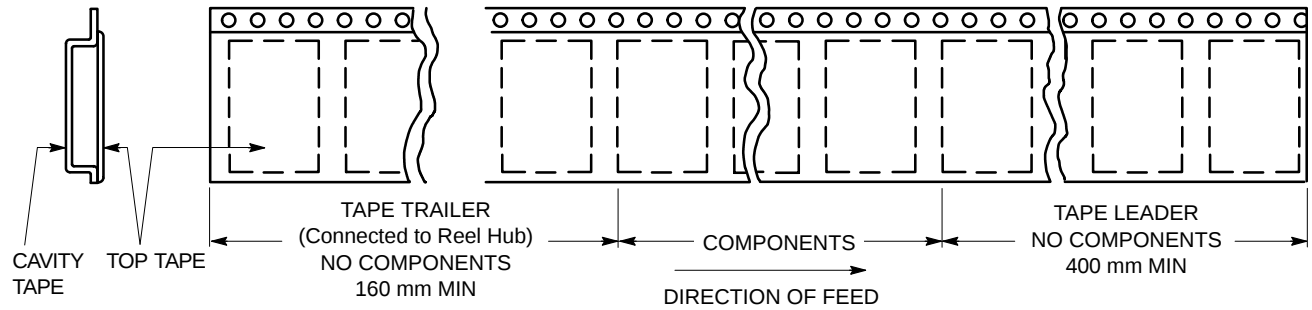


Figure 23. Tape Ends for Finished Goods

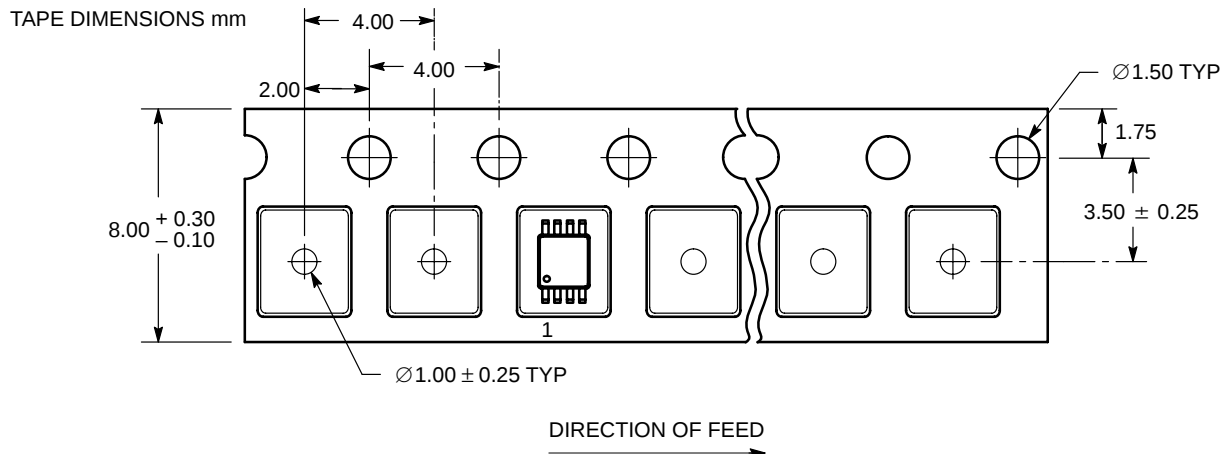


Figure 24. US8 Reel Configuration/Orientation

NLAS325

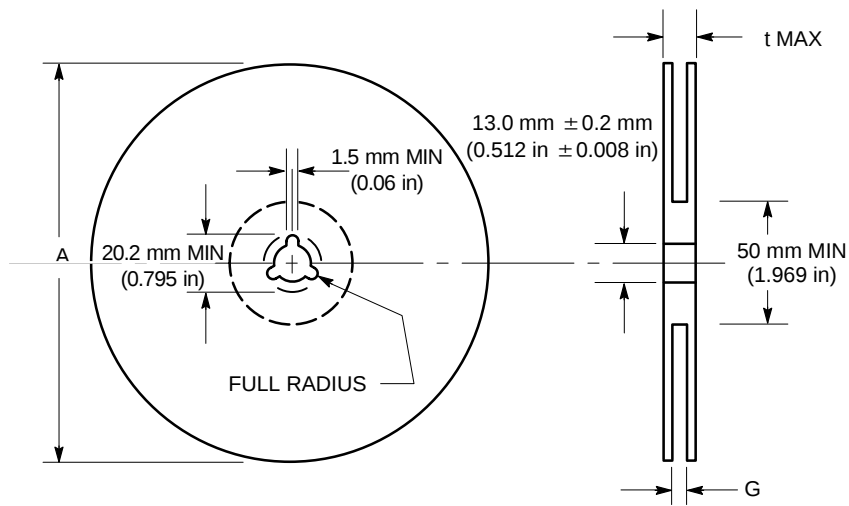


Figure 25. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

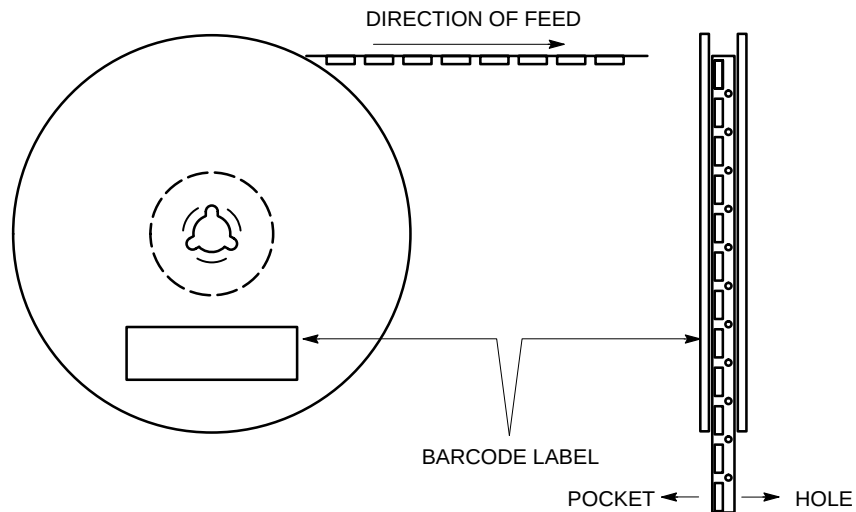
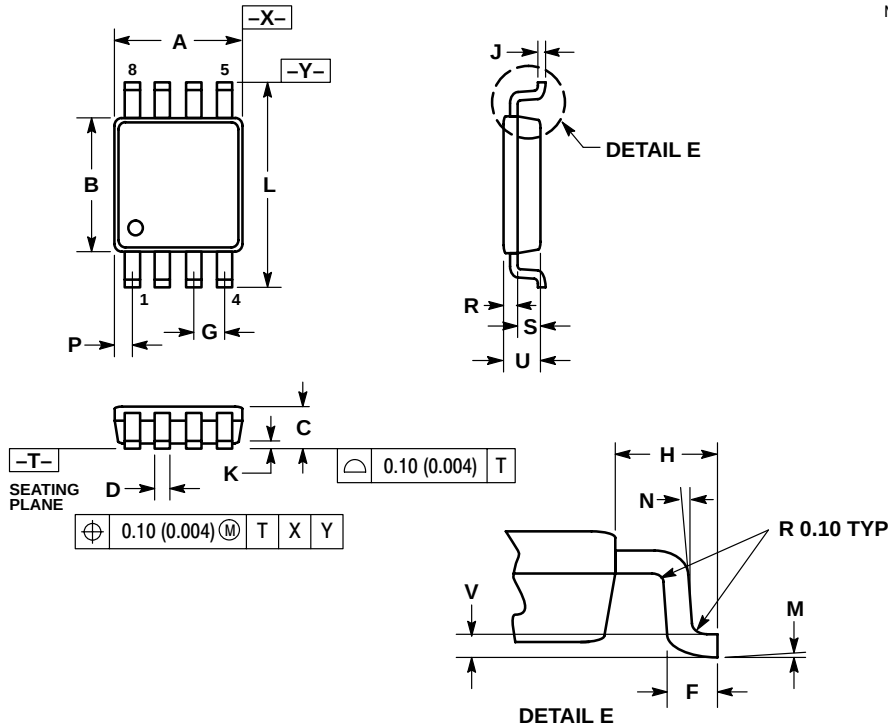


Figure 26. Reel Winding Direction

NLAS325

PACKAGE DIMENSIONS

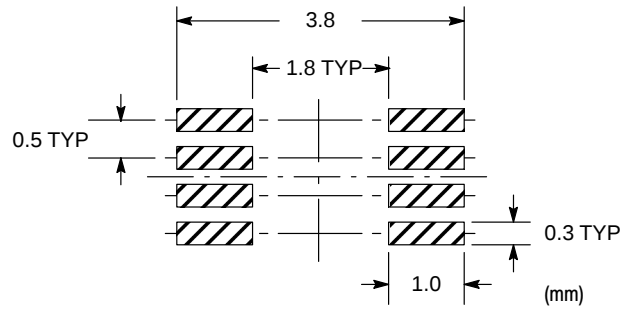
US8
US SUFFIX
CASE 493-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 INCH).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0°	6°	0°	6°
N	5°	10°	5°	10°
P	0.28	0.44	0.011	0.017
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.