### **NTQS6466**

## **Product Preview**

# **Power MOSFET** 6.8 Amps, 20 Volts

### N-Channel TSSOP-8

#### **Features**

- New Low Profile TSSOP–8 Package
- Ultra Low R<sub>DS(on)</sub>
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- IDSS and VDS(on) Specified at Elevated Temperatures

#### **Applications**

- Power Management in Portable and Battery-Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones
- Lithium Ion Battery Applications
- Note Book PC

### **MAXIMUM RATINGS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	10 secs	Steady State	Unit
Drain-to-Source Voltage	VDS	20		Vdc
Gate-to-Source Voltage	VGS	12		
Continuous Drain Current  - T <sub>J</sub> = 150°C (Note 1.)  - T <sub>A</sub> = 25°C	ΙD	8.1	6.8	Adc
− T <sub>A</sub> = 70°C		6.6	5.4	
Pulsed Drain Current (10 μs Pulse Width)	IDM	±30		Apk
Continuous Source Current (Diode Conduction) (Note 1.)	IS	1.35	0.95	Adc
Maximum Power Dissipation (Note 1.)  - T <sub>A</sub> = 25°C  - T <sub>A</sub> = 70°C	P <sub>D</sub>	1.5 1.0	1.05 0.67	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150		°C
Single Pulse Drain-to-source Avalanche Energy – Starting TJ= 25°C (VDD = 50 V, IL = 7.7 Apk, L = 44 mH)	EAS	1.:	36	J

<sup>1.</sup> Surface mounted to 1" x 1" FR-4 board.

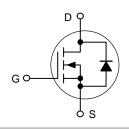


### ON Semiconductor

http://onsemi.com

### 6.8 AMPERES 20 VOLTS RDS(on) = 17 m $\Omega$

#### N-Channel

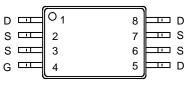


#### **MARKING DIAGRAM**



= Year WW = Work Week = MOSFET

#### **PIN ASSIGNMENT**



Top View

#### **ORDERING INFORMATION**

Device	Package	Shipping
NTQS6466	TSSOP-8	100 Units/Rail
NTQS6466R2	TSSOP-8	3000/Tape & Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

### **NTQS6466**

#### THERMAL RESISTANCE RATINGS

Rating	Symbol	Typical	Max	Unit
Maximum Junction-to-Ambient (Note 2.)	$R_{\theta JA}$			°C/W
t ≤ 10 sec		65	83	
Steady State		100	120	
Maximum Junction-to-Foot	$R_{ heta JF}$			°C/W
Steady State		43	52	

### $\textbf{ELECTRICAL CHARACTERISTICS} \ (T_J = 25^{\circ}C \ unless \ otherwise \ noted)$

Cha	racteristic	Symbol	Min	Тур	Max	Unit
STATIC						
Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA)		VGS(th)	0.45	0.9	_	Vdc
Gate-Body Leakage (VDS = 0 Vd	akage (V <sub>DS</sub> = 0 Vdc, V <sub>GS</sub> = ±8 Vdc)		_	_	±100	nAdc
$(V_{DS} = 16 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$	ero Gate Threshold Voltage Drain Current (VDS = 16 Vdc, VGS = 0 Vdc) (VDS = 16 Vdc, VGS = 0 Vdc, TJ = 70°C)		_ _	- -	1.0 10	μAdc
On-State Drain Current (Note 3.) (V <sub>DS</sub> = 5.0 Vdc, V <sub>GS</sub> = 4.5 Vdc	)	I <sub>D</sub> (on)	20	_	_	Adc
Drain-Source On-State Resistant (VGS = 4.5 Vdc, ID = 8.1 Adc) (VGS = 2.5 Vdc, ID = 6.6 Adc)	e (Note 3.)	R <sub>DS(on)</sub>	_ _	0.014 0.017	0.017 0.020	Ω
Forward Transconductance (VDS	Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 8.1 Adc) (Note 3.)		-	30	-	S
Diode Forward Voltage (I <sub>S</sub> = 1.35	Forward Voltage (I <sub>S</sub> = 1.35 Adc, V <sub>GS</sub> = 0 Vdc (Note 3.)		0.65	1.1	Vdc	
DYNAMIC (Note 4.)						
Total Gate Charge	(Vps = 10 Vdc,	Qg	-	25	27	nC
Gate-Source Charge	$V_{GS} = 5.0 \text{ Vdc},$	Q <sub>gs</sub>	-	3.2	-	
Gate-Drain Charge	$I_D = 8.1 \text{ Adc}$	Q <sub>gd</sub>	-	7.0	-	
Turn-On Delay Time	$(V_{DD} = 10 \text{ Vdc}, R_L = 10 \Omega,$ $I_D \cong 1.0 \text{ Adc},$	<sup>t</sup> d(on)	-	17	45	ns
Rise Time		t <sub>r</sub>	-	80	100	
Turn-Off Delay Time	$V_{GEN} = 4.5 \text{ Vdc},$	td(off)	-	95	110	
Fall Time	$R_G = 6.0 \Omega$ )	t <sub>f</sub>	-	90	100	
Source–Drain Reverse Recovery Time	(I <sub>F</sub> = 1.5 Adc, di/dt = 100 A/μs)	t <sub>rr</sub>	_	28	70	ns

<sup>2.</sup> Surface mounted to 1" x 1" FR-4 board.

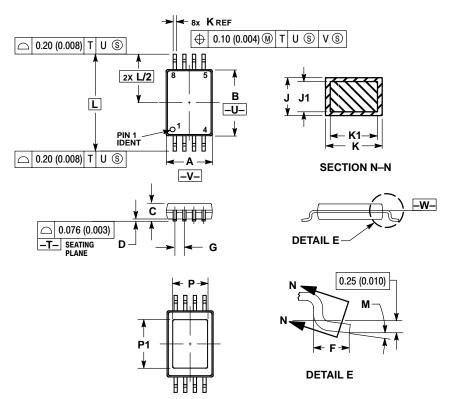
<sup>3.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2%.

<sup>4.</sup> Guaranteed by design, not subject to production testing.

### **NTQS6466**

#### **PACKAGE DIMENSIONS**

#### TSSOP-8 CASE 948S-01 **ISSUE O**



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15
- (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD
  FLASH OR PROTRUSION. INTERLEAD FLASH OR
  PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

  5. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	2.90	3.10	0.114	0.122	
В	4.30	4.50	0.169	0.177	
С		1.10		0.043	
D	0.05	0.15	0.002	0.006	
F	0.50	0.70	0.020	0.028	
G	0.65 BSC		0.026 BSC		
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40 BSC		0.252 BSC		
M	0°	8°	0°	8 °	
Р		2.20		0.087	
P1		3.20		0.126	

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001-800-4422-3781 Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031

**Phone**: 81–3–5740–2700 **Email**: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

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