

NL17SZ04

Single Inverter

The NL17SZ04 is an inverter in two tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

- Tiny SOT-353 and SOT-553 Packages
- -24 mA Balanced Output Sink and Source Capability
- Over-Voltage Tolerant Inputs and Outputs
- Pin For Pin with NC7SZ04P5X, TC7SZ04FU and TC7SZ04AFE
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation

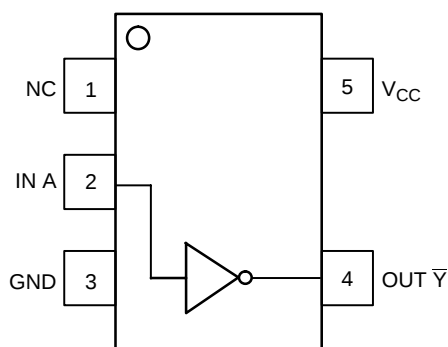


Figure 1. Pinout (Top View)

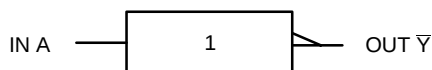
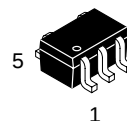


Figure 2. Logic Symbol



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SOT-353/SC70-5/SC-88A
DF SUFFIX
CASE 419A

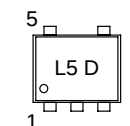
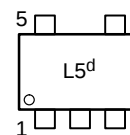
d = Date Code



SOT-553
XV5 SUFFIX
CASE 463B

L5 = Device Marking
D = One Digit Date Code

MARKING DIAGRAMS



PIN ASSIGNMENT

Pin	Function
1	NC
2	IN A
3	GND
4	OUT $\bar{Y}$
5	V_{CC}

FUNCTION TABLE

A Input	$\bar{Y}$ Output
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NL17SZ04

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to +7.0	V
V _I	DC Input Voltage	− 0.5 ≤ V _I ≤ +7.0	V
V _O	DC Output Voltage Output in Higher or Low State (Note 1)	− 0.5 ≤ V _O ≤ +7.0	V
I _{IK}	DC Input Diode Current V _I < GND	− 50	mA
I _{OK}	DC Output Diode Current V _O < GND	− 50	mA
I _O	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Supply Pin	± 100	mA
T _{STG}	Storage Temperature Range	− 65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance SOT-353 (Note 2) SOT-553	350 496	°C/W
P _D	Power Dissipation in Still Air at 85°C SOT-353 SOT-553	186 135	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
ESD	ESD Classification Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	Class IC Class A N/A	

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. IO absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A, rated to EIA/JESD22-A114-B.
4. Tested to EIA/JESD22-A115-A, rated to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage Operating Data Retention	1.65 1.5	5.5 5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage (High or Low State)	0	5.5	V
T _A	Operating Temperature Range	−40	+85	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.0 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0	20 10 5	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40 °C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High- Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	Low- Level Input Voltage		1.65 to 1.95 1.65 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V
V _{OH}	High- Level Output Voltage V _{IN} = V _{IL}	I _{OH} = -100 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -3 mA	1.65	1.29	1.52		1.29		
		I _{OH} = -8 mA	2.3	1.9	2.1		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.7		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.5		2.3		
		I _{OH} = -32 mA	4.5	3.8	4.0		3.8		
V _{OL}	Low- Level Output Voltage V _{IN} = V _{IH}	I _{OL} = 100 μA	1.65 to 5.5		0.0	0.1		0.1	V
		I _{OH} = 3 mA	1.65		0.08	0.24		0.24	
		I _{OL} = 8 mA	2.3		0.20	0.3		0.3	
		I _{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32 mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	0 to 5.5		± 1.0			± 10.0	μA
I _{OFF}	Power Off Leakage Current	V _{OUT} = 5.5 V or V _{IN} = 5.5 V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	1.65 to 5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40 °C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay (Figure 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.65 1.8	2.0 2.0	5.3 4.4	11.4 9.5	2.0 2.0	12.0 10.0	ns
		R _L = 1 MΩ, C _L = 15 pF	2.5 ± 0.2	0.2	3.5	6.5	0.8	7.0	
		R _L = 1 MΩ, C _L = 15 pF	3.3 ± 0.3	0.8	2.1	4.5	0.5	4.7	
		R _L = 500 Ω, C _L = 50 pF		1.2	2.9	5.5	1.5	5.2	
		R _L = 1 MΩ, C _L = 15 pF	5.0 ± 0.5	0.5	1.8	3.9	0.5	4.1	
		R _L = 500 Ω, C _L = 50 pF		0.8	2.4	4.3	0.8	4.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	> 2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NL17SZ04

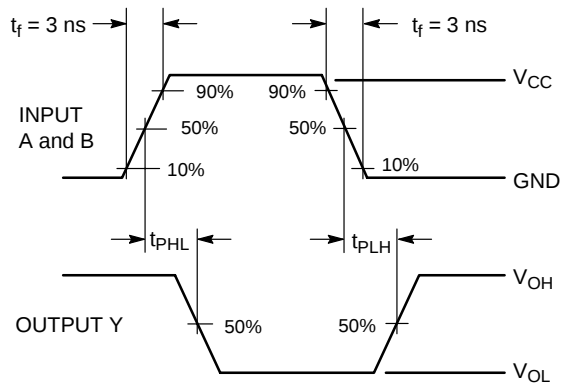
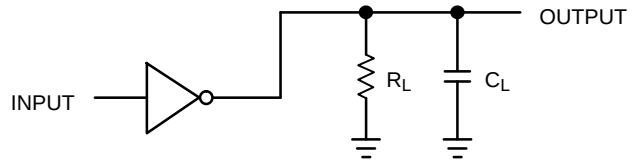


Figure 3. Switching Waveform



A 1- MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL17SZ04DFT2	NL	1	7	SZ	04	DF	T2	SC-88A/ SOT-353/ SC70-5	178 mm, 3000 Unit
NL17SZ04XV5T2	NL	1	7	SZ	04	XV5	T2	SOT-553	178 mm, 4000 Unit

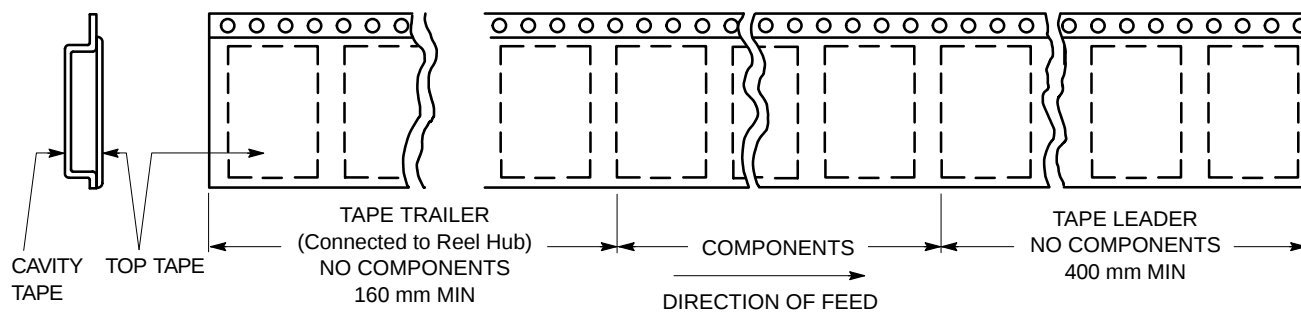
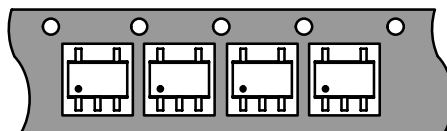
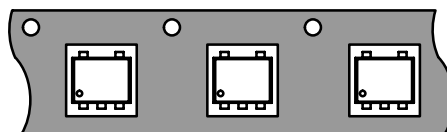


Figure 5. Tape Ends for Finished Goods



"T2" Pin One Opposing Sprocket Hole (3k Reel)

Figure 6. SOT-353/SC70-5/SC-88A Reel Configuration/Orientation



"T2" Pin One Opposing Sprocket Hole (4k Reel)

Figure 7. SOT-553 XV5T2 Reel Configuration/Orientation

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Figure 8. Reel Dimensions

REEL DIMENSIONS†

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

†For additional tape and reel information, refer to Brochure BRD8011/D.

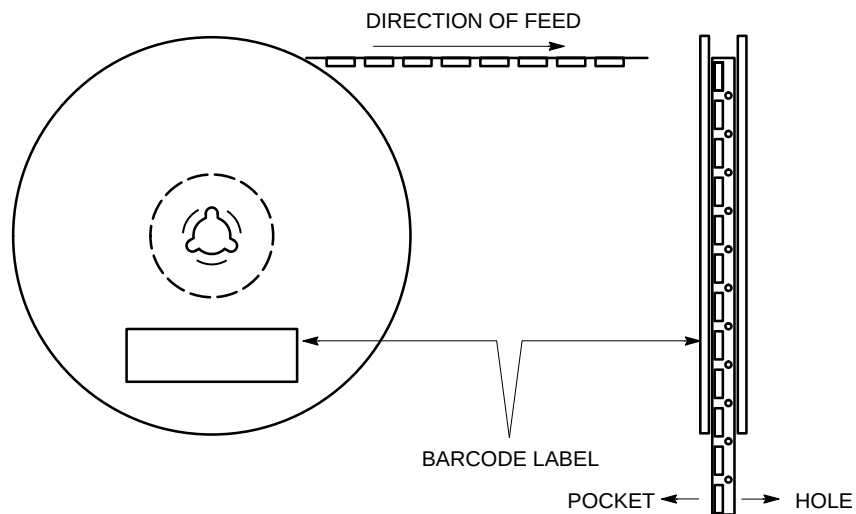
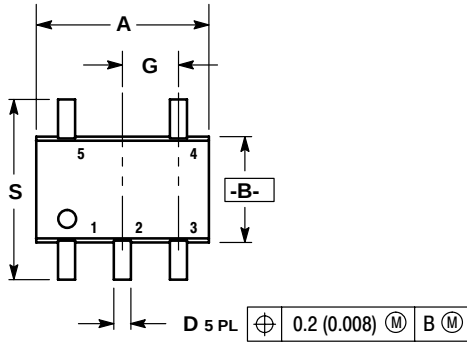


Figure 9. Reel Winding Direction

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PACKAGE DIMENSIONS

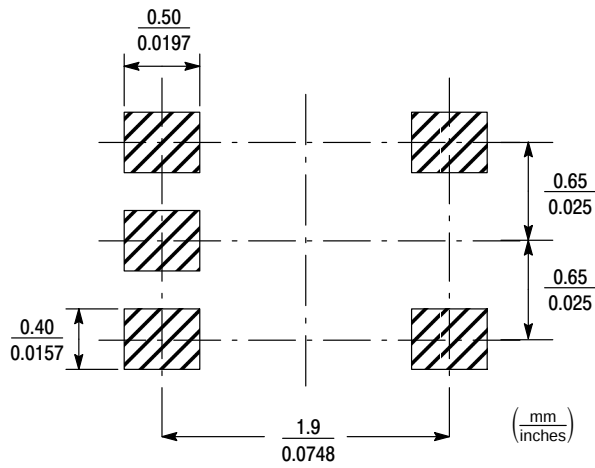
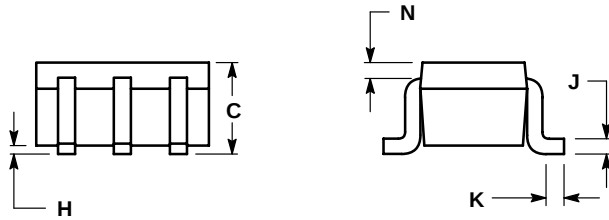
SOT-353
DF SUFFIX
5-LEAD PACKAGE
CASE 419A-02
ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.

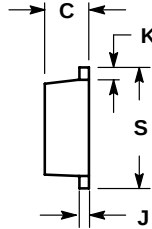
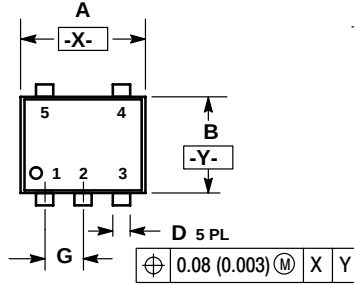
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



NL17SZ04

PACKAGE DIMENSIONS

SOT-553
XV5 SUFFIX
5-LEAD PACKAGE
CASE 463B-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL

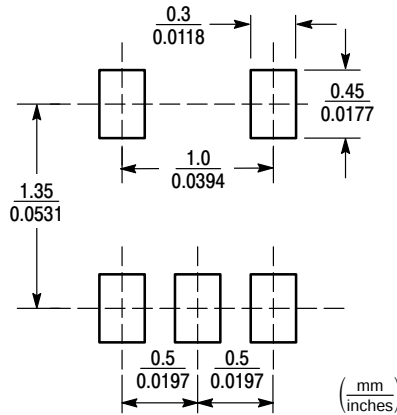
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:

- PIN 1. BASE 1
- EMITTER 1/2
- BASE 2
- COLLECTOR 2
- COLLECTOR 1

STYLE 2:

- PIN 1. CATHODE
- ANODE
- CATHODE
- CATHODE
- CATHODE



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