Advance Information

Power MOSFET

30 A, 30 V N-Channel SO-8 Leadless

The SO-8LL (Leadless) package uses the power QFN package technology. It's footprint matches that of the standard SO-8 single die device. This Leadless SO-8 package provides low parasitic inductance compared to the standard SO-8 package allowing for higher frequency operation.

Features

- Planar HD3E Process for Fast Switching Performance
- Body Diode for Low t_{rr} and Q_{rr}, Optimized for Synchronous Operation
- Low R_{DSon} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- $\bullet \;\; Optimized \; Q_{dg} \; X \; R_{SDon} \; (FOM) \; for \; Shootthrough \; Protection$
- Low Gate Charge
- Surface Mount

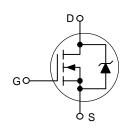
Product Summary

Symbol	Value
V_{DS}	30 V
R _{DSon} @ 10 V	$3.5~\text{m}\Omega$
Q_g	33 nC
I _D	30 A
Q _{gd}	10 nC



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MARKING DIAGRAM





SO-8 Leadless **CASE 751S**

= Specific Device Code XXXXX = Year

WW = Work Week

PIN ASSIGNMENT

PIN	FUNCTION
1	S – SOURCE
2	G – GATE
3	D – DRAIN

ORDERING INFORMATION

Device	Package	Shipping
NTLMS4506N	SO-8 Leadless	2500 Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ Unless otherwise specified)

	Symbol	Value	Units	
Drain-to-Source Voltage		V _{DSS}	30	V _{dc}
Gate-to-Source Voltage	Continuous	V _{GS}	±20	V _{dc}
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		I _D I _{DM} I _{DM}	20 30 84	A A A
Maximum Power Dissipation (S Single Pulse (t _p = 10 Secs) T _A	Steady State) @ T _A = 25°C (Note 1) = 25°C (Note 2)	P _D P _D	2.5 6.0	W W
Operating and Storage Temper	rature	T _J and T _{stg}	-55 to 150	°C
Single Pulse Drain-to Source	Avalanche Energy Starting T _J = 25°C	E _{AS}	220	mJ
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2) Junction-to-Ambient (Note 3)		$egin{array}{c} R_{ hetaJA} \ R_{ hetaJA} \ R_{ hetaJA} \end{array}$	50 20 100	°C/W
Maximum Lead Temperature for	or Soldering Purposes, 1/8" from Case for 10 Secs	TL	260	°C

When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
 1" pad (Cu Area 0.911 in²), t < 10sec.
 When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).
 Chip current capability limited by package.

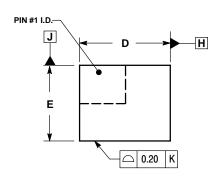
ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

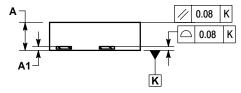
Characteristics		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS		•	_	•	•	
Drain-to-Source Breakdown Voltage ($V_{GS} = 0 \ V_{dc}, \ I_D = 250 \ \mu A_{dc}$) Temperature Coefficient (Positive)	Note 5)	V(br) _{DSS}	30 -	33 25	_ _	V _{dc} mV/°C
Zero Gate Voltage Drain Current $(V_{DS} = 24 V_{dc}, V_{GS} = 0 V_{dc})$ $(V_{DS} = 24 V_{dc}, V_{GS} = 0 V_{dc}, T_{J} = 18)$	50 °C)	I _{DSS}	_ _	- -	1.0 10	μA _{dc}
Gate-Body Leakage Current	$(V_{GS} = \pm 20 \ V_{dc}, \ V_{DS} = 0 \ V_{dc})$	I _{GSS}	_	_	±100	nA _{dc}
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage (Note 5) $(V_{DS} = V_{GS}, I_D = 250 \; \mu A_{dc})$ Threshold Temperature Coefficient (No	egative)	V _{GS} (th)	1.0	1.5 -3.8	2.0	V _{dc} mV/°C
Static Drain-to-Source On-Resistance $V_{GS} = 10 V_{dc}$, $I_D = 30 A_{dc}$ $V_{GS} = 4.5 V_{dc}$, $I_D = 15 A_{dc}$	e (Note 5)	R _{DS} (on)	_ _	3.5 4.8	4.4 5.8	mΩ
Forward Transconductance (Note 5)	$(V_{DS} = 10 \ V_{dc}, \ I_{D} = 10 \ A_{dc})$	9FS	_	90	_	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = 30 V_{dc}, V_{GS} = 0 V, f = 1 MHz)$	C _{iss}	_	4900	5150	pF
Output Capacitance	7	C _{oss}	-	1275	1352	
Transfer Capacitance	7	C _{rss}	_	380	400	1
SWITCHING CHARACTERISTICS (N	ote 6)					
Turn-On Delay Time	$(V_{en} = 10 V_{dc}, V_{DD} = 15 V_{dc}, I_D = 30 A_{dc}, R_G = 2.5 \Omega)$	t _d (on)	-	30	36	ns
Rise Time	$R_{G} = 2.5 \Omega$	t _r	-	15	19	
Turn-Off Delay Time	7	t _d (off)	-	110	132	
Fall Time	7	tf	-	35	42	
Gate Charge	$(V_{GS} = 4.5 V_{dc}, I_D = 30 A_{dc}, V_{DS} = 10 V_{dc})$ (Note 5)	Q _{T(g)}	-	33	36	nC
	$V_{DS} = 10 V_{dc}$ (Note 5)	Q _{1(gs)}	-	18	-	
		Q _{2(gd)}	-	10	-	
		Q _{sw}	-	TBD	-	
		Q _{oss}	_	TBD	_	
SOURCE-DRAIN DIODE CHARACTI	ERISTICS					
Forward On-Voltage	$(I_S = 15 A_{dc}, V_{GS} = 0 V_{dc})$ (Note 5) $(I_S = 1.5 A_{dc}, V_{GS} = 0 V_{dc}, T_J = 150^{\circ}C)$	V _{SD}	_ _	0.70 0.7	1.2 -	V _{dc}
Reverse Recovery Time	$(I_S = 15 A_{dc}, V_{GS} = 0 V_{dc}, V_{DD} = 24 V)$	t _{rr}	_	37	54	ns
	dl _S /dt = 100 A/μs) (Note 5)	t _a	_	20	_	
		t _b	_	18	_	
Reverse Recovery Stored Charge	7	Q _{RR}	_	0.026	_	μС

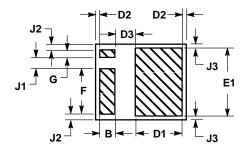
^{5.} Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperatures.

PACKAGE DIMENSIONS

SO-8 Leadless CASE 751S-02 ISSUE A







NOTES

- DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETER.

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	MILLIMETERS			
DIM	MIN	MAX		
Α	1.750 1.950			
A1	0.254 REF			
В	0.900 1.100			
D	6.000 BSC			
D1	3.046	3.246		
D2	0.154 0.354			
D3	1.246 1.446			
Е	5.000 BSC			
E1	4.392	4.592		
F	2.940	3.140		
G	0.400 0.600			
J1	0.680 0.880			
J2	0.250 0.450			
J3	0.154 0.354			

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