NTLMS4505N

Advance Information

Power MOSFET

31 A, 24 V N–Channel SO–8 Leadless

The SO–8LL (Leadless) package uses the power QFN package technology. It's footprint matches that of the standard SO–8 single die device. This Leadless SO–8 package provides low parasitic inductance compared to the standard SO–8 package allowing for higher frequency operation.

Features

- Planar HD3E Process for Fast Switching Performance
- Body Diode for Low t_{rr} and Q_{rr}, Optimized for Synchronous Operation
- Low $R_{DSo}n$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Optimized Q_{dg} X R_{SDon} (FOM) for Shoothrough Protection
- Low Gate Charge

Product Summary

Symbol	Value
V_{DS}	24 V
R_{DSon} @ 10 V	3.0 mΩ
Q_g	33 nC
I_D	31 A
Q_{gd}	10 nC

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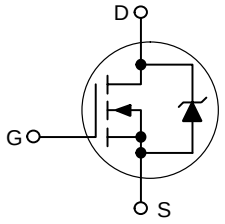
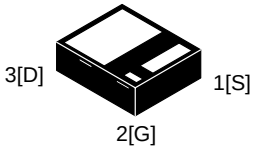


MARKING DIAGRAM



SO–8 Leadless
CASE 751S

xxxxx = Specific Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT

PIN	FUNCTION
1	S – SOURCE
2	G – GATE
3	D – DRAIN

ORDERING INFORMATION

Device	Package	Shipping
NTLMS4505N	SO–8 Leadless	2500 Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_J=25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	24	V_{dc}
Gate–to–Source Voltage – Continuous	V_{GS}	±20	V_{dc}
Drain Current			
Continuous @ T_A = 25°C (Note 1)	I_D	20	A
Continuous @ T_A = 25°C (Note 2)	I_{DM}	31	A
Single Pulse (t_p = 10 μs) (Note 4)	I_{DM}	84	A
Maximum Power Dissipation (Steady State) @ T_A = 25°C (Note 1)	P_D	2.5	W
Single Pulse (t_p = 10 Secs) T_A = 25°C (Note 2)	P_D	6.0	W
Operating and Storage Temperature	T_J and T_{stg}	–55 to 150	°C
Single Pulse Drain–to Source Avalanche Energy – Starting T_J = 25°C	E_{AS}	220	mJ
Thermal Resistance			°C/W
Junction–to–Ambient (Note 1)	$R_{\theta JA}$	50	
Junction–to–Ambient (Note 2)	$R_{\theta JA}$	20	
Junction–to–Ambient (Note 3)	$R_{\theta JA}$	100	
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 10 sec	T_L	260	°C

1. When surface mounted to an FR4 board using 1” pad size, (Cu Area 1.127 in^2).
2. 1” pad (Cu Area 0.911 in^2), t < 10 sec.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).
4. Chip current capability limited by package.

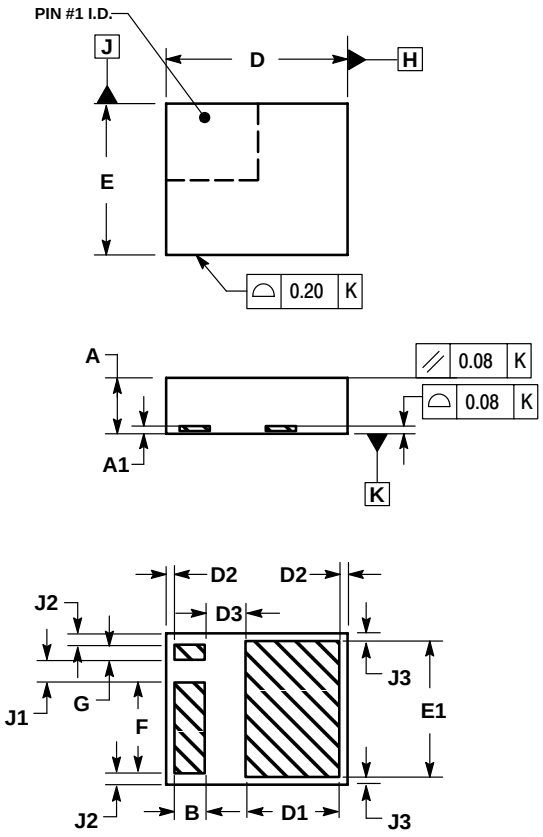
ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Note 5) Temperature Coefficient (Positive)	(V_{GS} = 0 V_{dc}, I_D = 250 μA_{dc})	$V(br)_{DSS}$	24 –	28 25	– –	V_{dc} mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}) (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 150 °C)		I_{DSS}	 – –	 – –	 1.0 10	μA_{dc}
Gate–Body Leakage Current	(V_{GS} = ±20 V_{dc}, V_{DS} = 0 V_{dc})	I_{GSS}	–	–	±100	nA_{dc}
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage (Note 5) Threshold Temperature Coefficient (Negative)	(V_{DS} = V_{GS}, I_D = 250 μA_{dc})	V_{GS}(th)	1.0 –	1.5 –3.8	2.0 –	V_{dc} mV/°C
Static Drain–to–Source On–Resistance (Note 5)	(V_{GS} = 10 V_{dc}, I_D = 31 A_{dc} (V_{GS} = 4.5 V_{dc}, I_D = 15 A_{dc}	R_{DS}(on)	– –	3.0 4.3	4.2 5.0	mΩ
Forward Transconductance (Note 5)	(V_{DS} = 10 V_{dc}, I_D = 10A_{dc})	g_{FS}	–	90	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 30 V_{dc}, V_{GS} = 0 V f = 1 MHz)	C_{iss}	–	4900	5150	pF
Output Capacitance		C_{oss}	–	1275	1352	
Transfer Capacitance		C_{rss}	–	380	400	
SWITCHING CHARACTERISTICS (Note 6)						
Turn–On Delay Time	(V_{en} = 10 V_{dc}, V_{DD} = 15 V_{dc} I_D = 31 A_{dc}, R_G = 2.5 Ω)	t_d(on)	–	30	36	ns
Rise Time		t_r	–	15	19	
Turn–Off Delay Time		t_d(off)	–	110	132	
Fall Time		tf	–	35	42	
Gate Charge	(V_{GS} = 4.5 V_{dc}, I_D = 31 A_{dc}, V_{DS} = 10 V_{dc}) (Note 5)	$Q_{T(g)}$	–	33	36	nC
		$Q_{1(gs)}$	–	18	–	
		$Q_{2(gd)}$	–	10	–	
		Q_{sw}	–	TBD	–	
		Q_{oss}	–	TBD	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 15A_{dc}, VGS = 0 V_{dc}) (Note 5) (I_S = 1.5 A_{dc}, VGS = 0 V_{dc}, T_J = 150°C)	V_{SD}	–	0.70 0.7	1.2 –	V_{dc}
Reverse Recovery Time	(I_S = 15 A_{dc}, V_{GS} = 0 V_{dc}, V_{DD} = 24 V, dI_S/dt = 100 A/μs) (Note 5)	t_{rr}	–	37	54	ns
		t_a	–	20	–	
		t_b	–	18	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.026	–	μC

5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperatures.

PACKAGE DIMENSIONS

SO–8 Leadless
CASE 751S–02
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS	
DIM	MIN	MAX
A	1.750	1.950
A1	0.254 REF	
B	0.900	1.100
D	6.000 BSC	
D1	3.046	3.246
D2	0.154	0.354
D3	1.246	1.446
E	5.000 BSC	
E1	4.392	4.592
F	2.940	3.140
G	0.400	0.600
J1	0.680	0.880
J2	0.250	0.450
J3	0.154	0.354

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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