NEXFLASH®
Technologies, Inc.

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NX25F080C, NX25F160C AND NX25F320C

8M-BIT, 16M-BIT AND 32M-BIT SERIAL FLASH MEMORY WITH 4-PIN SPI INTERFACE

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FEATURES

- **8M/16M/32M-bit Serial Flash Memory**

- **Flash storage for systems with limited pins, space, and power**
  - Ideal for high density serial code-download
  - Data, voice and image storage
  - Battery-operated products

- **Nonvolatile Memory Technology**
  - Single transistor EEPROM memory
  - 2048/4096/8192 sectors of 528 bytes each
  - Sector erase/write time of 10 ms/sector (typical)
  - 100,000 erase/write cycles
  - Ten year data retention

- **4-pin SPI Serial Interface**
  - Easily interfaces to popular microcontrollers
  - Clock operation as fast as 16MHz
  - Optional Hold and Ready/Busy pin functions

- **Ultra-low Power for Battery-Operation**
  - Single 2.7-3.6V supply for Read, Erase/Write
  - 1 µA standby, 5 mA active (typical)

- **Special Features**
  - Two on-board 528-byte SRAM Buffers
  - Byte-level addressing
  - Transfer and Compare sector to SRAM
  - Configurable software write-protection
  - Continuous Auto-Increment Read

- **Package Options**
  - 28-PIN TSOP (Type I)
  - Removable Cards and Modules

DESCRIPTION

The NX25F080/160/320C Serial Flash memory provide a storage solution for systems which are limited in power, pins, space, hardware and firmware resources. The NX25F080/160/320C is ideal for applications that store voice, images and data in a portable/mobile environment as well for down-loading code into controllers with embedded DRAM or SRAM. The NX25F080/160/320C operates on a single 2.7V-3.6V power supply for read and erase/write with typical current consumption as low as 5mA active and less than 1uA standby. The array is organized into 2048/4096/8192 sectors of 528 bytes each. Sector erase/write speeds are as fast as 10ms. The 4-pin SPI serial interface works directly with popular micro-controllers. Special features include dual on-chip serial SRAM, byte-level addressing, and transfer/compare sector to SRAM, hardware/software write protection, auto-increment read and removable Serial Flash Module packaging option. Development is supported with the PC-based NexFlash Serial Flash Development Kit.

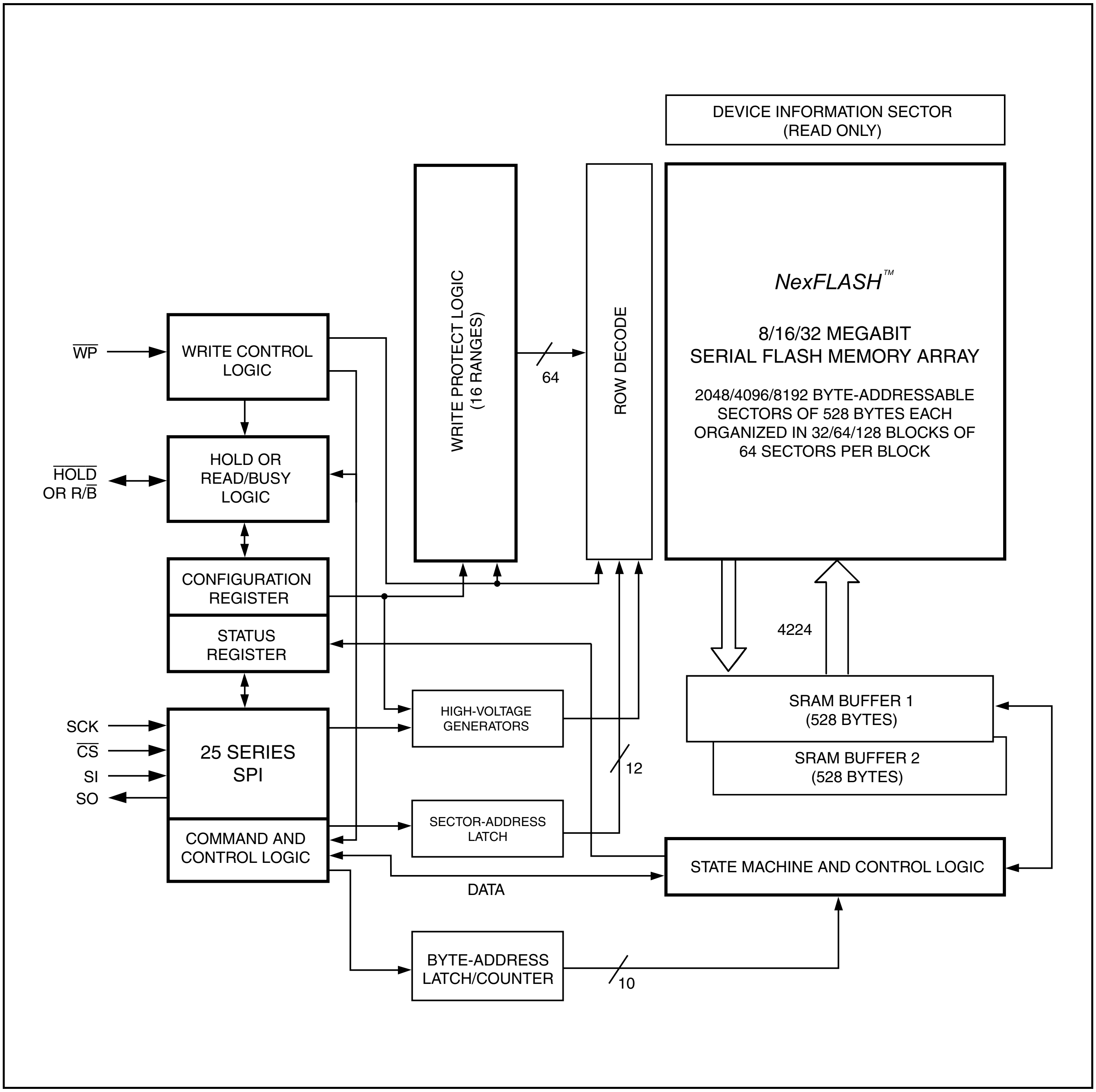


Figure 1. NX25F080/160/320C Architectural Block Diagram

Pin Descriptions

Serial Data Input (SI)
The SI pin receives data into the device with the SCK pin. All data transmitted to the device is clocked relative to the rising edge of SCK.

Serial Data Output (SO)
The SO pin transmits data from the device with the SCK pin. All data transmitted from the device is clocked relative to the edge defined with the RCE bit in the configuration register. The default is RCE bit set to 0 which outputs data on the falling edge of the SCK pin and is compatible with standard systems that support SPI. The clock rate can be faster with the SPI_RCE bit set to 1, (see t_{CYC} in AC Characteristics).

Serial Clock Input (SCK)
All commands and data written to the SI pin are clocked relative to rising edge of SCK. All data read from the SO pin is clocked relative to the rising or falling edge of SCK.

Chip Select (CS)
The chip select input is required to start and finish an SPI command. SCK must be low when chip select is asserted low. Upon power-up, an initial low-high transition of chip select is required before any command will be acknowledged. Once the device is de-selected, the SO pin will enter a high impedance state and power consumption will be reduced to standby levels unless a transfer, compare, or sector programming are in progress. If a transfer, compare, or sector programming is in progress, the command will complete and then the device will enter standby mode.

Write Protect Input (WP)
The write protect input (WP) works in conjunction with the configuration register bits WR3..WR0, WD, and the status register bit WE. When WP is asserted low, the entire flash memory array is write protected. When the WP pin is high and the status register WE bit set, the device addresses corresponding to the write protect range and direction are write protected. When the status register bit WE is reset, the entire array is write protected. See the section on the configuration register for more details.

HOLD , Ready/Busy or No-connect (HOLD, R/B or N/C)
This multifunction pin can serve either as a Hold input (HOLD), Ready/Busy output (Ready-/Busy or a No-connect). The pin function is user programmable through the configuration register bits HR0, HR1. The device comes from the factory with this pin programmed as a No Connect (NC). The pin can be re-configured by the user by writing to the configuration register.

Power Supply Pins (Vcc and Gnd)
The NX25F080/160/320C supports a single power supply between 2.7V and 3.6V connected to the Vcc and Gnd pins.

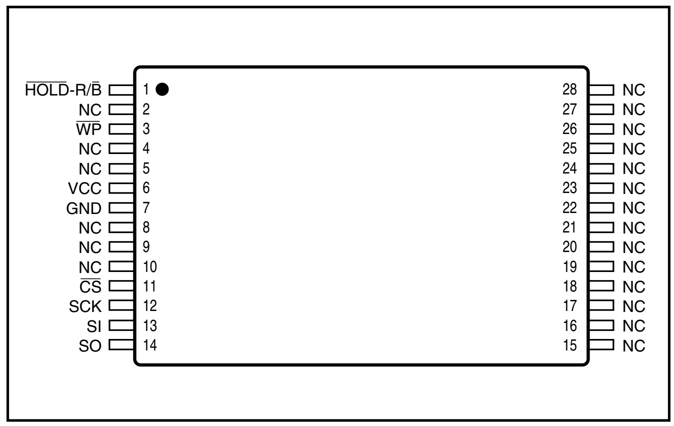


Figure 2. NX25F080/160/320C Pin Assignments SPI Interface, 28-Pin TSOP, Type I (T Package)

Table 1. Pin Descriptions for the 25F640

SI	Serial Data Input
SO	Serial Data Output
SCK	Serial Clock Input
CS	Chip Select Input
WP	Write Protect Input
Hold, R/B	Hold Input Ready-Busy Output or No Connect
VCC	Power Supply
GND	Ground

Serial Flash Memory Array

The NX25F080/160/320C Serial Flash memory array is organized as 2048/4096/8192 sectors of 528-bytes (4,224 bits) each, as shown in Figure 3. The block size of the device is 64 sectors, yielding 64 blocks for the NX25F080/160/320C.

The Serial Flash memory of the NX25F080/160/320C are byte-addressable for read operations. This allows a single byte, or specified sequence of bytes, to be read without having to clock an entire 528-byte sector out of the device. In most cases data is read through one of two 528-byte SRAM buffers by using the Transfer Sector to SRAM and Read SRAM commands. For applications that require a continuous serial stream of data, such as downloading code into SRAM or DRAM upon power-up, a Read Sector with Auto Increment command is provided. This command allows the data from and entire device or a large numbers of sectors to be read with a single command. When the clock reaches the end of a sector it automatically increments to the next and so on. Data can be written to the Flash memory array one sector (528-bytes) at a time through the Serial SRAM using a *Write to Sector* command or a *Transfer SRAM to Sector* command. No pre-erase is needed. Instead, the device incorporates an auto-erase-before-write feature that automatically erases the addressed sector at the beginning of the write operation. After completing the command the memory array will become busy while it is programming the specified non-volatile memory cells of that sector. This busy time will not exceed t_{WP} during which time the Flash array is unavailable for read or write access. The device can be tested to determine the array's availability using the Ready/Busy status that is available during most read commands, through the status register, or on the Ready/Busy pin.

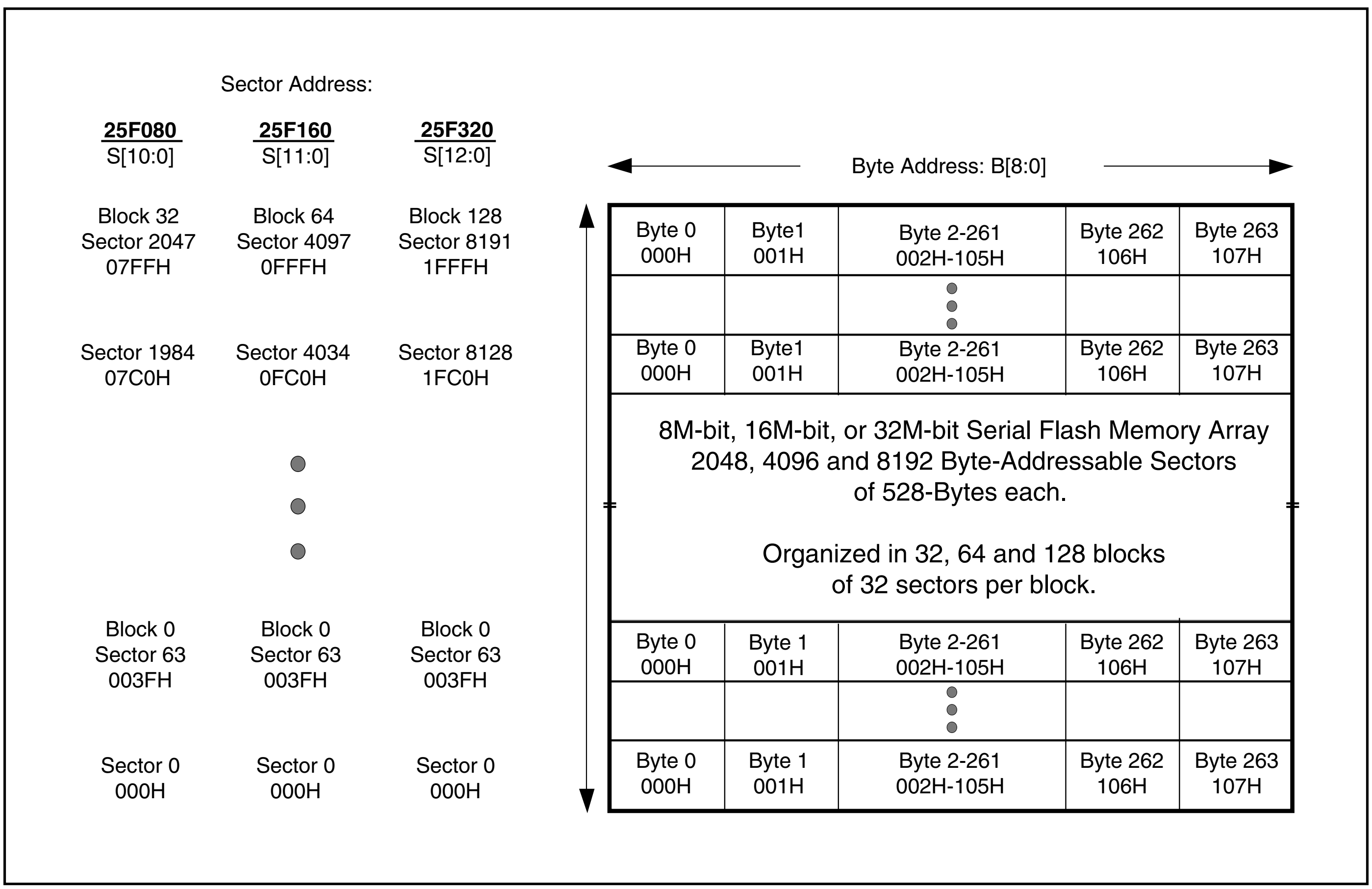


Figure 3. NX25F080/160/320C Serial Flash Memory Array

After sector programming is complete and the device is ready, it is recommended to verify the data in the sector with the data in the SRAM using the compare command, (see Write/ Verify Flow towards the end of this data sheet).

Serial SRAM

One of the most powerful features of the NX25F080/160/320C is the integrated dual Serial SRAMs. The main purpose of the Serial SRAMs is to serve as a buffer for sector data to be written into the Serial Flash memory array. Using the *Write to Sector* command, data is first shifted into the SRAM from the SPI bus. When the command sequence has been completed, the entire 528-bytes is written to the selected sector. See Erase/Write cycle timing (t_{WP}).

The SRAM is fully byte-addressable. Thus, the entire 528-bytes, a single byte, or a sequence of bytes can be read from, or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The *Transfer Sector to SRAM* command allows the contents of a specified sector of Flash memory to be moved to the SRAM (see figure 4). This can be useful when only a portion of a sector needs to be altered. In this case the sector is first transferred to the SRAM, where modifications are made using the *Write to SRAM* command. Once modifications are completed, a *Transfer SRAM to Sector* command is used to update the sector.

The *Compare Sector* command allows the contents of the SRAM to be compared with the specified sector in memory. The result of the compare is set in the status register. This command is useful for performing a fast verify of the last sector write operation (see Write/ Verify Flow figure 12). This command can be useful when re-writing multi-sector files that have only minor changes from the previous write. If the new data in the SRAM is the same as the previously written data, the sector can be skipped. Used in this way, the command saves time that would have been used for programming. It also extends the endurance of the Flash memory cells.

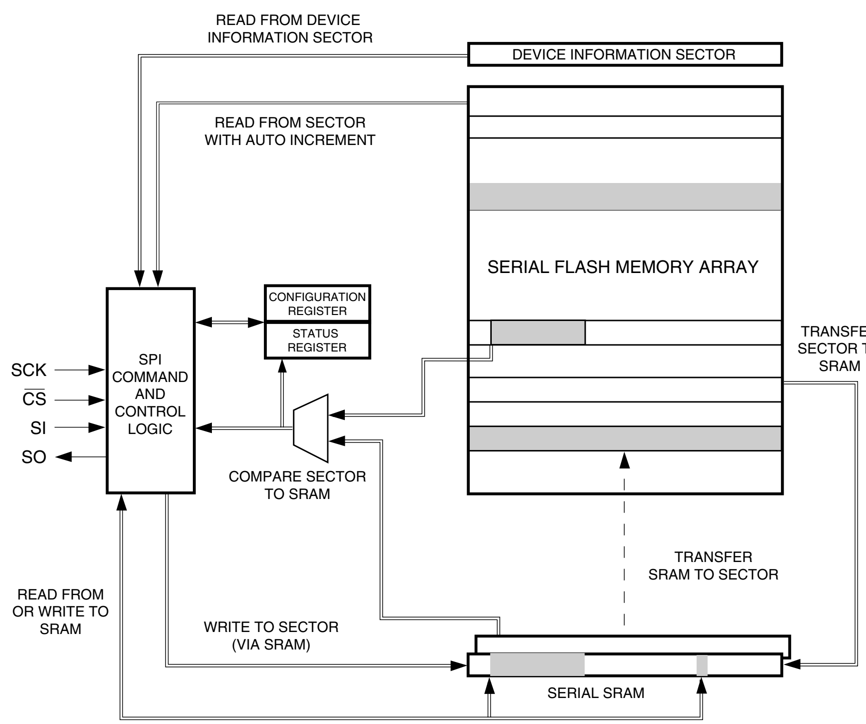


Figure 4. Command Relationships of the SPI Interface, Serial Flash Memory Array and SRAM

Using the SRAM Independent of Flash Memory
The SRAM can be used independently of Flash memory operations for lookup tables, variable storage, or scratch pad purposes. If the Flash memory needs to be written to while SRAM is being used for a different purpose, the contents can be temporarily stored to a sector and then transferred back again when needed. The SRAM can be especially useful for RAM-limited microcontroller-based systems, eliminating the need for external SRAM and freeing pins for other purposes. It can also make it possible to use small pin-count microcontrollers, since only a few pins are needed for the interface instead of the 20-40 pins required for parallel bus-oriented Flash devices.

Write Protection

The NX25F080/160/320C provide advanced software and hardware write protection features. Software-controlled write protection of the entire array is handled using the *Write Enable and Write Disable* commands. Hardware write protection is possible using the Write Protect pin ($\overline{WP}$). Write-protecting a portion of Flash memory is accommodated by programming a write protect range in the configuration register.

Configuration Register

The Configuration Register stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read clock edge and write protect range (Figure 5). The configuration register is accessed using the *Write and Read Configuration Register* commands. The non-volatile configuration register will maintain its setting even when power is removed.

To avoid unnecessary programming of the configuration register, and to save time during power-up, the configuration register should be read upon power-up and compared to the intended setting before sending a Write Configuration Register command (Figure 5).

The factory default setting for the configuration register is CF7-CF0 is: 0000 1001 B (write protect range = none, read using falling edge of the clock, and pin 1 = no connect). Bits CF15-CF8 are reserved. When writing to the configuration register CF15-CF8 should be 0. When reading, the settings of CF15-CF8 should be ignored.

Write Protect Range and Direction, WR[3:0], WD
The write protect range and direction bits WR[3:0] and WD are located at configuration bits CF[7:4] and CF[3] respectively. The write protect range and direction bits select how the array is protected. They work in conjunction with the $\overline{WP}$ input pin, valid only if $\overline{WP}$ is inactive (high). WR[3:0] can select write protection of all sectors, none of the sectors, or specific sectors grouped in blocks of 64 (~32 KB). The WD bit specifies whether the protected block range starts from the first sector, address 0 (000H), or from the last sector (0FFF). Table 2 lists the write protect

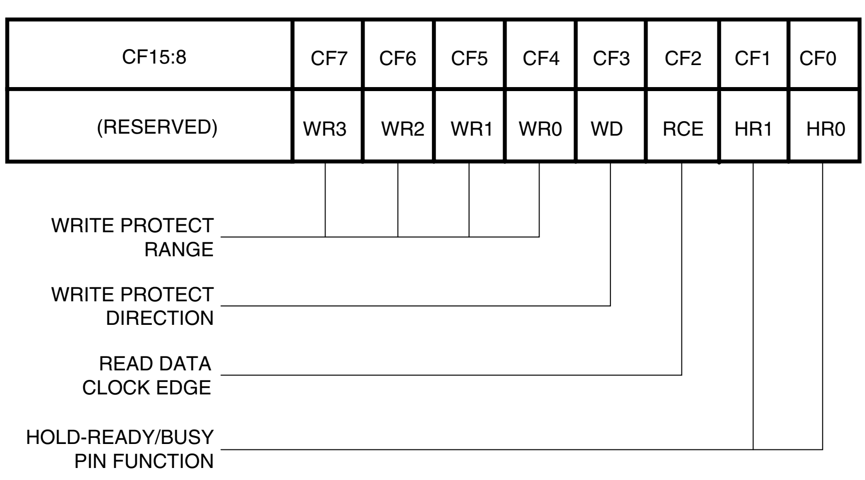


Figure 5. Configuration Register Bit Locations

sector range for the devices. Once protected, all further writes to sectors within the range will be ignored. The factory default setting is with no write protected sectors, WR=[0,0,0,0] and WD=1.

Read Clock Edge, RCE

The Read Clock Edge bit (RCE) is located at configuration bit location CF[2]. It selects which edge of the clock (SCK) is used while reading data out of the device. Although the SPI protocol specifies that data is written during the rising edge and read on the falling edge of the clock, if required, the output can be driven on the rising edge of the clock by setting the configuration registers RCE bit to a 1. Using the rising edge of clock for reading data may be beneficial to the timing of some high-speed systems. The factory default setting is the falling edge of SCK for standard SPI.

RCE=0 Read data is output on the falling edge of SCK (Standard SPI).

RCE=1 Read data is output on the rising edge of SCK(Fast SPI).

Table 2A. Write Protect Range for the NX25F080C

Write Protect Range Config. Bits				Write Protected Sectors (Hex)	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	0000-007F	07C0-07FF
0	0	1	0	0000-007F	0F80-0FFF
0	0	1	1	0000-00BF	0F40-0FFF
0	1	0	0	0000-00FF	0F00-0FFF
0	1	0	1	0000-013F	0EC0-0FFF
0	1	1	0	0000-017F	0E80-0FFF
0	1	1	1	0000-01BF	0E40-0FFF
1	0	0	0	0000-01FF	0E00-0FFF
1	0	0	1	0000-023F	0DC0-0FFF
1	0	1	0	0000-027F	0D80-0FFF
1	0	1	1	0000-02BF	0D40-0FFF
1	1	0	0	0000-02FF	0D00-0FFF
1	1	0	1	0000-033F	0CC0-0FFF
1	1	1	0	0000-037F	00C0-07FF
1	1	1	1	ALL	ALL

Table 2B. Write Protect Range for the NX25F160C

Write Protect Range Config. Bits				Write Protected Sectors (Hex)	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	0000-003F	0FC0-0FFF
0	0	1	0	0000-007F	0F80-0FFF
0	0	1	1	0000-00BF	0F40-0FFF
0	1	0	0	0000-00FF	0F00-0FFF
0	1	0	1	0000-013F	0EC0-0FFF
0	1	1	0	0000-017F	0E80-0FFF
0	1	1	1	0000-01BF	0E40-0FFF
1	0	0	0	0000-01FF	0E00-0FFF
1	0	0	1	0000-023F	0DC0-0FFF
1	0	1	0	0000-027F	0D80-0FFF
1	0	1	1	0000-02BF	0D40-0FFF
1	1	0	0	0000-02FF	0D00-0FFF
1	1	0	1	0000-033F	0CC0-0FFF
1	1	1	0	0000-037F	0C80-0FFF
1	1	1	1	ALL	ALL

Table 2C. Write Protect Range for the NX25F320C

Write Protect Range Config. Bits				Write Protected Sectors (Hex)	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	0000-003F	1FC0-1FFF
0	0	1	0	0000-007F	0F80-0FFF
0	0	1	1	0000-00BF	0F40-0FFF
0	1	0	0	0000-00FF	0F00-0FFF
0	1	0	1	0000-013F	0EC0-0FFF
0	1	1	0	0000-017F	0E80-0FFF
0	1	1	1	0000-01BF	0E40-0FFF
1	0	0	0	0000-01FF	0E00-0FFF
1	0	0	1	0000-023F	0DC0-0FFF
1	0	1	0	0000-027F	0D80-0FFF
1	0	1	1	0000-02BF	0D40-0FFF
1	1	0	0	0000-02FF	0D00-0FFF
1	1	0	1	0000-033F	0CC0-0FFF
1	1	1	0	0000-037F	18C0-1FFF
1	1	1	1	ALL	ALL

$\overline{\text{HOLD}}$-R/$\overline{\text{B}}$, HR[1:0]

The Hold-Ready/Busy ($\overline{\text{HOLD}}$-R/$\overline{\text{B}}$) bits HR1 and HR0 are located at bits CF[1:0] of the configuration register. These two bits select one of four possible functions: No Connect, $\overline{\text{HOLD}}$ input, R/$\overline{\text{B}}$ Output, or R/$\overline{\text{B}}$ Output with open drain. The factory setting for the pin is "No Connect".

HR1	HR0	Pin Configuration
0	0	$\overline{\text{HOLD}}$ input
0	1	No Connect
1	0	R/$\overline{\text{B}}$ Output (Open Drain)
1	1	R/$\overline{\text{B}}$ Output

Configured as a R/$\overline{\text{B}}$ output, the pin can serve as a system interrupt. When R/$\overline{\text{B}}$ is high, the array is ready to be programmed. When R/$\overline{\text{B}}$ is low, it is busy programming. If configured with an open-drain, an external pull-up resistor should be used.

As a $\overline{\text{HOLD}}$ input, the pin can be used in conjunction with the $\overline{\text{CS}}$ and SCK pin to suspend a serial command sequence without resetting the command. This can be useful if a command is in process and a higher priority task on the same SPI bus needs to be attended to. To suspend a command, $\overline{\text{HOLD}}$ must be brought low while $\overline{\text{CS}}$ and SCK are low. With $\overline{\text{HOLD}}$ low, further data on the SI pin is ignored (even while SCK is clocked) and the SO pin goes to or remains in a high-impedance state. To resume the command sequence, $\overline{\text{HOLD}}$ must be brought high when $\overline{\text{CS}}$ and SCK are low.

Status Register Bit Descriptions

The status register provides status of the Flash array's Ready/Busy condition (R/$\overline{\text{B}}$), transfers between the SRAM and program buffer (TR0 and TR1), Write-Enable/Disable (WE), Compare Not Equal (CNE), Power Detect (PD) and Data Integrity status (DI0 and DI1). The register can be read using the Read Status Register command (Figure 6).

Ready/Busy Status, BUSY

The BUSY status bit is located at bit ST[15] of the status register. Testing the BUSY bit is one of several ways to check Ready/Busy status of the array. At power-up the BUSY bit is reset to 0.

BUSY=1 The device is busy programming.
BUSY=0 The deivce is ready for further use.

SRAM Transfer or Compare, TR0 and TR1

The TR status bits are located at bit ST[13] and ST[14] of the status register. The bits provide status during the *Transfer Sector to SRAM, Transfer SRAM to SRAM, Compare Sector to SRAM* and *Refresh Sector* commands. An active state 1 indicates the SRAM Array is not avail-

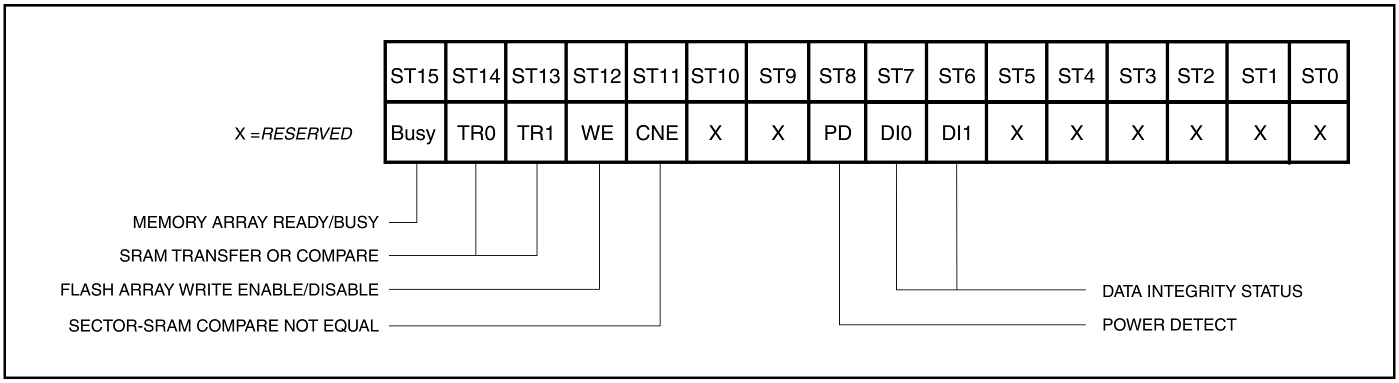


Figure 6. Status Register Bit Locations

able for use. The device will also indicate a BUSY state while the TR bits are active. Upon power up the TR bits reset to 0.

TR=1 Transfer, Compare or Refresh in Process.
TR=0 Transfer, Compare or Refresh not in Process.

Write Enable/Disable, WE

The WE status bit is located at bit ST[12] of the status register. The bit provides write protect status of global *Write Enable and Write Disable* commands. Upon power-up the WE bit resets to 0.

WE=1 Write Enabled, array can be written to.
WE=0 Write Disabled, array can not be written to.

Compare Not Equal, CNE

The CNE status bit is located at bit ST[11] of the status register. The bit provides a comparison result during a *Compare Sector with SRAM* command. The CNE bit is reset to a 0 upon power-up and when a *compare with SRAM* command is executed.

CNE=1 Sector and SRAM contents are not equal.
CNE=0 Sector and SRAM are equal or CNE bit reset.

Power Detect, PD

The Power Detect bit ST[8] works in conjunction with the Set Power Detection and Reset Power Detection Commands and is primarily used for removable media applications. The Set Power Detect Command must be issued before the PD bit can be used for power detection.

PD=0 Power has been removed
PD=1 Power has not been removed

Data Integrity Status Bits (DI0, DI1)

The Data Integrity status bits provide an indication of the data integrity of the last sector that was tranfered to the SRAM. The bits should be checked after every transfer sector to SRAM operation.

DI0, DI1 = 00 Sector data is valid
DI0, DI1 =10 Block refresh is recommended
DI0, DI1 =11 Sector data error

If DI0 and DI1 = 00, data is valid and no action is required. If DI0 and DI1 = 10, the 64 sectors within the block that was last read should be refreshed (see Refresh command). If DI0 and DI1 = 11 a data read error has occurred. Possible cause for a data error might be excessive system noise, improper power supply levels during the read or write operation, or excessive erase/write cycles. Contact NexFlash applications department for further information regarding handling data error status.

Command Set

The NX25F080/160/320C has a powerful command set that is fully controlled through the SPI bus. Command relationships are shown in Figure 4 and a list of commands and their associated address, status, clock, and data bytes are shown in Table 3. Flow diagrams for writing to a sector and reading from a sector are shown in Figures 7 and 8. Detailed clock timing of the Write to Sector using SRAM, Transfer Sector to SRAM and Read SRAM command sequences are shown in Figures 9, 10 and 11.

After power up, a device enters an idle state that will maintain until $\overline{CS}$ pin is asserted low. Chip reset is defined as a low to high transition of CS. Thus, to reset the chip at power on, a high to low to high transition is required. A command may start after a high to low transition of CS. When a command is started, CS needs to stay low for the duration of the command and data.

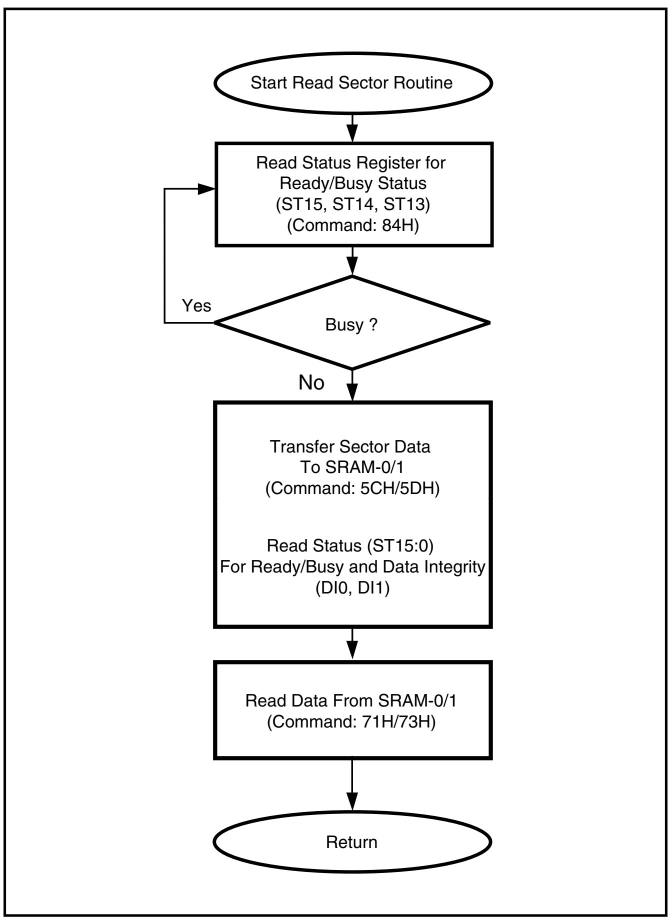


Figure 7. Read data from sector

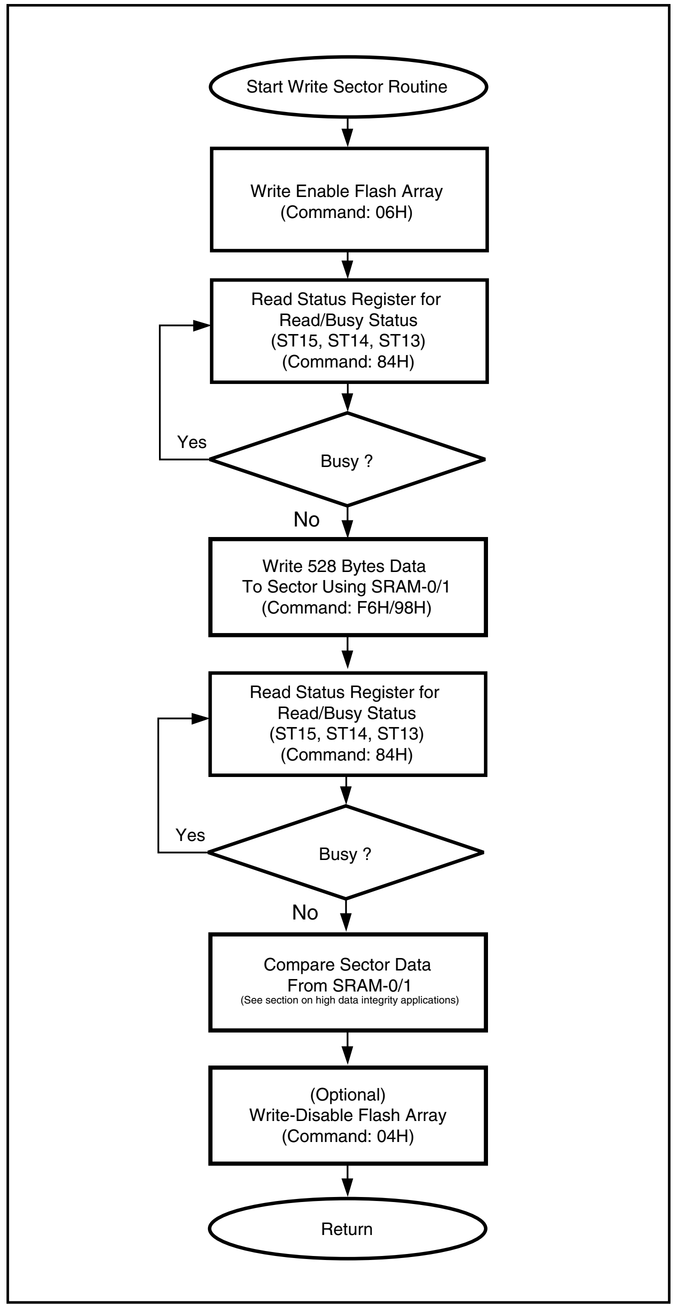


Figure 8. Write data to sector (Erase + Program)

Table 3 Command Set for the NX25F080/160/320C Serial Flash Memory (3)

Command Name	Byte 1	Byte 2-3	Byte 4-5 or n-bytes			
Sector and SRAM Read Commands						
Transfer Sector to SRAM-0 (2)	5CH	SA15:0	0000H	0000H	ST15:0 (4)	
Transfer Sector to SRAM-1 (2)	5DH	SA15:0	0000H	0000H	ST15:0 (4)	
Read SRAM-0 (1)	71H	BA15:0	00H	Read Data		
Read SRAM-1 (1)	73H	BA15:0	00H	Read Data		
Read from Sector with Auto Increment (2)(5)	50H	SA15:0	BA15:0	0000H	RB15:0	Read Data (multiple sectors)
Sector and SRAM Write Commands						
Write Enable (1)	06H					
Write Disable (1)	04H					
Write Sector using SRAM-0 (2)	F6H	SA15:0	BA15:0	Write Data+00H		
Write Sector using SRAM-1 (2)	98H	SA15:0	BA15:0	Write Data+00H		
Write to SRAM-0 (1)	72H	BA15:0	Write Data+00H			
Write to SRAM-1 (1)	74H	BA15:0	Write Data+00H			
Compare, Transfer and Refresh Commands						
Compare Sector to SRAM-0 (2)	8DH	SA15:0	0000H			
Compare Sector to SRAM-1 (2)	8EH	SA15:0	0000H			
Transfer SRAM-0 to Sector (2)	F6H	SA15:0	0000H			
Transfer SRAM-1 to Sector (2)	98H	SA15:0	0000H			
Transfer SRAM-0 to SRAM-1 (2)	92H	0000H	0000H	0000H		
Transfer SRAM-1 to SRAM-0 (2)	55H	0000H	0000H	0000H		
Refresh Sector using SRAM-0 (2)	58H	SA15:0	0000H	0000H		
Refresh Sector using SRAM-1 (2)	59H	SA15:0	0000H	0000H		
Configuration and Status Commands						
Read Device Information Sector (2)	15H	0000H	BA15:0	0000H	RB15:0	Read Data
Read Configuration Register (1)	8CH	CF15:0				
Write Configuration Register (1)	8AH	CF15:0	0000H			
Read Status Register (1)	84H	ST15:0				
Clear Power Down Bit (1)	09H					
Set Power Down Bit (1)	03H					

Key:
SA = Sector Address, BA = Byte Address, RB = Read/Busy, CF = Configuration Register, ST = Status Register

Notes:
1. Command may be used when device is busy
2. Command may not be used when device is busy
3. Additional commands such as Auto Incrementand other commands offering compatibility with earlier generation NexFlash devices are available. Contact NexFlash for further information.
4. ST15:0 status repeats every 16 Clocks
5. This command is for low cycle-endurance applications only. (Contact NexFlash for further information)

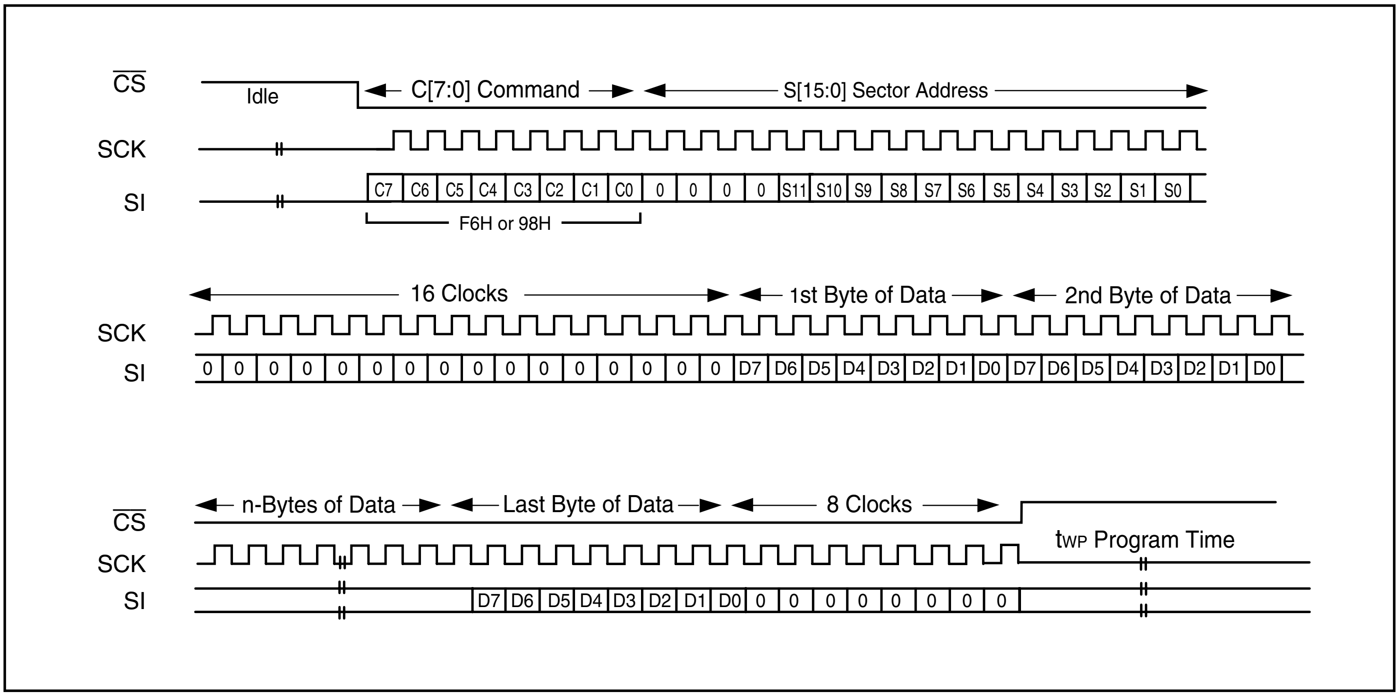


Figure 9. Write to Sector using SRAM Command Sequence

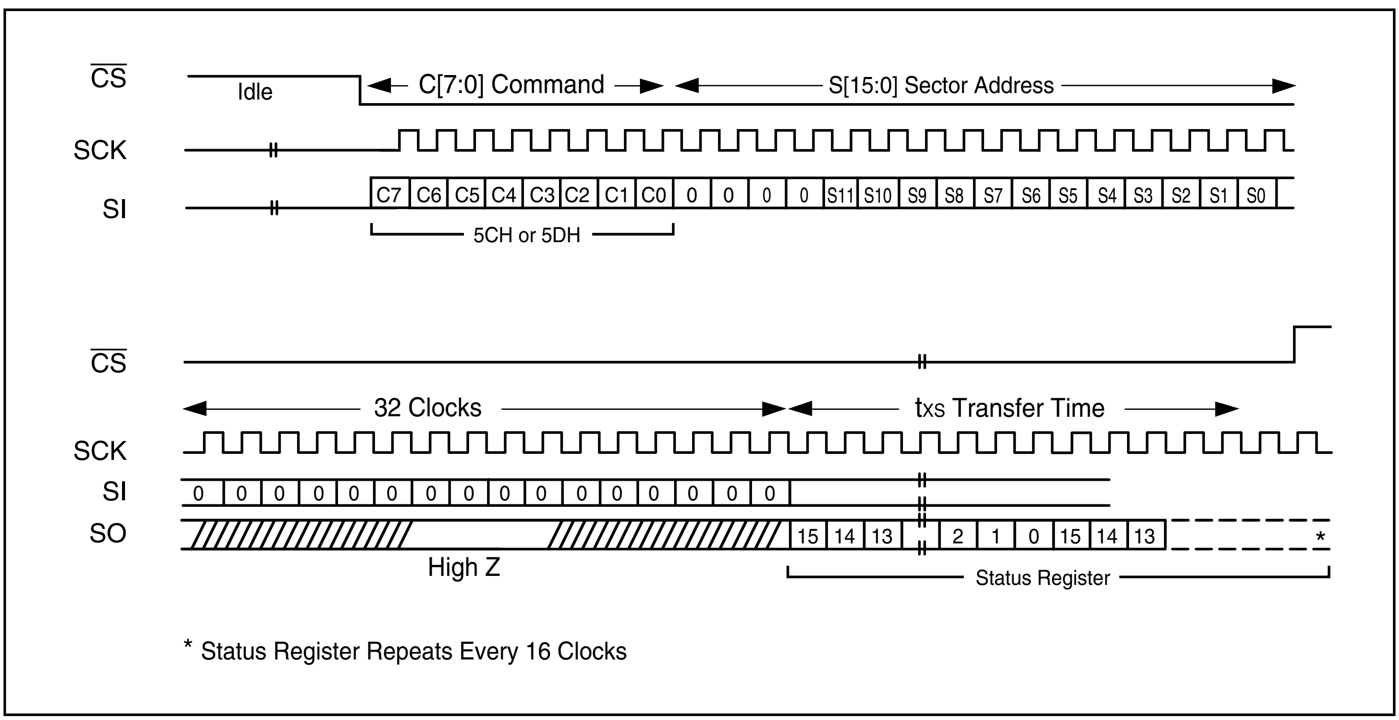


Figure 10. Transfer Sector to SRAM Command Sequence

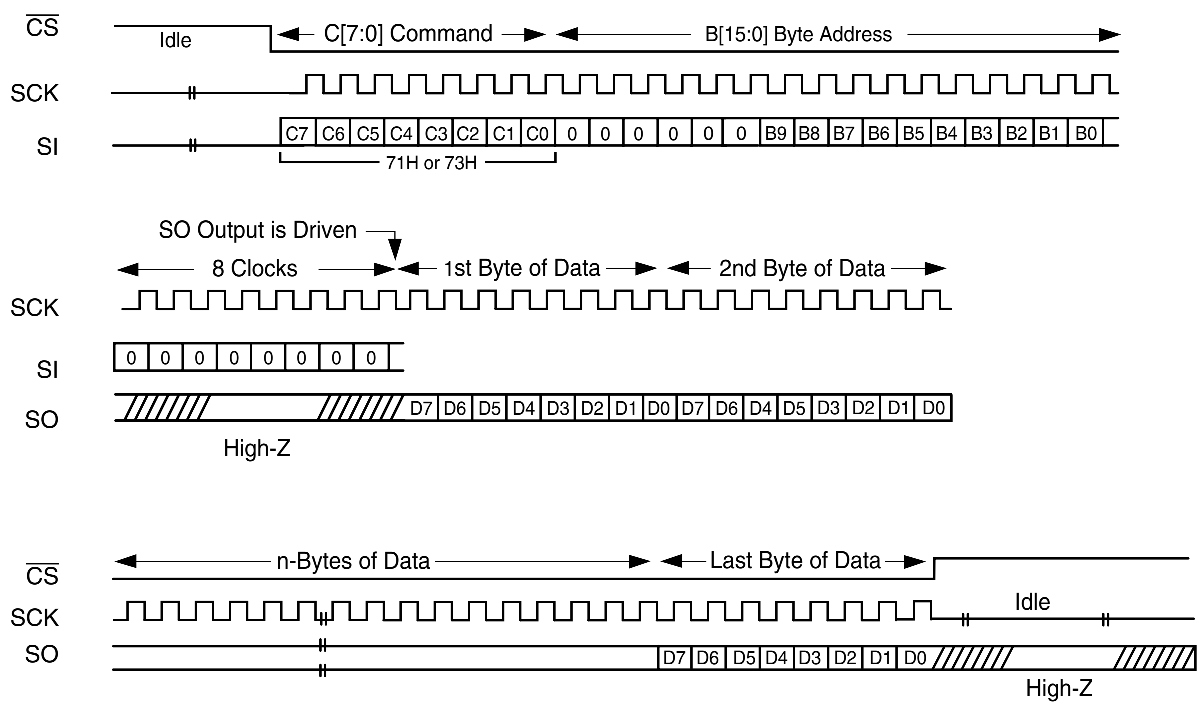


Figure 11. Read from SRAM Command Sequence

SERIAL FLASH SECTOR AND SRAM READ COMMANDS

Transfer Sector to SRAM (5CH and 5DH)

The *Transfer Sector to SRAM* command transfers the contents of a specified 528-byte sector directly to the SRAM. Writing to a sector is accomplished by first bringing $\overline{CS}$ low and shifting in the *Transfer Sector to SRAM* command (53H and 5DH) followed by a 16-bit "sector-address" field. Although the sector-address field is 16-bits, only bits Bits S[10:0] for NX25F080C, S[10:0] FOR NX25F080C, S[11:0] FOR NX25F160C AND S[12:0] FOR NX25F320C for NX25F160C and S[12:0] for NX25F320C are used. The uppermost sector address bits are not used but must be clocked in (use 0 data). Following the sector address, a 32-bit "0" field is clocked into the device. The transfer operation will start and the Busy and TR bit in the status register will be set. The Status Register bits ST[15:0] are then provided on the SO output every 16 clocks. This feature allows the Busy and TR bit in the status register to be checked without sending a separate Status Register command. When the transfer operation is complete the Busy and TR bits in the status register will be cleared and the Data Integrity bits DI0 and DI1 can be checked to confirm that data is valid.

Read SRAM (71H and 73H)

The *Read SRAM* command (71H and 73H) provides access to the 528-byte SRAM independent of any Flash memory array operations. The TR bit in the status register should be checked first if *Transfer Sector to SRAM* or *Compare Sector to SRAM* commands are used. Reading from the SRAM is accomplished by first bringing $\overline{CS}$ low then shifting in the *Read SRAM* command (71H or 73H) followed by its 16-bit "byte-address" field is clocked into the device to designate the starting location within the 528-byte sector. Only B[9:0] of the byte-address field are used; the uppermost bits are not used but must be clocked in (use 0 for data). Only byte-addresses of 0 to 209H (528 bytes) are valid. Following the byte-address field, 8 control clocks are required with data=0. The Serial Data Output (SO) will change from a high-impedance state and begin to drive the output. If SO uses the rising edge of clock (configuration register RCE=1), the output will be driven after the last control clock. If SO uses the falling edge of clock (RCE=0), the output will be driven on the next falling edge of clock. The data field is shifted out with the least significant byte first (i.e., byte-00H, byte-01H, ...). The bit order within each byte is the most significant bit first (i.e.,D7,...D0). The byte-address is internally incremented to the next higher byte address as the clock continues.

Read Sector with Auto-Increment (50H)

For applications that require a continuous serial stream of data, such as downloading code into SRAM or DRAM upon power-up, a Read Sector with Auto Increment (50H)command is provided. This command allows the data from and entire device or a large numbers of sectors to be read with a single command. When the clock reaches the end of a sector it automatically increments to the next and so on. This command is for low cycle-endurance applications only, contact NexFlash for further information.

SERIAL FLASH SECTOR AND SRAM WRITE COMMANDS

Write Enable (06H)

Upon power-up, the Flash memory array is write- protected until the *Write Enable* command (06H) has been issued. The $\overline{WP}$ pin must be inactive while writing the command for the write enable to be accepted. The status of the device's write protect state can be read in the status register. The *Write Enable* command sequence is completed by asserting $\overline{CS}$ high after eight additional clocks.

Write Disable (04H)

The *Write Disable* command (04H) protects the Flash memory array from being programmed. Once issued, further *Write to Sector* or *Transfer SRAM to Sector* commands will be ignored. The status of the write protect state can be read in the status register. The *Write Disable* command sequence is completed by asserting $\overline{CS}$ high after eight additional clocks.

Write to Sector Using SRAM (F6H or 98H)

Before writing to a sector in the Flash memory array, all hardware and software write protection must be in an enabled state. This means that the $\overline{WP}$ pin must be in a high state, a *Write Enable* command must have previously been issued, and the sector location that is to be written to must be outside the write protect range set in the configuration register. Additionally, the Ready/Busy status should be checked to confirm that the memory array is available to be written to, refer to figures 8 and 12 for block diagram.

Writing to a sector is accomplished by first bringing $\overline{CS}$ low and shifting in the *Write to Sector* Using SRAM command (F6H or 98H) followed by a 16-bit "sector-address" field. Although the sector-address field is 16-bits, only bits S[10:0] for NX25F080C, S[11:0] for NX25F160C and S[12:0] for NX25F320C are used. The uppermost sector address bits are not used but must be clocked in (use 0 data). Following the sector address, a 16-bit "byte-address" field is clocked into the device to designate the starting location within the 528-byte sector. Only bits B[9:0] of the byte-address field are used and only values of 0-209H (528 bytes) are valid.

After the byte-address has been loaded, data is shifted into the 528-byte SRAM, which serves as a temporary storage buffer. Existing data in the SRAM will be written over. The byte order of the data shifted into the SRAM is least significant byte first (i.e., byte-00H, byte-01H,...). The bit order within each byte is most significant bit first (i.e., D7,...D0). The byte-address is automatically incremented to the next higher byte address as the clock continues. When the last byte address to be written is reached, the command can be completed with an additional eight control clocks (with data=0) followed by asserting $\overline{CS}$ high.

After the $\overline{CS}$ pin is brought high, the data in the SRAM is transferred to the specified sector in memory array. See t_{WP} timing specifications. During this time the array and SRAM will be "busy" and will ignore further array-related commands until complete. All Ready/Busy status indicators will indicate a busy status.

Write to SRAM Command (72H and 74H)

The *Write to SRAM* command (72H and 74H) provides access to the 528-byte SRAM independently of any Flash memory array operation. When $\overline{CS}$ is asserted high to complete the command, the contents of the SRAM will be maintained until overwritten through another command or the power is removed. Using the *Write to SRAM* command, data can be loaded in preparation of writing to a sector in memory and then transferred to a selected sector using the *Transfer SRAM to Sector* command. The TR bit in the status register should be checked first if *Transfer Sector to SRAM* or *Compare Sector to SRAM* commands are used.

COMPARE, TRANSFER AND REFRESH COMMANDS

Compare Sector to SRAM (8DH and 8EH)

The *Compare Sector to SRAM* command (8DH and 8EH) does a bit-by-bit comparison of the data stored in the addressed sector against data in the SRAM. The TR bit will be 1 during the transfer compare operation. If any of the compared bits are not equal, then the *Compare Not Equal* (CNE) bit in the Status Register is set to a 1. This command is very useful for performing a fast verify of the Last Sector write operation for the highest data integrity.

Transfer SRAM to Sector (F6H and 98H)

The *Transfer SRAM to Sector* command (F6H and 98H) will write the existing contents of the SRAM to the specified sector in memory. The command sequence is identical to that of the *Write to Sector Using SRAM* command except that immediately after the sector address field S[15:0] and 16 control clocks, the $\overline{CS}$ pin is asserted high. This automatically transfers the 528-bytes of SRAM data to the specified sector in the memory array. During this time, the array and the SRAM will be busy.

Refresh Sector Using SRAM (58H and 59H)

The *Refresh Sector Using SRAM* command (58H and 59H) will automatically transfer the contents of the specified sector into the SRAM and then re-write the data to the same sector. The purpose of this command is to refresh the data for all sectors within the same block of 64 sectors to enhance data integrity and cycle endurance. The Refresh sector command should be used in accordance with the Data Integrity Status bit in the status register. During this command the array and the SRAM will be busy.

CONFIGURATION AND STATUS COMMANDS

Read Device Information Sector (15H)

The *Read Device Information* command provides access to a read-only sector that can be used to electronically identify the *NexFlash* Serial Flash device being interfaced to. Information available includes: part number, density, voltage, temperature range, package type, and any special options. This can be extremely useful for systems that need to accommodate optional densities (e.g., either 8M,16M or 32M-bit). In this case the firmware can interrogate the Device Information Sector and determine the density. Contact *NexFlash* for more detailed information on the Device Information Sector format.

Read Configuration Register (8CH)

The *Read Configuration Register* command provides access to the configuration register, which stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read clock edge, write protect range (see figure 5). A 16-bit Configuration Data field CF[15:0] provides the contents of the Configuration Register. Although the field is 16-bits long, only bits CF[7:0] are used. All other upper bits are reserved for future features.

Write Configuration Register (8AH)

The *Write Configuration Register* command provides access to the configuration register which stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read-data clock edge and write protect range. The configuration register is non-volatile. Once set using the *Write Configuration Register* command, the contents will maintain even when power is removed. Because the register's state is stored in non-volatile memory, there is a finite endurance limit to the number of times it can be written to. To limit the number of writes, it is recommended that before writing to the configuration register it should first be read by using the *Read Configuration Register* command. If no change is required, the *Write Configuration Register* command can be skipped. This process will help extend the endurance of the configuration register bits and eliminate additional programming "busy" time.

The *Write Configuration Register* command sequence starts with the command byte (8AH) followed by a 16-bit field that specifies configuration register bit settings. Although the field is 16-bits long, only bits CF[7:0] are used. All other upper bits are reserved and must be clocked using 0 for data. After an additional 16 control clocks using 0 for data, the command can be completed by asserting CS high. The device will become busy for a short time (t_{WP}) while the non-volatile memory cells of the configuration register are programmed.

Read Status Register (84H)

The *Read Status Register* command provides access to the status register and its status flags for Ready/Busy (R/B), SRAM buffer transfer operations (TR0 and TR1), Write Enable/Disable (WE), and Compare Not Equal (CNE), Power Detect and Data Integrity bits (Figure 6). An 16-bit Status field ST[15:0] provides the contents of the Status Register.

Clear Power Detection Bit (09H)

The *Reset Power Detection Bit* command (09H) can be used to force the Power Detect Status bit in the status register to a 0 state. (see Set Power Detection Bit command (03H).

Set Power Detection Bit (03H)

The *Set Power Detection Bit* command (03H) can be used to detect if power has been removed from the device. The command works in conjunction with the Power Detect (PD) status bit. Upon power up the PD bit is cleared to 0. The PD bit can be set to a 1 using the *Set Power Detection Bit* command. Once set, if a power down condition occurs (Vcc voltage < 2V) the PD bit will reset to 0. This function is especially useful for applications using *NexFlash* Serial Flash Modules or other removable media.

Command Compatibility with Earlier Generation NexFlash Products

The NX25F080/160/320C supports additional commands for compatibility with earlier generation NexFlash products such as the NX25FxxxB-series (see Table 4). This command table should only be used if command compatibility is required. The Erase/Write cycle endurance when using these commands may be less the standard command set in Table 3. Contact NexFlash Marketing and Applications department for further information

Table 4. Command Set for Compatibility with NexFlash "B-Series" Serial Flash Memories. (3)

Command Name	Byte 1	Byte 2-3	Byte 4-7 or n-bytes			
Sector and SRAM Read Commands						
Transfer Sector to SRAM-0 (2)	53H	SA15:0	0000H	0000H	ST15:0	
Transfer Sector to SRAM-1 (2)	56H	SA15:0	0000H	0000H	ST15:0	
Read SRAM-0 (1)	71H	BA15:0	00H	Read Data		
Read SRAM-1 (1)	73H	BA15:0	00H	Read Data		
Read from Sector with Auto Increment (2)	50H	SA15:0	BA15:0	0000H	RB15:0	Read Data (multiple sectors)
Read from Sector (2)	52H	SA15:0	0000H	0000H	RB15:0	Read Data (one sector)
Sector and SRAM Write Commands						
Write Enable (1)	06H					
Write Disable (1)	04H					
Write Sector using SRAM-0 (2)	F3H	SA15:0	0000H	Write Data + 00H		
Write Sector using SRAM-1 (2)	94H	SA15:0	0000H	Write Data + 00H		
Write to SRAM-0 (1)	72H	BA15:0	Write Data + 00H			
Write to SRAM-1 (1)	74H	BA15:0	Write Data + 00H			
Compare, Transfer and Refresh Commands						
Compare Sector to SRAM-0 (2)	8DH	SA15:0	0000H			
Compare Sector to SRAM-1 (2)	8EH	SA15:0	0000H			
Transfer SRAM-0 to Sector (2)	F3H	SA15:0	0000H			
Transfer SRAM-1 to Sector (2)	94H	SA15:0	0000H			
Transfer SRAM-0 to SRAM-1 (2)	92H	0000H	0000H	0000H		
Transfer SRAM-1 to SRAM-0 (2)	56H	0000H	0000H	0000H		
Refresh Sector using SRAM-0 (2)	58H	SA15:0	0000H	0000H		
Refresh Sector using SRAM-1 (2)	59H	SA15:0	0000H	0000H		
Configuration and Status Commands						
Read Device Information Sector (2)	15H	SA15:0	BA15:0	0000H	RB15:0	Read Data
Read Configuration Register (1)	8CH	CF15:0				
Write Configuration Register (1)	8AH	CF15:0	0000H			
Read Status Register (1)	84H	ST15:0				
Clear Power Down Bit (1)	09H					
Set Power Down Bit (1)	03H					

Key:
SA = Sector Address, BA = Byte Address, RB = Read/Busy, CF = Configuration Register, ST = Status Register

Notes:
1. Command may be used when device is busy
2. Command may not be used when device is busy
3. Sector Write and Transfer to Sector commands from this table are to be used for Auto Increment Read operation and other low cycle-endurance applications. (Contact NexFlash

Sector Format and Tag/Sync Bytes

The first byte of each sector is pre-programmed during manufacturing with a tag/sync value of C9H. Although this byte location of the sector can be changed, it is recommended that it be maintained and incorporated into the application's sector formatting. The tag/sync values serve two purposes. First, they provide a sync-detect that can help verify if the command sequence was clocked into the device properly. Secondly, they serve as a tag to identify a fully functional (valid) sector. This is especially important if "restricted sector" (-R) devices are ever to be used. Restricted sector devices provide a more cost effective alternative to standard devices with 100% valid sectors. Restricted sector devices have a limited number of sectors that do not meet manufacturing programming criteria over the specified operating range. When such a sector is detected, the first byte is tagged with a pattern other than C9H. In addition to individual sector tagging, all restricted sectors for a given device are listed in the Device Information Sector. For more information see the Device Information Sector Application Note SFAN-02.

High Data Integrity Applications

To maximize data integrity a simple "verification after write" is recommended. The write verify can be done quickly (less than t_{XS}) using the Compare Sector command. The compare result can be checked in the Status Register. If compare is not equal (CNE=1) then a sector rewrite should be done using the Transfer SRAM to Sector command. A single retry is adequate for most applications. However, if an application requires extended endurance additional retrys can be added.

In the NX25F080/160/320C a data block is every 64 sectors starting from sector 0; that is, block 0 is sector 0-63, block 1 is sector 64-127 and so on. For the highest data integrity, it is important to separate static data (configuration settings, tables) and frequently updated data (streaming voice/image or data acquisition) into separate blocks. Following this convention optimizes the environment for the data stored in the flash cells within each block.

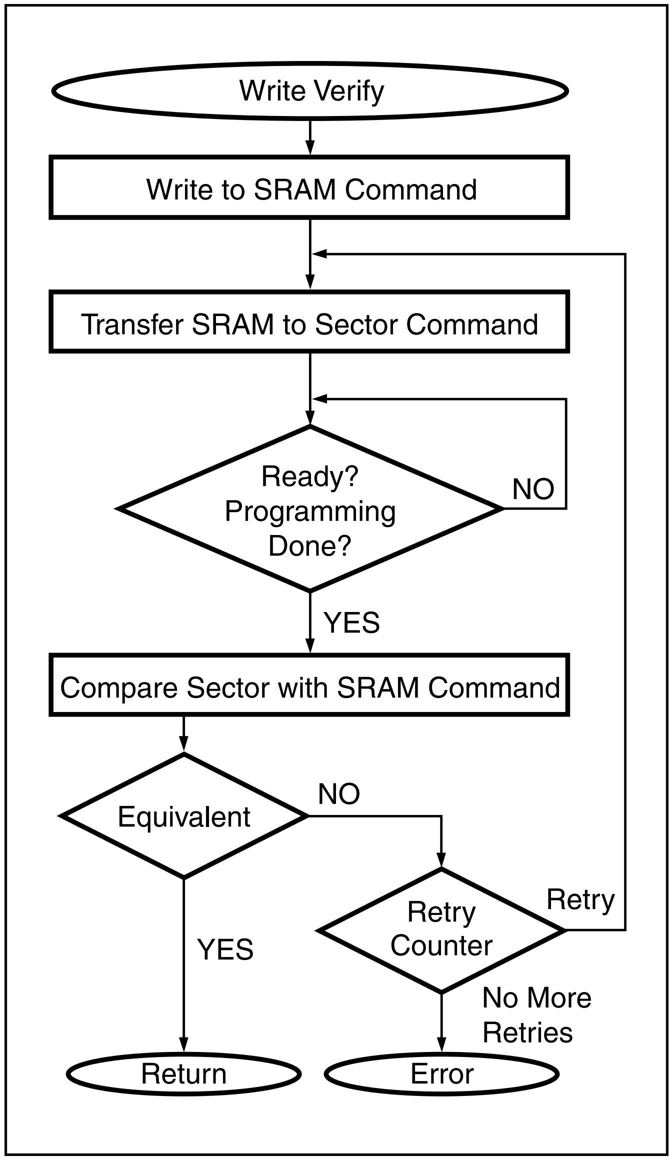


Figure 12. Write/Verify Flow

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		0 to +4.0	V
V_{IN}, V_{OUT}	Voltage Applied to Any Pin	Relative to Ground	–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to +150	˚C
T_{LEAD}	Lead Temperature	Soldering 10 Seconds	+300	˚C

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.

OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	3.0V	2.7	3.6	V
T_A	Ambient Temperature, Operating	Commercial	0	70	°C
		Industrial	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (PRELIMINARY)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.4	—	Vcc 0.2	V
V_{IH}	Input High Voltage		Vcc –0.7	—	Vcc +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 2.7V	—	—	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = 2.7V	Vcc –0.85	—	—	V
V_{OLC}	Output Low Voltage CMOS	V_{CC} = 2.7V, I_{OL} = 10 µA	—	—	0.15	V
V_{OHC}	Output High Voltage CMOS	V_{CC} = 2.7V, I_{OH} = –10 µA	V_{CC} –0.3	—	—	V
I_{IL}	Input Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{OL}	I/O Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Erase/Write	—	2.5	5	mA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Read	—	5	10	mA
I_{CCSB} (standby)	Standby Vcc Supply Current	CS = V_{CC}, V_{IN} = Vcc or 0 Standby	—	<1	10	µA
C_{IN}	Input Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF
C_{OUT}	Output Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF

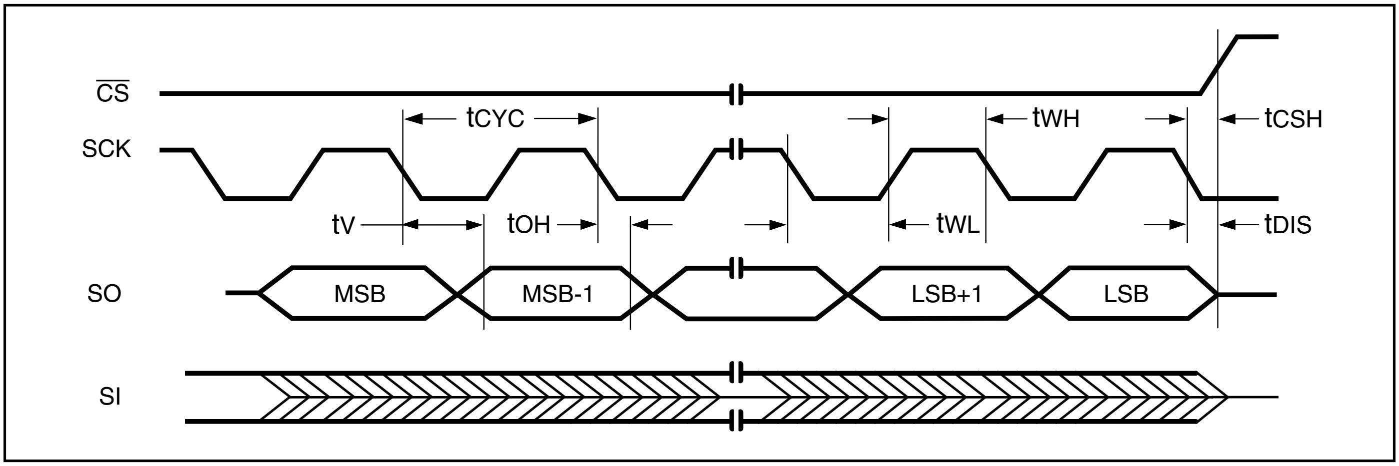
Note:
1. Tested on a sample basis or specified through design or characterization data.

AC ELECTRICAL CHARACTERISTICS (PRELIMINARY)

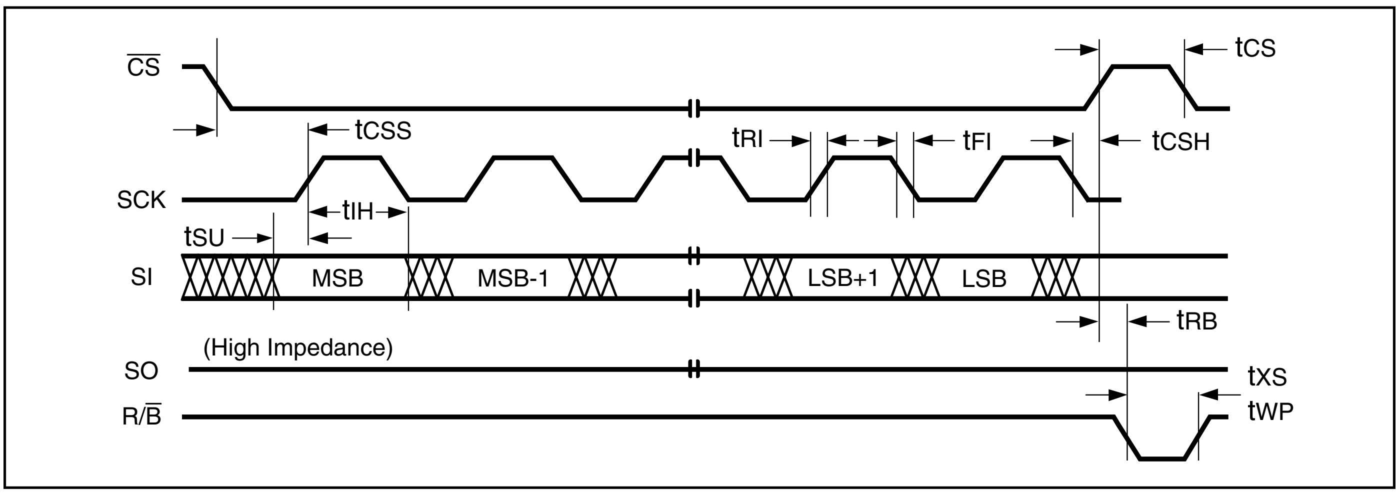
Symbol	Description	16 MHz Min	Typ	Max	Unit
t_{CYC}	SCK Serial Clock Period With RCE=1 SCK Serial Clock Period With RCE=0 (1)	62 77	— —	— —	ns ns
t_{WH} t_{WL}	SCK Serial Clock High or Low Time	$t_{CYC}/2$	—	—	ns
t_{RI} t_{FI}	SCK Serial Clock Rise or Fall Time (2)	—	—	5	ns
t_{SU}	Data Input Setup Time to SCLK	20	—	—	ns
t_{IH}	Data Input Hold Time from SCLK	0	—	—	ns
t_V	Data Output Valid after SCLK (1,3)	—	—	25	ns
t_{LEAD}	$\overline{CS}$ Setup Time to Command	100	—	—	ns
t_{LAG}	$\overline{CS}$ Delay Time after Command	100	—	—	ns
t_{WP}	Erase/Write Program Time (4) *(see Write to Sector Command)*	—	10	15	ms
t_{XS}	Transfer Sector *(see Transfer Command)*	100	150	520	µs
t_{HD}	SCK Setup Time to $\overline{HOLD}$	10	—	—	ns
t_{CD}	SCK Hold Time from $\overline{HOLD}$	30	—	—	ns
t_{CS}	$\overline{CS}$ Deselect Time	160	—	—	ns
t_{RB}	READY / BUSY Valid Time	160	—	—	ns
t_{DIS}	Data Output Disable Time	—	—	160	ns
t_{OH}	Data Output Hold Time After SCK	0	—	—	ns

Notes:
1. To achieve maximum clock performance, the read clock edge will need to be set for rising edge operation in the configuration register (RCE=1).
2. Test points are 10% and 90% points for rise/fall times. All others timings are measured at 50% point.
3. With 30 pF (16 MHz) load SO to GND.
4. Maximum program time for 99% of sectors, <1% may require 4x this value.

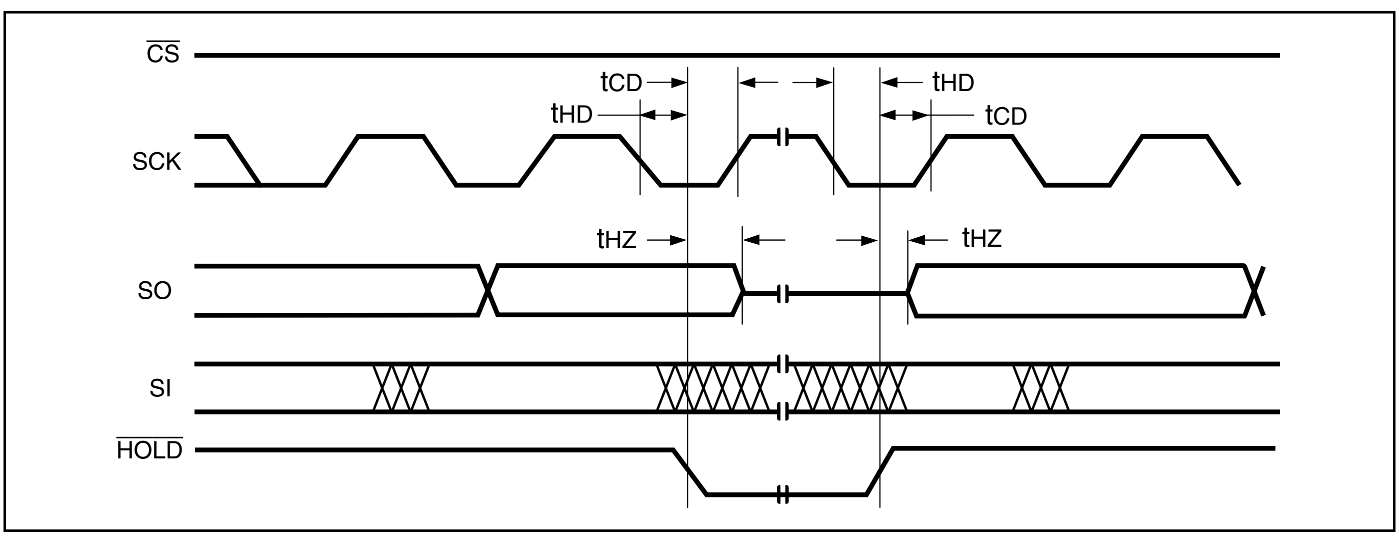
SERIAL OUTPUT TIMING



SERIAL INPUT TIMING

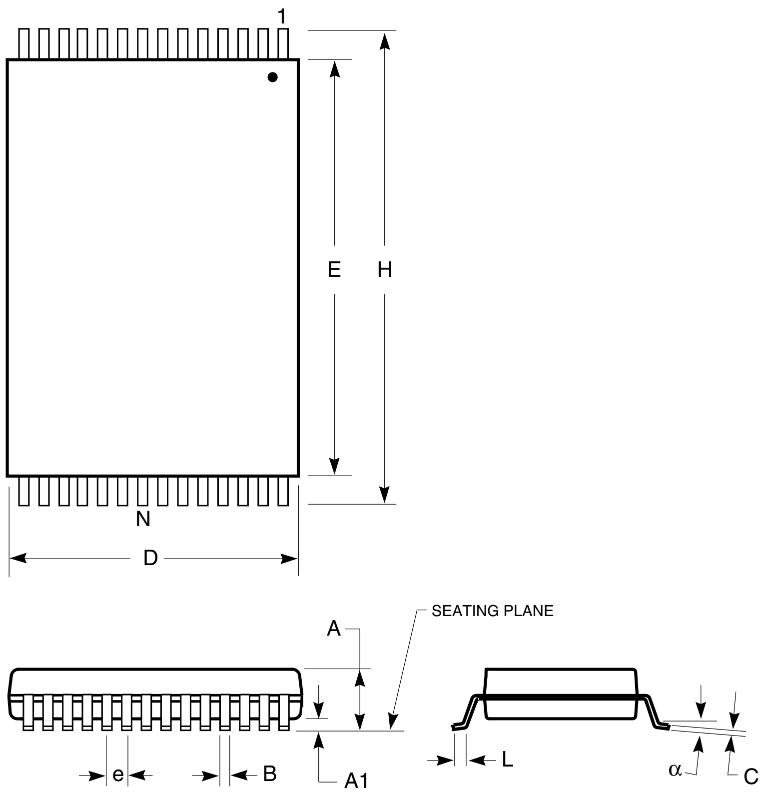


HOLD TIMING



PACKAGING INFORMATION

Plastic TSOP - 28-pins
Package Code: T (Type I)



Plastic TSOP Type I (V)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
No. Leads		28		
A	1.00	1.20	0.039	0.047
A1	0.05	0.20	0.002	0.008
B	0.15	0.25	0.006	0.010
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.311	0.319
E	11.60	11.80	0.457	0.465
H	13.30	13.50	0.524	0.531
e	0.55 BSC		0.022 BSC	
L	0.50	0.70	0.020	0.028
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PRELIMINARY DESIGNATION

The "Preliminary" designation on an *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

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(a) the risk of injury or damage has been minimized;

(b) the user assumes all such risks; and

(c) potential liability of *NexFlash* is adequately protected under the circumstances.

Trademarks:

ORDERING INFORMATION

Size	Order Part No.	Package
8M-bit	NX25F080C-3V	SPI, 28-pin, TSOP, 3V
16M-bit	NX25F160C-3V	SPI, 28-pin, TSOP, 3V
32M-bit	NX25F320C-3V	SPI, 28-pin, TSOP, 3V

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