NTP8N50, NTB8N50

Preferred Device

Advance Information

Power MOSFET
8 Amps, 500 Volts
N–Channel TO–220 and D^{2}PAK

Designed for high voltage, high speed switching applications in power supplies, converters, power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specifications
- Avalanche Energy Specified

Typical Applications

- Switch Mode Power Supplies
- PWM Motor Controls
- Converters
- Bridge Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage – Continuous – Non–Repetitive ($t_p \le 10$ ms)	 V_{GS} V_{GSM}	 ±20 ±40	Vdc
Drain – Continuous – Continuous @ 100°C – Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 8.0 6.2 28	Adc
Total Power Dissipation Derate above 25°C	P_D	202 1.61	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 8 A, L = 10 mH, R_G = 25 Ω)	E_{AS}	320	mJ
Thermal Resistance – Junction–to–Case – Junction–to–Ambient – Junction–to–Ambient (Note 1.)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 0.62 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor™

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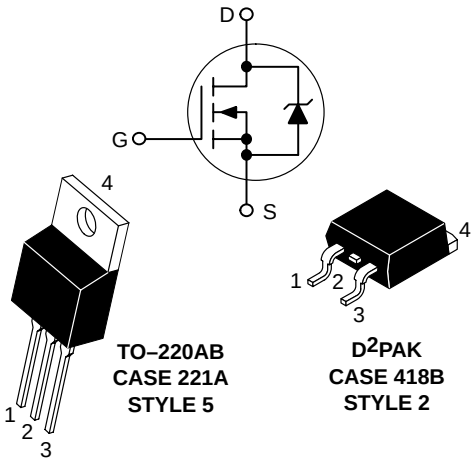
8 AMPERES
500 VOLTS
$R_{DS(on)}$ = 750 mΩ

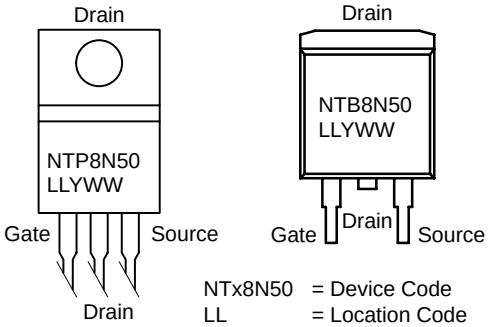
N–Channel



TO–220AB
CASE 221A
STYLE 5

D^{2}PAK
CASE 418B
STYLE 2

MARKING DIAGRAMS AND PIN ASSIGNMENTS



NTx8N50 = Device Code
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTP8N50	TO–220AB	50 Units/Rail
NTB8N50	D^{2}PAK	50 Units/Rail
NTB8N50T4	D^{2}PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

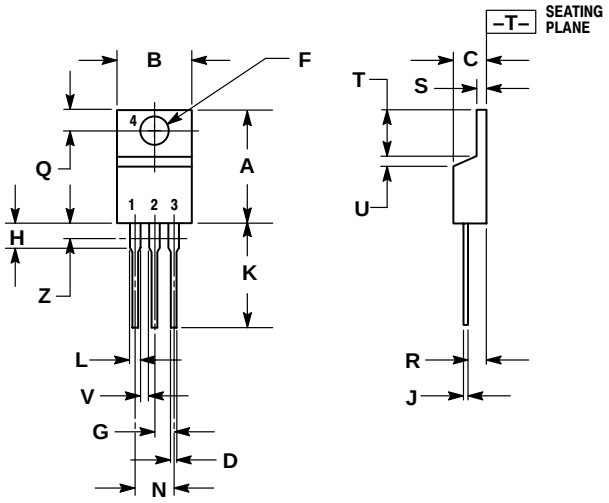
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)	$V_{(BR)DSS}$	500	–	–	Vdc
Temperature Coefficient (Positive)		–	560	–	mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	–	–	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J =125°C)		–	–	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)	$I_{GSS(f)}$	–	–	100	nAdc
	$I_{GSS(r)}$	–	–	100	
ON CHARACTERISTICS (Note 2.)					
Gate Threshold Voltage (I_D = 0.25 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	2.0	2.6	4.0	Vdc
Temperature Coefficient (Negative)		–	6.5	–	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	$R_{DS(on)}$	–	600	750	mOhm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 8.0 Adc)	$V_{DS(on)}$	–	–	7.2	Vdc
(V_{GS} = 10 Vdc, I_D = 4.0 Adc, T_J = 125°C)		–	–	6.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 4.0 Adc)	g_{FS}	4.0	7.0	–	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	–	1530	2140	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	–	380	530	
Transfer Capacitance	C_{rss}	–	15	30	
SWITCHING CHARACTERISTICS (Note 3.)					
Turn–On Delay Time	$t_{d(on)}$	–	14	30	ns
Rise Time (V_{DD} = 250 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	t_r	–	17	30	
Turn–Off Delay Time	$t_{d(off)}$	–	34	70	
Fall Time	t_f	–	25	50	
Gate Charge	Q_T	–	25	40	nC
(V_{DS} = 400 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc)	Q_1	–	6.0	–	
	Q_2	–	8.0	–	
	Q_3	–	12	–	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (Note 2.) (I_S = 8.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	–	0.9	1.1	Vdc
(I_S = 8.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		–	0.8	–	
Reverse Recovery Time	t_{rr}	–	375	–	ns
(I_S = 8.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_a	–	155	–	
	t_b	–	220	–	
Reverse Recovery Stored Charge	Q_{RR}	–	2.75	–	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from contact screw on tab to center of die)	L_D	–	3.5	–	nH
(Measured from the drain lead 0.25″ from package to center of die)		–	4.5	–	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	–	7.5	–	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA

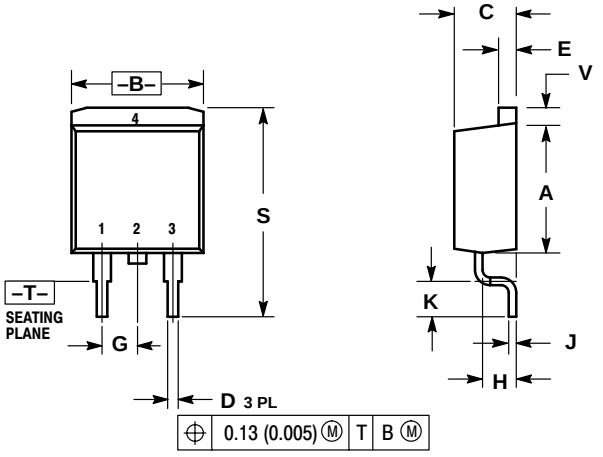


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

D^2PAK
CASE 418B–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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