Power MOSFET 75 Amps, 60 Volts, Logic Level

N-Channel TO-220 and D2PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	VDSS	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 10 M Ω)	VDGR	60	Vdc
Gate–to–Source Voltage – Continuous – Non–Repetitive (t _p ≤10 ms)	V _{GS} V _{GS}	±20 ±15	Vdc
Drain Current - Continuous @ $T_A = 25^{\circ}C$ - Continuous @ $T_A = 100^{\circ}C$ - Single Pulse ($t_p \le 10 \mu s$)	I _D	75 50 225	Adc Apk
Total Power Dissipation @ T _A = 25°C Derate above 25°C Total Power Dissipation @ T _A = 25°C (Note 1.)	PD	214 1.4 2.4	W W/°C W
Operating and Storage Temperature Range	TJ, T _{stg}	-55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ($V_{DD} = 50$ Vdc, $V_{GS} = 5.0$ Vdc, $L = 0.3$ mH $I_{L(pk)} = 75$ A, $V_{DS} = 60$ Vdc)	EAS	844	mJ
Thermal Resistance – Junction–to–Case – Junction–to–Ambient (Note 1.)	R _θ JC R _θ JA	0.7 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

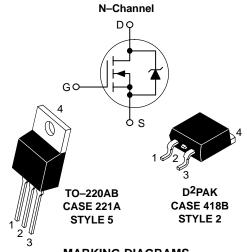
When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).



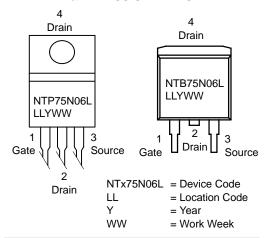
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75 AMPERES 60 VOLTS RDS(on) = 11 m Ω



MARKING DIAGRAMS & PIN ASSIGNMENTS



ORDERING INFORMATION

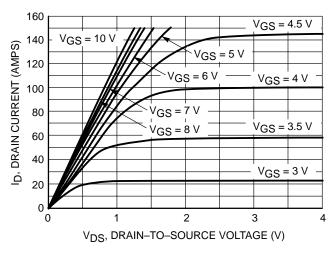
Device	Package	Shipping
NTP75N06L	TO-220AB	50 Units/Rail
NTB75N06L	D ² PAK	50 Units/Rail
NTB75N06LT4	D ² PAK	800/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_{.J} = 25°C unless otherwise noted)

	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdowr (VGS = 0 Vdc, ID = 250 µ/ Temperature Coefficient (Pos	V(BR)DSS	60 -	72 74	_ _	Vdc mV/°C	
Zero Gate Voltage Drain Cur (V _{DS} = 60 Vdc, V _{GS} = 0 \ (V _{DS} = 60 Vdc, V _{GS} = 0 \	IDSS	_ _	_ _	10 100	μAdc	
Gate-Body Leakage Current	IGSS	-	-	±100	nAdc	
ON CHARACTERISTICS (Not	e 2.)					
Gate Threshold Voltage (Not (V _{DS} = V _{GS} , I _D = 250 μA Threshold Temperature Coef	VGS(th)	1.0	1.58 6.0	2.0	Vdc mV/°C	
Static Drain-to-Source On- (VGS = 5.0 Vdc, I _D = 37.5	R _{DS(on)}	_	9.0	11	mOhm	
Static Drain-to-Source On- (VGS = 5.0 Vdc, I _D = 75 A (V _{GS} = 5.0 Vdc, I _D = 37.5	VDS(on)		0.75 0.61	0.99	Vdc	
Forward Transconductance	9FS	-	55	-	mhos	
DYNAMIC CHARACTERISTIC	CS					
Input Capacitance		C _{iss}	1	3122	4370	pF
Output Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	Coss	1	1029	1440	
Transfer Capacitance	,	C _{rss}	-	276	390	
SWITCHING CHARACTERIS	TICS (Note 3.)					
Turn-On Delay Time		^t d(on)	_	22	32	ns
Rise Time	(V _{DD} = 30 Vdc, I _D = 75 Adc,	t _r	-	265	370	
Turn-Off Delay Time	$V_{GS} = 5.0 \text{ Vdc}, R_G = 9.1 \Omega) \text{ (Note 2.)}$	td(off)	1	113	160	
Fall Time		t _f	-	170	240	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 75 Adc, V _{GS} = 5.0 Vdc) (Note 2.)	QT	-	66	92	nC
		Q ₁	-	9.0	-	
	100 010 120, (1100 1.)	Q ₂	-	47	-	
SOURCE-DRAIN DIODE CH	ARACTERISTICS					
Forward On–Voltage	$(I_S = 75 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 2.)}$ $(I_S = 75 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$	V _{SD}	_ _	1.0 0.9	1.15 -	Vdc
Reverse Recovery Time	me $(I_S = 75 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, \\ dI_S/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 2.)}$	t _{rr}	_	70	_	ns
		ta	-	43	_	
		t _b	-	27	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.16	-	μС

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

^{3.} Switching characteristics are independent of operating junction temperatures.



160 $V_{DS} \ge 10 \text{ V}$ 140 ID, DRAIN CURRENT (AMPS) 120 100 80 60 40 $T_J = 25^{\circ}C$ 20 $T_{J} = 100^{\circ}C$ 0 1.4 1.8 2.6 3 3.4 3.8 4.2 4.6 5 V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

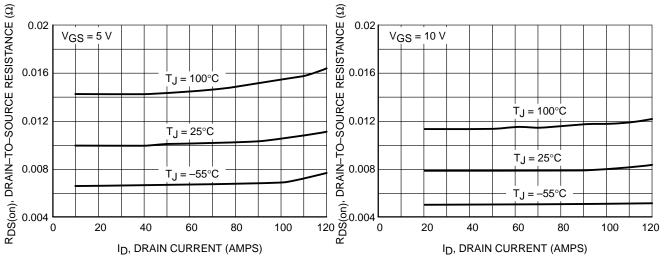
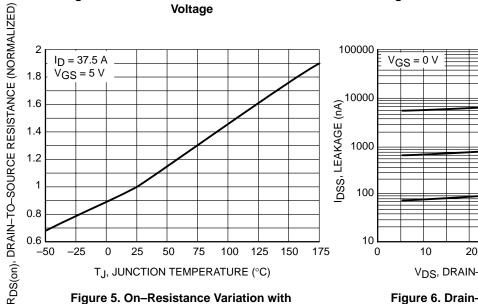


Figure 3. On–Resistance vs. Gate–to–Source Voltage

Figure 4. On–Resistance vs. Drain Current and Gate Voltage



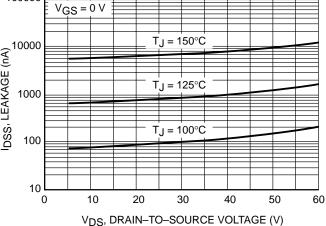


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

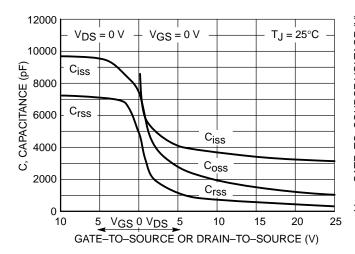


Figure 7. Capacitance Variation

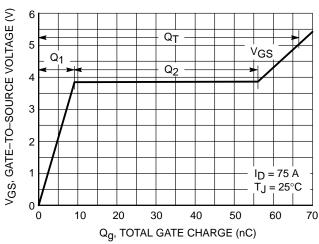


Figure 8. Gate—to—Source and Drain—to—Source Voltage vs. Total Charge

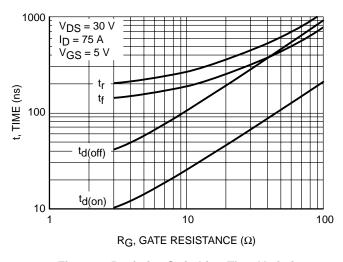


Figure 9. Resistive Switching Time Variations vs. Gate Resistance

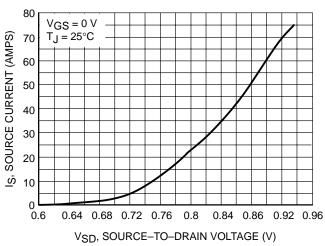


Figure 10. Diode Forward Voltage vs. Current

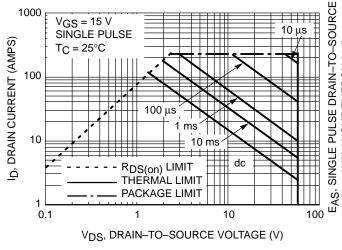


Figure 11. Maximum Rated Forward Biased Safe Operating Area

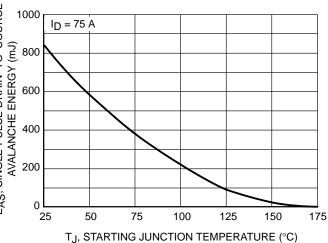


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

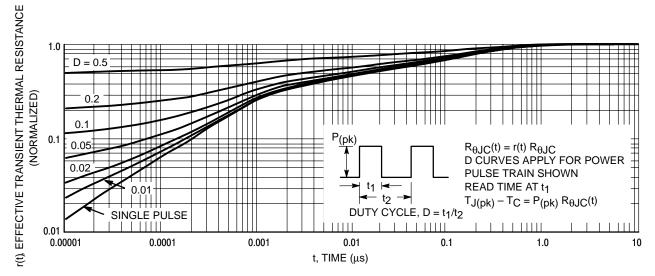
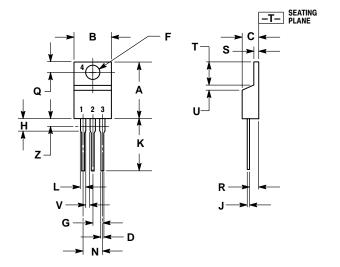


Figure 13. Thermal Response

PACKAGE DIMENSIONS

TO-220 THREE-LEAD TO-220AB

CASE 221A-09 **ISSUE AA**



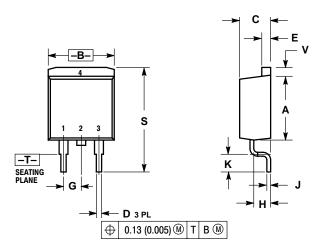
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
7	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
5	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

- STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

PACKAGE DIMENSIONS

D²PAK CASE 418B-03 ISSUE D



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.340	0.380	8.64	9.65
В	0.380	0.405	9.65	10.29
С	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
Е	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
Н	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
v	0.045	0.055	1 1/	1.40

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

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