NTHC5513

Power MOSFET

Complementary, 20 V, +3.1 A / -2.1 A, ChipFET™ Package

This complementary (N and P channel) device was designed with a small footprint package and ON Semiconductor's leading low $R_{DS(on)}$ technology for increased circuit efficiency. The performance is ideally suited for portable or handheld applications.

Features

- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD package Featuring Complementary Pair
- ChipFET Package Provides Great Thermal Characteristics Similar to Larger Packages
- Low $R_{DS(on)}$ in a ChipFET Package for High Efficiency Performance
- Low Profile (< 1.10 mm) Allows Placement in Extremely Thin Environments Such as Portable Electronics

Applications

- Load Switch Applications Requiring Level Shift
- DC-to-DC Conversion Circuits
- Drive Small Brushless DC Motors
- Designed for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	20	V
Gate-to-Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	N-Ch Steady State	T_A = 25°C	I_D	3.1	A
		T_A = 85°C		2.15	
	P-Ch Steady State	T_A = 25°C		-2.1	
		T_A = 85°C		-1.5	
Pulsed Drain Current (Note 1)	N-Ch	t = 10 µs	I_{DM}	10	A
	P-Ch	t = 10 µs		-7.0	
Power Dissipation -Steady State (Note 1)		T_A = 25°C	P_D	1.13	W
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient Steady-State (Note 1)	$R_{\theta JA}$	110	°C/W

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).

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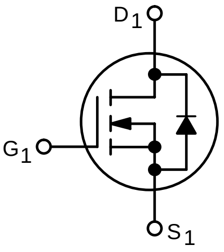
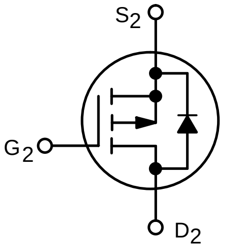
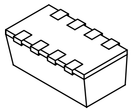
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX (Note 1)
N-Channel 20 V	60 mΩ @ 4.5 V	3.1 A
	80 mΩ @ 2.5 V	
P-Channel -20 V	130 mΩ @ -4.5 V	-2.1 A
	200 mΩ @ -2.5 V	



N-Channel MOSFET

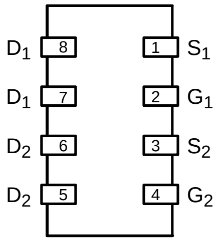


P-Channel MOSFET



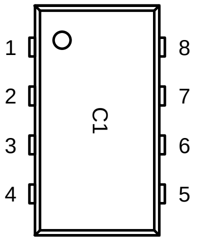
ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



Bottom View

MARKING DIAGRAM



Top View

C1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTHC5513T1	ChipFET	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)								
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = -250 μA	-20			
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V				1.0	μA
		P	V_{GS} = 0 V, V_{DS} = -16 V				-1.0	
		N	V_{GS} = 0 V, V_{DS} = 16 V, T_J = 125 °C				10	
		P	V_{GS} = 0 V, V_{DS} = -16 V, T_J = 125 °C				-10	
Gate-to-Source Leakage Current	I_{GSS}		V_{DS} = 0 V, V_{GS} = ±12 V				±100	nA
ON CHARACTERISTICS (Note 2)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.6		1.2	V
		P		I_D = -250 μA	-0.6		-1.2	
Drain-to-Source On Resistance	$R_{DS}(on)$	N	V_{GS} = 4.5 V , I_D = 3.0 A			0.060	0.080	Ω
		P	V_{GS} = -4.5 V , I_D = -2.1 A			0.130	0.155	
		N	V_{GS} = 2.5 V , I_D = 2.3 A			0.080	0.115	
		P	V_{GS} = -2.5 V, I_D = -1.7 A			0.200	0.240	
Forward Transconductance	g_{FS}	N	V_{DS} = 10 V, I_D = 3.0 A			6.0		S
		P	V_{DS} = -10 V , I_D = -2.1 A			6.0		
CHARGES AND CAPACITANCES								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V	V_{DS} = 10 V		180		pF
		P		V_{DS} = -10 V		185		
Output Capacitance	C_{OSS}	N		V_{DS} = 10 V		80		
		P		V_{DS} = -10 V		95		
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 10 V		25		
		P		V_{DS} = -10 V		30		
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.1 A			2.6	4.0	nC
		P	V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -2.1 A			3.1	6.0	
Gate-to-Source Gate Charge	Q_{GS}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.1 A			0.6		
		P	V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -2.1 A			0.5		
Gate-to-Drain “Miller” Charge	Q_{GD}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.1 A			0.7		
		P	V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -2.1 A			1.1		
SWITCHING CHARACTERISTICS (Note 3)								
Turn-On Delay Time	$t_{d(ON)}$	N	V_{DD} = 16 V, V_{GS} = 4.5 V, I_D = 3.1 A, R_G = 2.5 Ω			5.0	10	ns
Rise Time	t_r					15	30	
Turn-Off Delay Time	$t_{d(OFF)}$					10	20	
Fall Time	t_f					3.0	6.0	
Turn-On Delay Time	$t_{d(ON)}$	P	V_{DD} = -16 V, V_{GS} = -4.5 V, I_D = -2.1 A, R_G = 2.5 Ω			7.0	15	
Rise Time	t_r					13	25	
Turn-Off Delay Time	$t_{d(OFF)}$					33	50	
Fall Time	t_f					27	58	

NOTES:

2. Pulse Test: pulse width ≤ 250 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

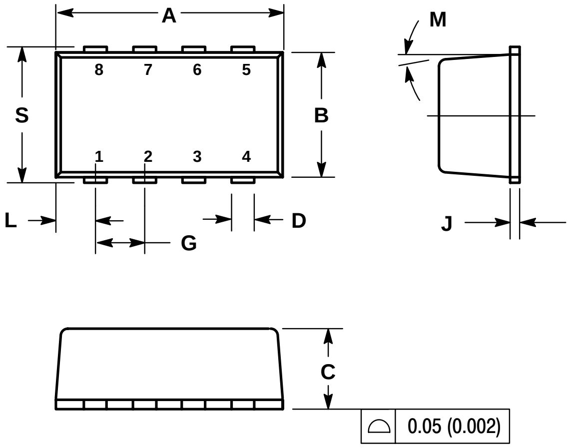
ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage (Note 2)	V_{SD}	N	V_{GS} = 0 V	I_S = 3.1 A		0.8	1.15	V
		P		I_S = -2.1 A		-0.8	-1.15	
Reverse Recovery Time (Note 3)	t_{RR}	N	V_{GS} = 0 V, d_{ISD} / d_t = 100 A/μs	I_S = 1.5 A		12.5		ns
		P		I_S = -1.5 A		12.5		
Charge Time	t_a	N		I_S = 1.5 A		9.0		
		P		I_S = -1.5 A		9.0		
Discharge Time	t_b	N		I_S = 1.5 A		3.5		
		P		I_S = -1.5 A		3.5		
Reverse Recovery Charge	Q_{RR}	N		I_S = 1.5 A		6.0		nC
		P		I_S = -1.5 A		6.0		

NOTES:
2. Pulse Test: pulse width ≤ 250 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

PACKAGE DIMENSIONS

ChipFET
CASE 1206A-03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A–01 AND 1206A–02 OBSOLETE. NEW STANDARD IS 1206A–03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

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