NTB23N03R

Power MOSFET
23 Amps, 25 Volts
N-Channel D^{2}PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Typical Applications

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	Vdc
Gate-to-Source Voltage - Continuous	V_{GS}	±20	Vdc
Drain Current - Continuous @ T_A = 25°C, Limited by Chip - Continuous @ T_A = 25°C, Limited by Package - Single Pulse (t_p = 10 μs)	 I_D I_D I_{DM}	 23 6.0 60	A
Total Power Dissipation @ T_A = 25°C	P_D	TBD	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	TBD	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

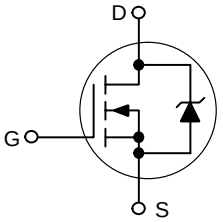
1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).

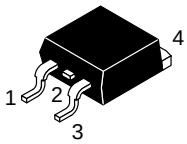
ON Semiconductor®

http://onsemi.com

23 AMPERES, 25 VOLTS
$R_{DS(on)}$ = 32 mΩ (Typ)

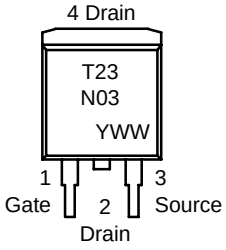
N-CHANNEL





D^{2}PAK
CASE 418B
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



T23N03 = Specific Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTB23N03R	D^{2}PAK	50 Units/Rail
NTB23N03RT4	D^{2}PAK	800/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V(br)_{DSS}$	 25 -	 28 -	 - -	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 - -	 - -	 1.0 10	μAdc
Gate-Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 -	 1.8 -	 2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V_{GS} = 4.5 Vdc, I_D = 6 Adc) (V_{GS} = 10 Vdc, I_D = 6 Adc)		$R_{DS(on)}$	 - -	 50.3 32.3	 60 45	mΩ
Forward Transconductance (Note 3) (V_{DS} = 10 Vdc, I_D = 6 Adc)		g_{FS}	 -	 14	 -	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	-	225	-	pF
Output Capacitance		C_{oss}	-	108	-	
Transfer Capacitance		C_{rss}	-	48	-	
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	(V_{GS} = 10 Vdc, V_{DD} = 10 Vdc, I_D = 6 Adc, R_G = 3 Ω)	$t_{d(on)}$	-	2.0	-	ns
Rise Time		t_r	-	14.9	-	
Turn-Off Delay Time		$t_{d(off)}$	-	9.9	-	
Fall Time		t_f	-	2.0	-	
Gate Charge	(V_{GS} = 4.5 Vdc, I_D = 6 Adc, V_{DS} = 10 Vdc) (Note 3)	Q_T	-	3.76	-	nC
		Q_1	-	1.7	-	
		Q_2	-	1.6	-	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I_S = 6 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 6 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 - -	 0.87 0.74	 1.2 -	Vdc
Reverse Recovery Time	(I_S = 6 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	-	8.7	-	ns
		t_a	-	5.2	-	
		t_b	-	3.5	-	
Reverse Recovery Stored Charge		Q_{RR}	-	0.003	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

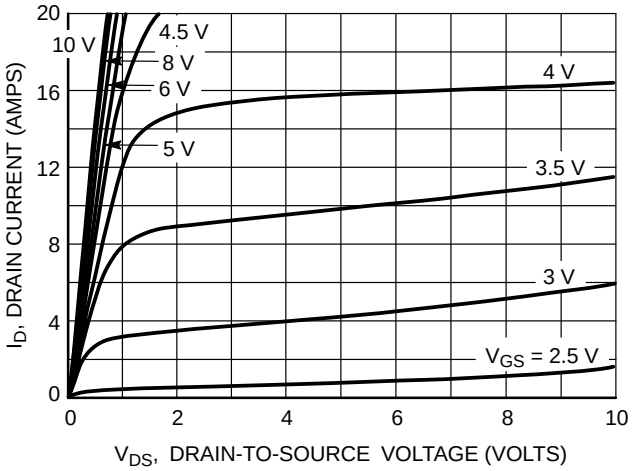


Figure 1. On-Region Characteristics

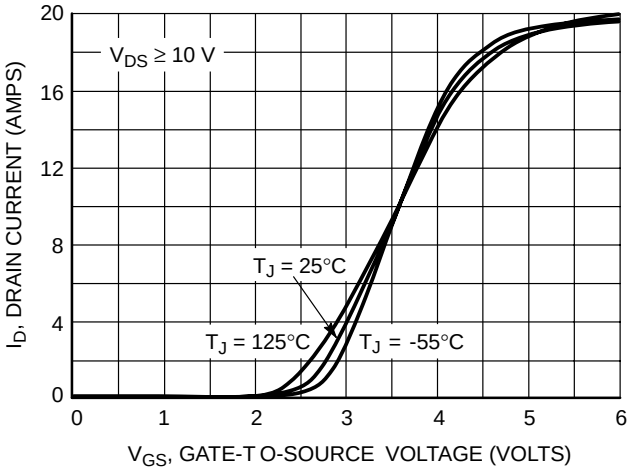


Figure 2. Transfer Characteristics

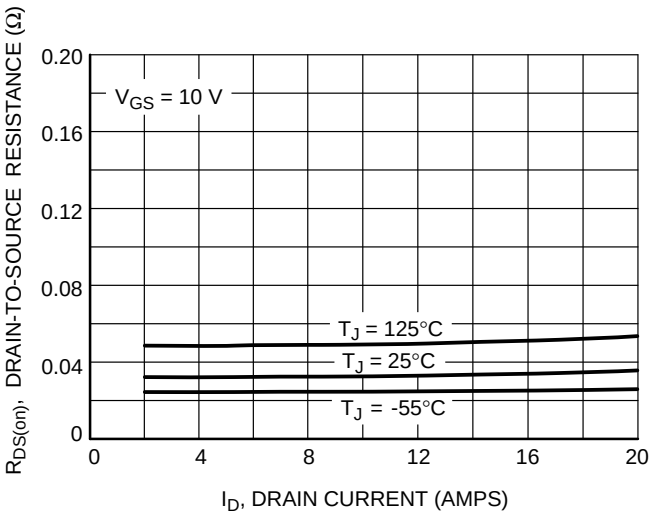


Figure 3. On-Resistance versus Drain Current and Temperature

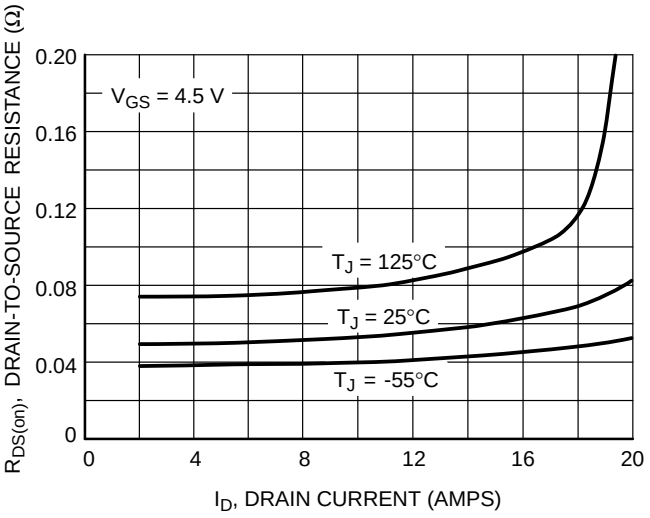


Figure 4. On-Resistance versus Drain Current and Temperature

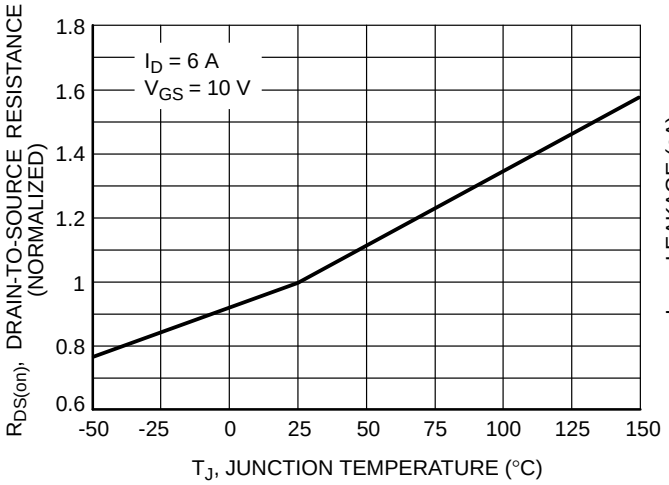


Figure 5. On-Resistance Variation with Temperature

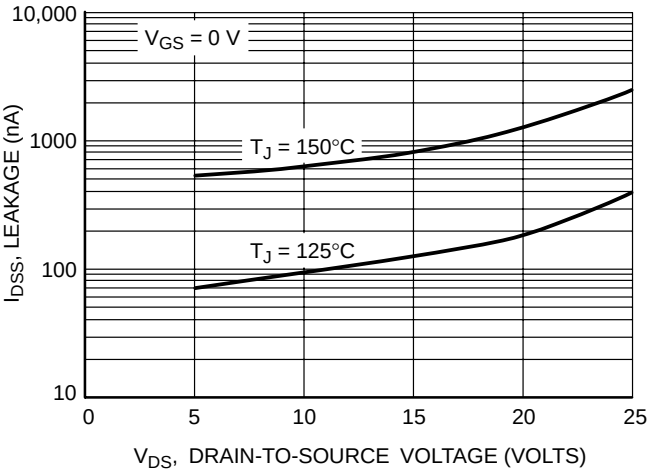


Figure 6. Drain-to-Source Leakage Current versus Voltage

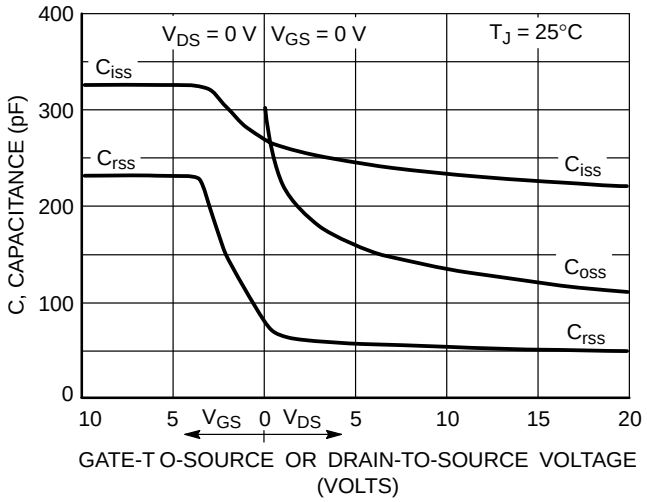


Figure 7. Capacitance Variation

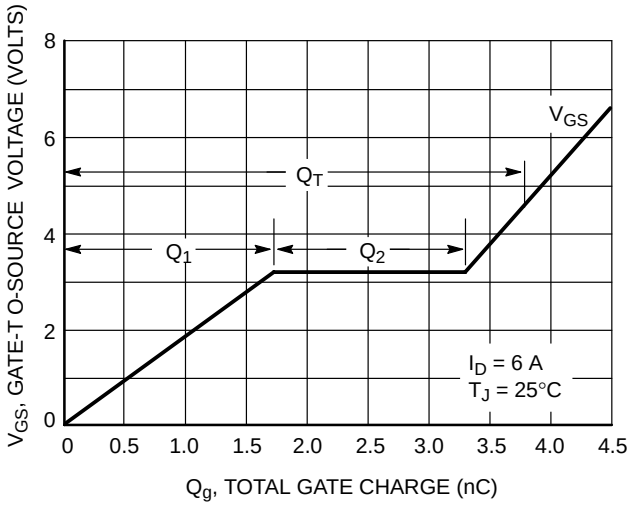


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

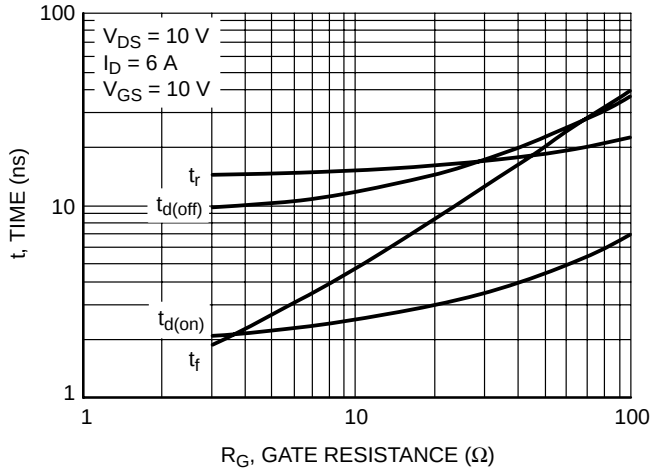


Figure 9. Resistive Switching Time Variation versus Gate Resistance

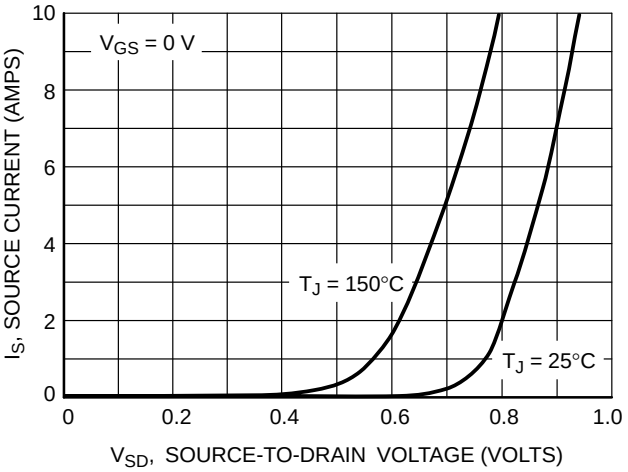
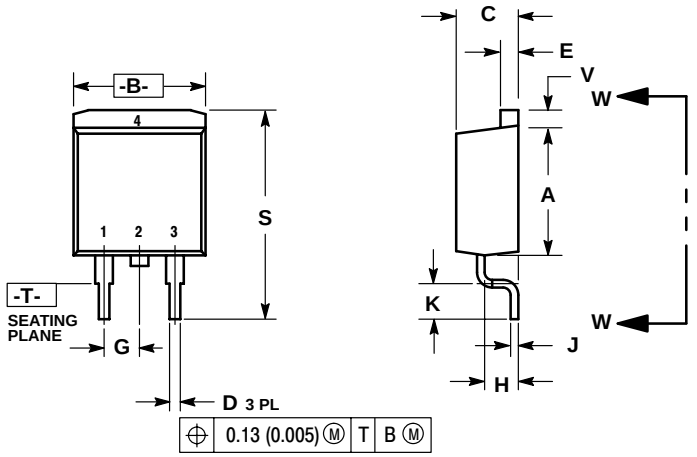


Figure 10. Diode Forward Voltage versus Current

PACKAGE DIMENSIONS

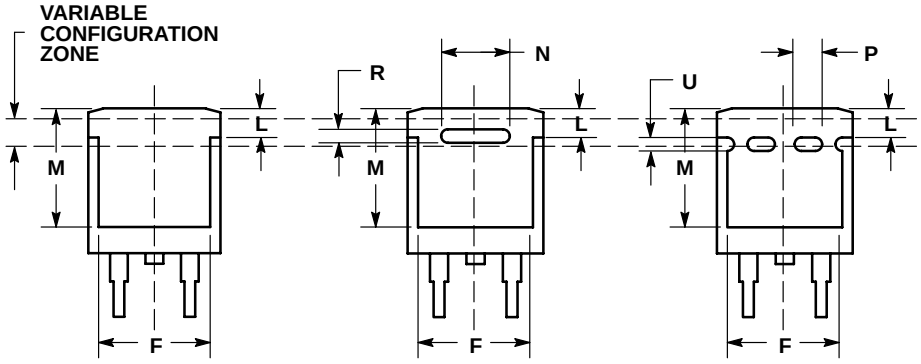
D²PAK
CASE 418B-04
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

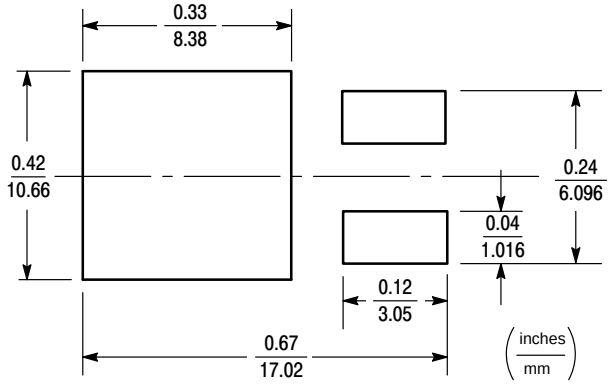
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



VIEW W-W 1 | VIEW W-W 2 | VIEW W-W 3

RECOMMENDED FOOTPRINT



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