nPower BBT2400
Quad 2.5G Transceiver

Infiniband™ Low Power CMOS 4 Channel 2.50Gbps Transceiver

Features

- Up to 10.0 Gbps Duplex Raw Data Rate
- Up to 2.50 Gbps per channel
- Compliant with 10-Gigabit Ethernet (IEEE 802.3ae) D.3.1
  - Superior to proposed jitter requirements
- User-Controlled Dual-Speed functionality
  - 2.5 Gbps
  - 1.25 Gbps
- Ultra low-power operation
  - 200mW typical per channel
  - 1.8V or 2.5V I/O: 3.3V tolerant
- 8B/10B Encoder/Decoder Ch. (optional)
- XGMII
  - SSTL2 or HSTL 1.8V
  - 8-bit or 10-bit Parallel Input/Output Data
- Comma detection (Both disparities) Byte alignment
  - Programmable "K" character
- Channel-to-Channel Alignment
- Single-ended or differential input Reference clock
- Flexible Tx and Rx Clock Schemes
- Receive Cable Equalization
- Per Channel Signal detect indicator
- Double Data-Rate (DDR) Mode
- 802.3 compliant MDC/MDIO serial interface
- Clock compensation via IDLE insertion, deletion

Applications

The nPower BBT2400 is a quad 8-bit/10-bit parallel-to-serial and serial-to-parallel transceiver device ideal for high bandwidth interconnection between line cards, serial back-planes, or optical modules. In addition to high-bandwidth links, the transceivers can be configured as a single 10 **G**igabit e**X**tended **A**ttachment **U**nit Interface (XAUI), providing up to 10.0 Gbps of duplex bandwidth. See Figure 1.

Benefits

- Industry-leading power performance
- Receiver Equalization eliminates needs to over-drive at transmitter
  - Reduced EMI, cross-talk
- Link distances of up to 40" FR-4 traces and two connectors
- Proven Interoperability with various back-planes, optical modules and semiconductors
- Complete applications collateral
  - Evaluation Board
  - Applications Note
  - Verilog Model, SPICE Model
  - High-Speed System Engineering technical support

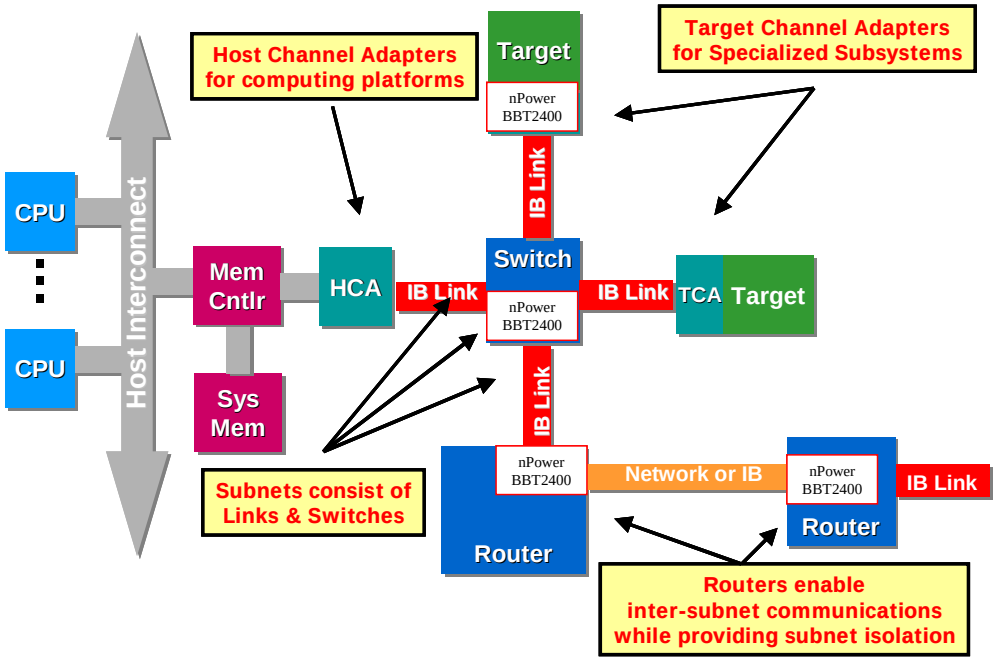

Figure 1 Channel Adapters & Router Applications

Data Flow

The BBT2400 Transmitters normally accept data from the parallel XGMII data bus, clocked by the appropriate Transmit Byte Clock for the channel, and resynchronize it into the Transmit FIFO using local reference clock. The data is then optionally encoded using the standard IEEE802.3-2000 8B/10B encoder, serialized, and sent out on the differential CML, XAUI-compatible Tx pins. The BBT2400 Receivers accept serial data from the CML pins, perform clock and data recovery on the bit stream, optionally scan the data for the "comma" patterns and Byte-Align the data on either 'disparity' comma pattern, and de-serialize the data. The data is then optionally 10B/8B decoded into the 8bit or 10 bit data link stream, and fed into the receiver FIFO, where clock compensation, optional channel alignment, and resynchronization to any one of the individual recovered clocks, one channel clock, or the local reference clock are performed.

In addition, several other facilities are provided to ease system testing. Loopback at either the serial or parallel ports is available under external pin or MII control. Suitable control and status registers are available through the IEEE standard MDIO/MDC system. The XGMII interface may be configured in source-centered or source synchronous timing formats for ASIC-friendly timing.

If the Built-in-Self-Test function (BIST) is in use, the serial Tx data instead is derived from a PRBS 2^23 -1 pattern generator. In this BIST mode, the received serial data is checked against the PRBS pattern transmitted and, if an error is found, a flag signal is provided.

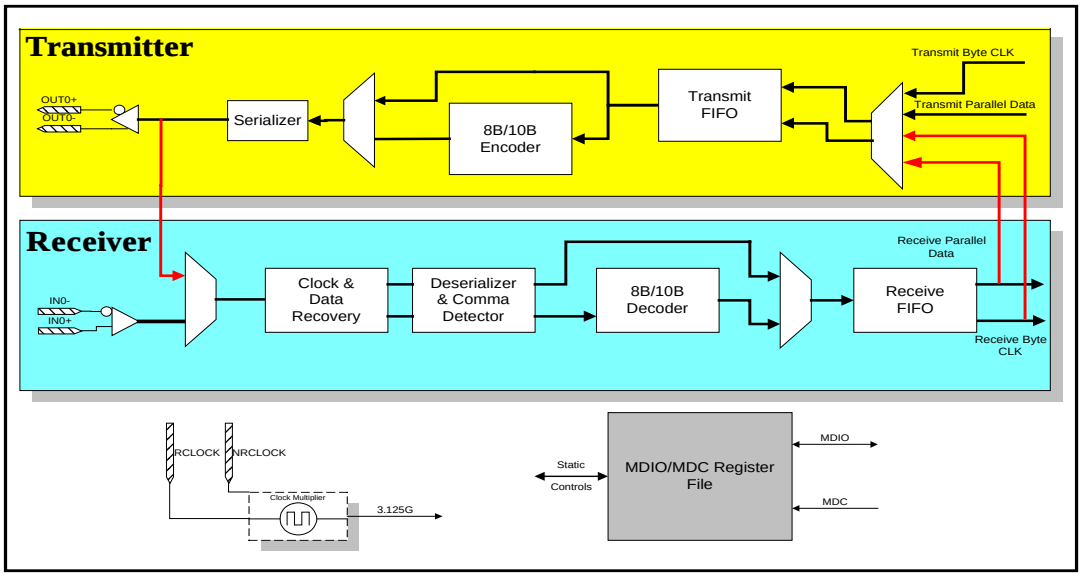

Figure 2 BBT2400 Functional Block Diagram

Part Ordering Information:
nPower BBT2400 – 289-pin BGA

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