NEC

MOS FIELD EFFECT TRANSISTOR
NP34N06HLD,NP34N06ILD

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel Temperature 175 Degree Rated
- Super Low On-state Resistance
  $R_{DS(on)1}$ = 20 mΩ (MAX.) (V_{GS} = 10 V, I_D = 17 A)
  $R_{DS(on)2}$ = 35 mΩ (MAX.) (V_{GS} = 5 V, I_D = 17 A)
- Low C_{iss} : C_{iss} = 2100 pF (TYP.)
- Built-in Gate Protection Diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP34N06HLD	TO-251
NP34N06ILD	TO-252

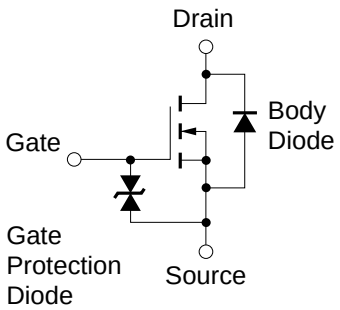
★ ABSOLUTE MAXIMAM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±34	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±108	A
Total Power Dissipation (T_A = 25 °C)	P_T	1.2	W
Total Power Dissipation (T_{ch} = 25 °C)	P_T	50	W
Single Avalanche Current	I_{AS}	T.B.D.	A
Single Avalanche Energy Note2	E_{AS}	T.B.D.	mJ
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to + 175	°C

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

EQUIVALENT CIRCUIT



THERMAL RESISTANCE

Channel to Case	Rth(ch-c)	3.0	°C/W
Channel to Ambient	Rth(ch-a)	125	°C/W

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

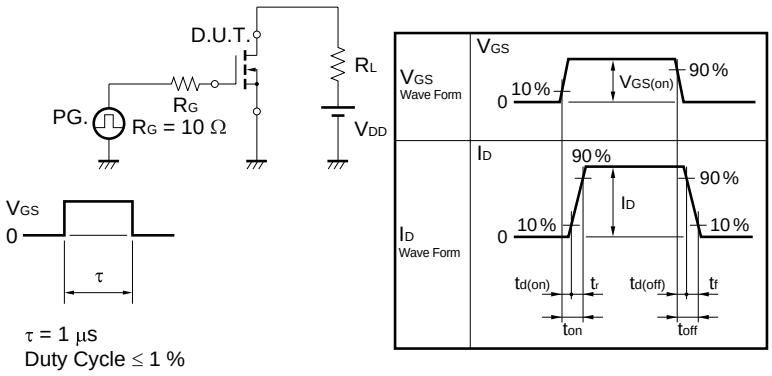
Document No. D13932EJ2V0PM00 (2nd edition)
Date Published January 1999 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

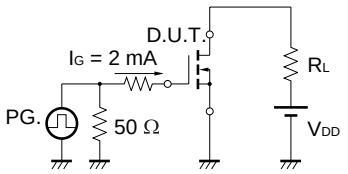
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 17 A		15	20	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 17 A		19	35	mΩ
	$R_{DS(on)3}$	V_{GS} = 4 V, I_D = 17 A		21	40	mΩ
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 17 A	8	16		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		2100	3150	pF
Output Capacitance	C_{oss}			550	830	pF
Reverse Transfer Capacitance	C_{rss}			210	380	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 17 A, $V_{GS(on)}$ = 10 V, V_{DD} = 30 V, R_G = 10 Ω		30	70	ns
Rise Time	t_r			250	630	ns
Turn-off Delay Time	$t_{d(off)}$			13	30	ns
Fall Time	t_f			15	38	ns
Total Gate Charge	Q_G	I_D = 34 A, V_{DD} = 48 V, V_{GS} = 10 V		45	68	nC
Gate to Source Charge	Q_{GS}			7.0		nC
Gate to Drain Charge	Q_{GD}			13		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 34 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 34 A, V_{GS} = 0 V, di/dt = 100 A/μs		60		ns
Reverse Recovery Charge	Q_{rr}			100		nC

TEST CIRCUIT 1 SWITCHING TIME



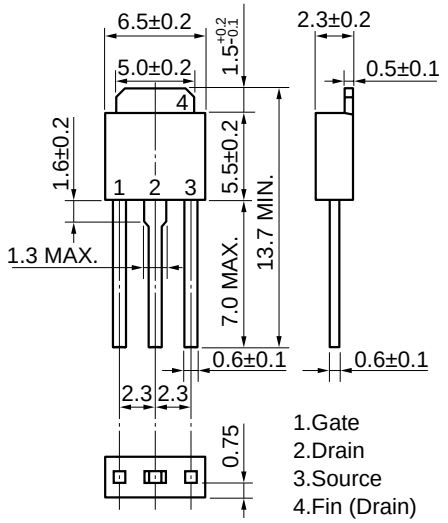
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

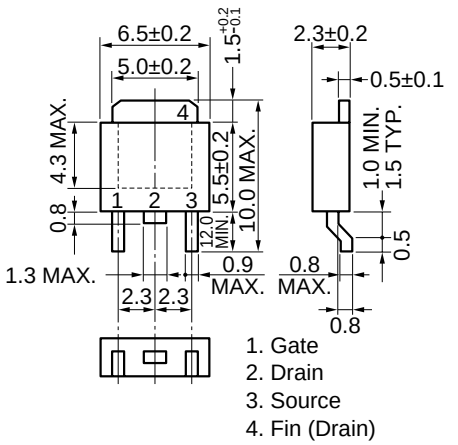


PACKAGE DRAWINGS (Unit : mm)

TO-251 (MP-3)



TO-252 (MP-3Z)



M4 96.5