

MOS FIELD EFFECT TRANSISTOR NP34N06HLD, NP34N06ILD

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel Temperature 175 Degree Rated
- Super Low On-state Resistance
 $R_{DS(on)1} = 20 \text{ m}\Omega$ (MAX.) ($V_{GS} = 10 \text{ V}$, $I_D = 17 \text{ A}$)
 $R_{DS(on)2} = 35 \text{ m}\Omega$ (MAX.) ($V_{GS} = 5 \text{ V}$, $I_D = 17 \text{ A}$)
- Low C_{iss} : $C_{iss} = 2100 \text{ pF}$ (TYP.)
- Built-in Gate Protection Diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP34N06HLD	TO-251
NP34N06ILD	TO-252

★ ABSOLUTE MAXIMAM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 34	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 108	A
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_T	1.2	W
Total Power Dissipation ($T_{ch} = 25 \text{ }^\circ\text{C}$)	P_T	50	W
Single Avalanche Current	I_{AS}	T.B.D.	A
Single Avalanche Energy ^{Note2}	E_{AS}	T.B.D.	mJ
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 175	$^\circ\text{C}$

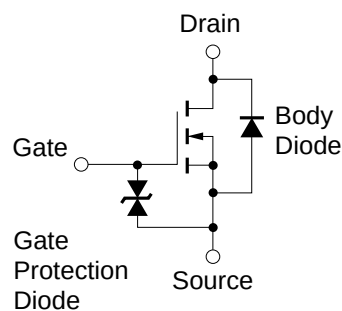
Notes 1. $PW \leq 10 \text{ } \mu\text{s}$, Duty cycle $\leq 1 \%$

2. Starting $T_{ch} = 25 \text{ }^\circ\text{C}$, $R_G = 25 \text{ } \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-c)}$	3.0	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-a)}$	125	$^\circ\text{C/W}$

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

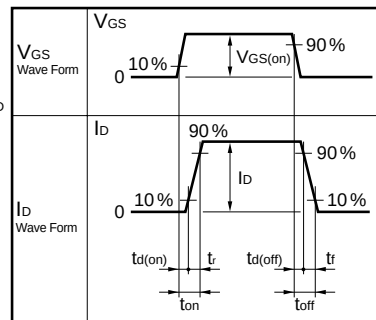
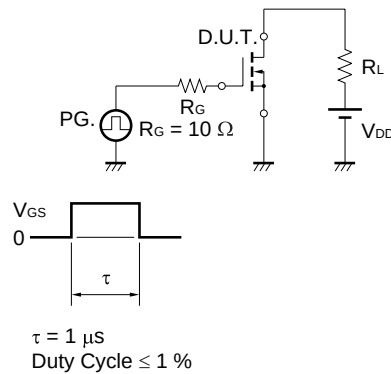
When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

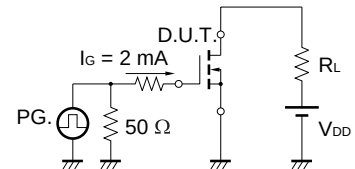
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 17 A		15	20	mΩ
	R _{DS(on)2}	V _{GS} = 5 V, I _D = 17 A		19	35	mΩ
	R _{DS(on)3}	V _{GS} = 4 V, I _D = 17 A		21	40	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 17 A	8	16		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		2100	3150	pF
Output Capacitance	C _{oss}			550	830	pF
Reverse Transfer Capacitance	C _{rss}			210	380	pF
Turn-on Delay Time	t _{d(on)}	I _D = 17 A, V _{GS(on)} = 10 V, V _{DD} = 30 V, R _G = 10 Ω		30	70	ns
Rise Time	t _r			250	630	ns
Turn-off Delay Time	t _{d(off)}			13	30	ns
Fall Time	t _f			15	38	ns
Total Gate Charge	Q _G	I _D = 34 A, V _{DD} = 48 V, V _{GS} = 10 V		45	68	nC
Gate to Source Charge	Q _{GS}			7.0		nC
Gate to Drain Charge	Q _{GD}			13		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 34 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 34 A, V _{GS} = 0 V, di/dt = 100 A/μs		60		ns
Reverse Recovery Charge	Q _{rr}			100		nC

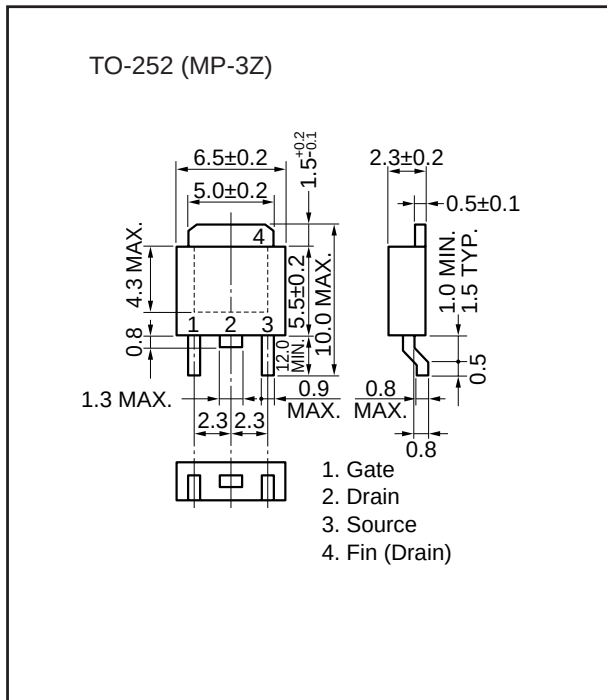
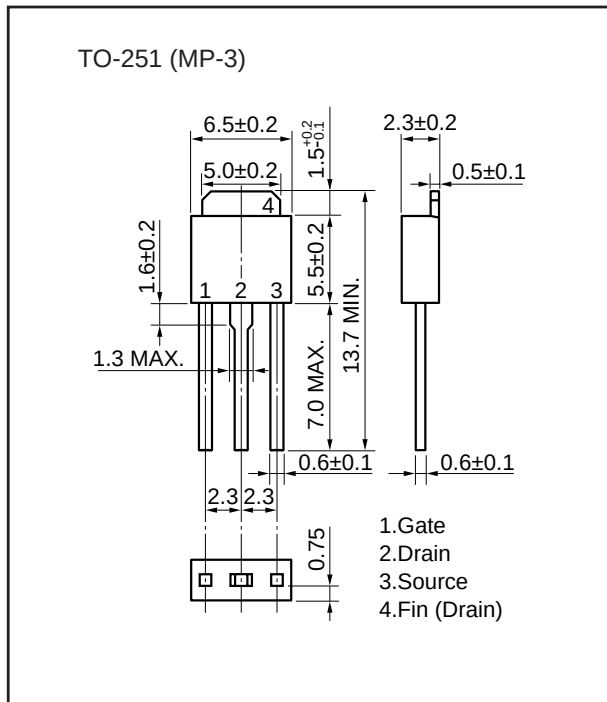
TEST CIRCUIT 1 SWITCHING TIME



TEST CIRCUIT 2 GATE CHARGE



PACKAGE DRAWINGS (Unit : mm)



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Anti-radioactive design is not implemented in this product.