NLAS1053

2:1 Mux/Demux Analog Switches

The NLAS1053 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. The device consists of a single 2:1 Mux/Demux (SPDT), similar to ON Semiconductor's NLAS4053 analog and digital voltages that may vary across the full power supply range (from V_{CC} to GND).

The inhibit and select input pins have over voltage protection that allows voltages above V_{CC} up to 7.0 V to be present without damage or disruption of operation of the part, regardless of the operating voltage.

- High Speed: t_{PD} = 1 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High Bandwidth, Improved Linearity, and Low RDS_{ON}
- INH Pin Allows a Both Channels 'OFF' Condition (With a High)
- $RDS_{ON} \cong 25\ \Omega$, Performance Very Similar to the NLAS4053
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Useful For Switching Video Frequencies Beyond 50 MHz
- Latch–Up Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V
- Tiny US8 Package, Only 2.1 X 3.0 mm

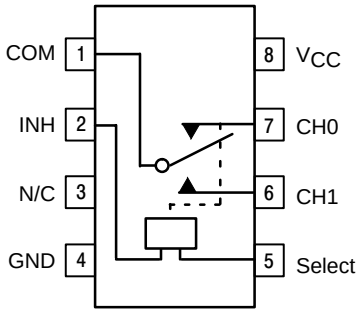
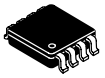


Figure 1. Pin Assignment

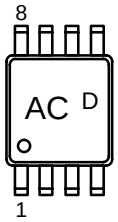
ON Semiconductor™

http://onsemi.com

MARKING DIAGRAMS



US8
US SUFFIX
CASE 493–01



AC = Device Code
D = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

FUNCTION TABLE

INH	Select	Ch 0	Ch 1
H	X	OFF	OFF
L	L	ON	OFF
L	H	OFF	ON

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		–0.5 to +7.0	V
V_{IN}	Digital Input Voltage (Select and Inhibit)		–0.5 ≤ V is ≤ +7.0	V
V_{IS}	Analog Output Voltage (V_{CH} or V_{COM})		–0.5 ≤ V is ≤ V_{CC} +0.5	V
I_{IK}	DC Current, Into or Out of Any Pin		50	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance		250	°C/W
P_D	Power Dissipation in Still Air at 85°C		250	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL–94–VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 200 N/A	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 5)	±300	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		2.0	5.5	V
V_{IN}	Digital Input Voltage (Select and Inhibit)		GND	5.5	V
V_{IO}	Static or Dynamic Voltage Across an Off Switch		GND	V_{CC}	V
V_{IS}	Analog Input Voltage (CH, COM)		GND	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		–55	+125	°C
t_r, t_f	Input Rise or Fall Time, (Enable Input)	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

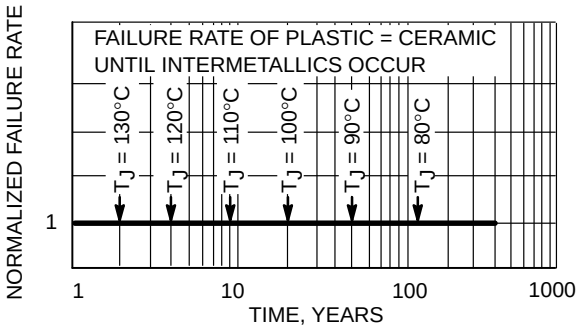


Figure 2. Failure Rate versus Time Junction Temperature

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				−55°C to 25°C	<85°C	<125°C	
V_{IH}	Minimum High–Level Input Voltage, Select and Inhibit Inputs		2.0 2.5 3.0 4.5 5.5	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	V
V_{IL}	Maximum Low–Level Input Voltage, Select and Inhibit Inputs		2.0 2.5 3.0 4.5 5.5	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current, Select and Inhibit Inputs	V_{IN} = 5.5 V or GND	0 V to 5.5 V	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	Select and Inhibit = V_{CC} or GND	5.5	1.0	1.0	2.0	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	< 85°C	< 125°C	
R_{ON}	Maximum “ON” Resistance (Figures 17 – 23)	$V_{IN} = V_{IL}$ or V_{IH} V_{IS} = GND to V_{CC} $\|I_{IN}\| \le$ 10.0 mA	2.5 3.0 4.5 5.5	70 40 20 16	85 46 28 22	105 52 34 28	Ω
R_{FLAT} (ON)	ON Resistance Flatness (Figures 17 – 23)	$V_{IN} = V_{IL}$ or V_{IH} $\|I_{IN}\| \le$ 10.0 mA V_{IS} = 1V, 2V, 3.5V	4.5	4	4	5	Ω
ΔR_{ON} (ON)	ON Resistance Match Between Channels	$V_{IN} = V_{IL}$ or V_{IH} $\|I_{IN}\| \le$ 10.0 mA V_{CH1} or V_{CH0} = 3.5 V	4.5	2	2	3	Ω
I_{CH0} I_{CH1}	CH1 or CH0 Off Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} V_{CH1} or V_{CH0} = 1.0 V_{COM} 4.5 V	5.5	1	10	100	nA
$I_{COM(ON)}$	COM ON Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} V_{CH1} 1.0 V or 4.5 V with V_{CH0} floating or V_{CH1} 1.0 V or 4.5 V with V_{CH1} floating V_{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Max Limit							Unit
				–55 to 25°C			< 85°C		< 125°C		
				Min	Typ*	Max	Min	Max	Min	Max	
t_{ON}	Turn–On Time (Figures 12 and 13) INH to Output	R_L = 300 Ω, C_L = 35 pF (Figures 4 and 5)	2.5 3.0 4.5 5.5	2 2 1 1	7 5 4 3	12 10 9 8	2 2 1 1	15 15 12 12	2 2 1 1	15 15 12 12	ns
t_{OFF}	Turn–Off Time (Figures 12 and 13) INH to Output	R_L = 300 Ω, C_L = 35 pF (Figures 4 and 5)	2.5 3.0 4.5 5.5	2 2 1 1	7 5 4 3	12 10 9 8	2 2 1 1	15 15 12 12	2 2 1 1	15 15 12 12	ns
t_{trans}	Transition Time (Channel Selection Time) (Figure) Select to Output	R_L = 300 Ω, C_L = 35 pF (Figures and)	2.5 3.0 4.5 5.5	5 5 2 2	18 13 12 9	28 21 16 14	5 5 2 2	30 25 20 20	5 5 2 2	30 25 20 20	ns
t_{BBM}	Minimum Break–Before–Make Time	V_{IS} = 3.0 V (Figure 3) R_L = 300 Ω, C_L = 35 pF	2.5 3.0 4.5 5.5	1 1 1 1	12 11 6 5		1 1 1 1		1 1 1 1		ns

*Typical Characteristics are at 25°C.

		Typical @ 25, VCC = 5.0 V	
C_{IN}	Maximum Input Capacitance, Select/INH Input	8	pF
C_{NO} or C_{NC}	Analog I/O (switch off)	10	
C_{COM}	Common I/O (switch off)	10	
$C_{(ON)}$	Feedthrough (switch on)	20	

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V_{CC} V	Typical 25°C	Unit
BW	Maximum On–Channel –3dB Bandwidth or Minimum Frequency Response (Figure 10)	V_{IN} = 0 dBm V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	170 200 200	MHz
V_{ONL}	Maximum Feedthrough On Loss	V_{IN} = 0 dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	–3 –3 –3	dB
V_{ISO}	Off–Channel Isolation (Figure 10)	f = 100 kHz; V_{IS} = 1 V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	–93 –93 –93	dB
Q	Charge Injection Select Input to Common I/O (Figure 15)	V_{IN} = V_{CC} to GND, F_{IS} = 20 kHz $t_r = t_f$ = 3 ns R_{IS} = 0 Ω, C_L = 1000 pF $Q = C_L * \Delta V_{OUT}$ (Figure 8)	3.0 5.5	1.5 3.0	pC
THD	Total Harmonic Distortion THD + Noise (Figure 14)	F_{IS} = 20 Hz to 100 kHz, R_L = Rgen = 600 Ω, C_L = 50 pF V_{IS} = 5.0 V_{PP} sine wave	5.5	0.1	%

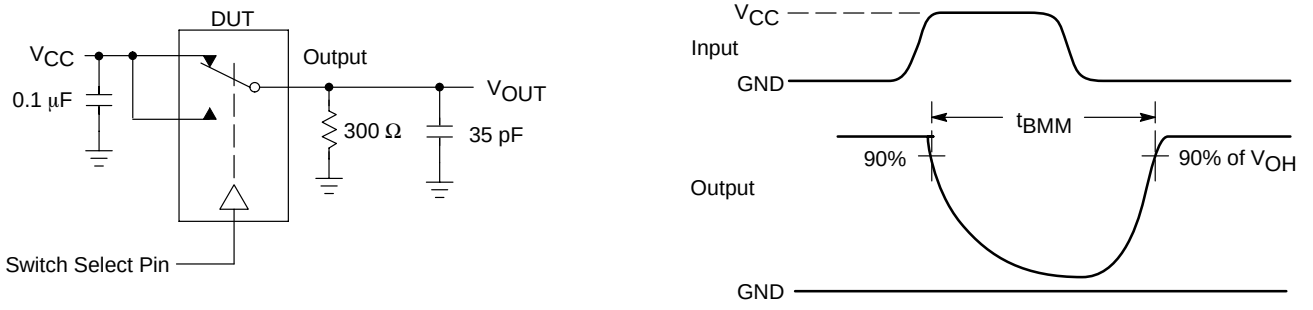


Figure 3. t_{BBM} (Time Break–Before–Make)

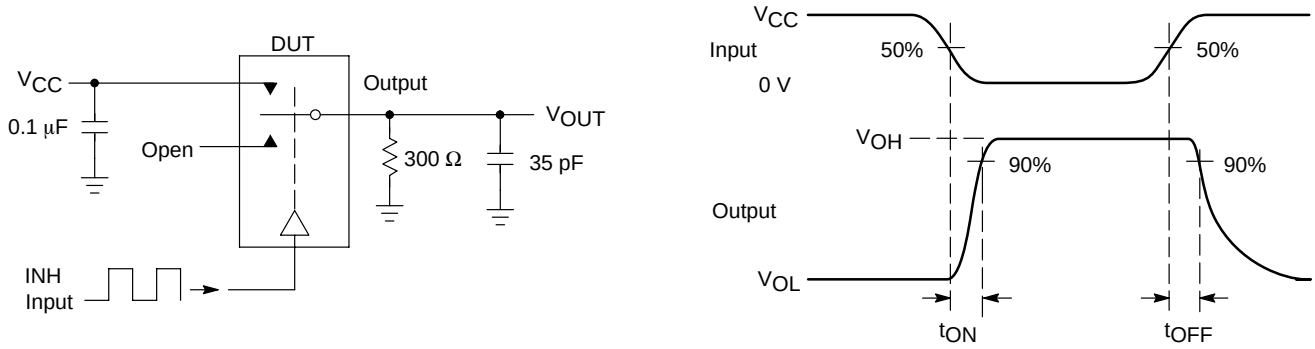


Figure 4. t_{ON}/t_{OFF}

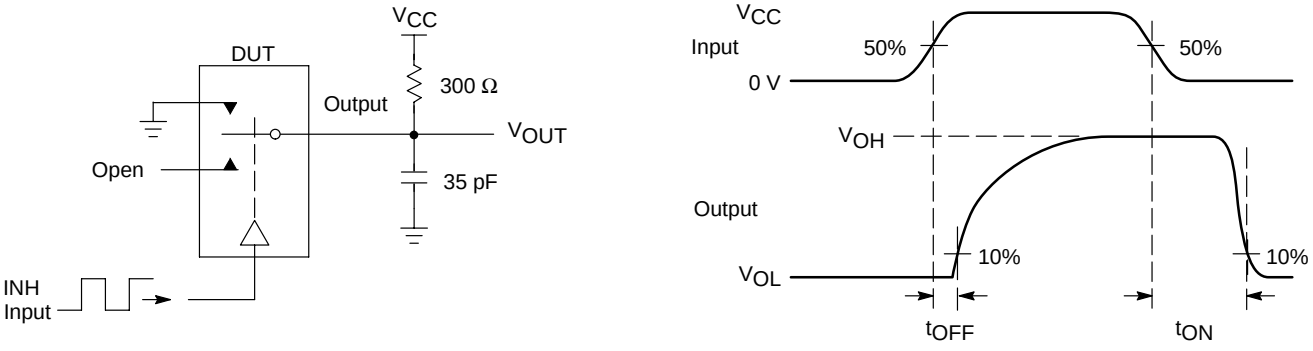


Figure 5. t_{ON}/t_{OFF}

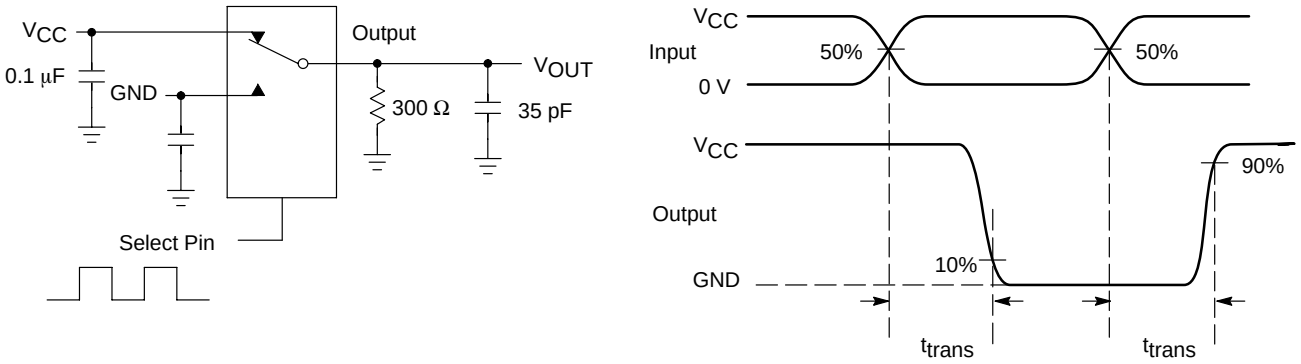
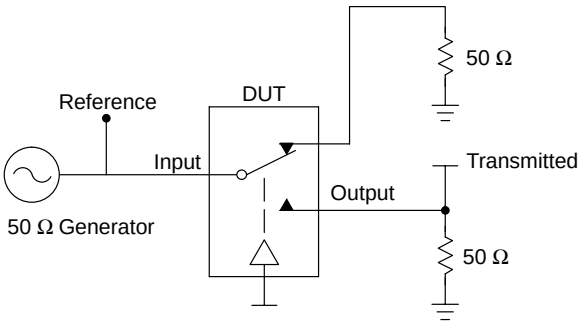


Figure 6. t_{trans} (Channel Selection Time)



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = $20 \text{ Log}\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = $20 \text{ Log}\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

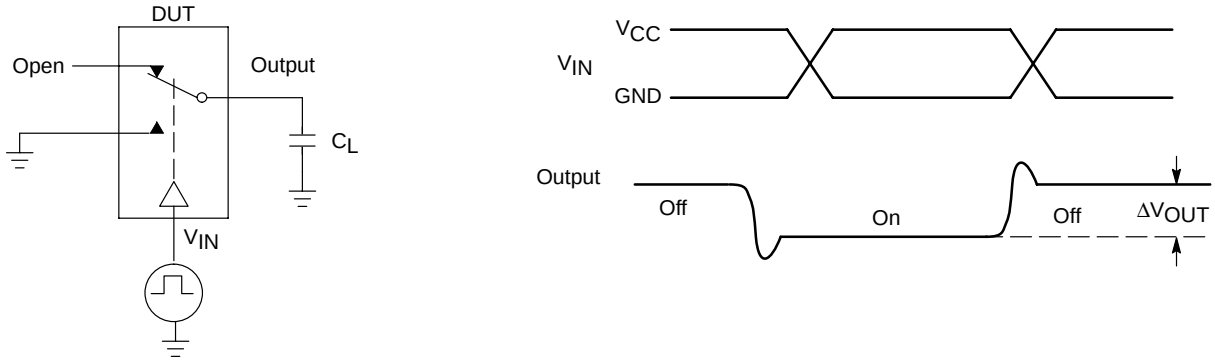


Figure 8. Charge Injection: (Q)

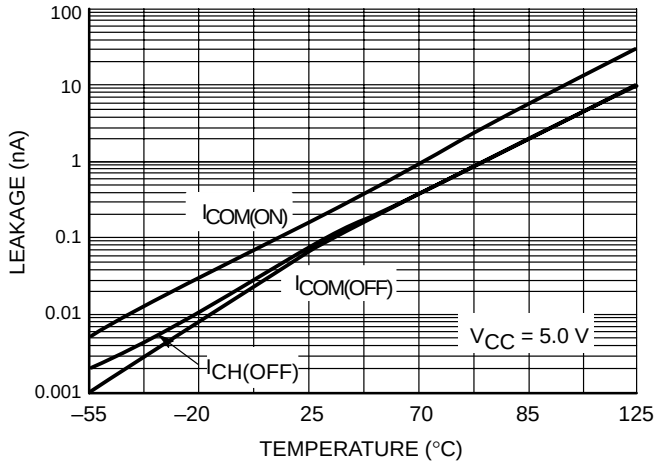


Figure 9. Switch Leakage versus Temperature

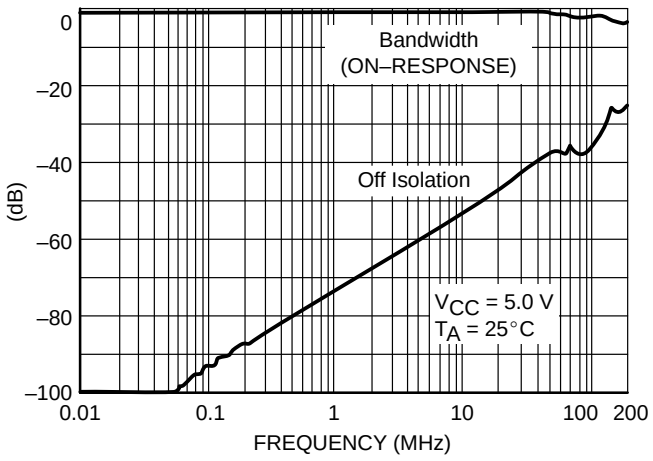


Figure 10. Bandwidth and Off–Channel Isolation

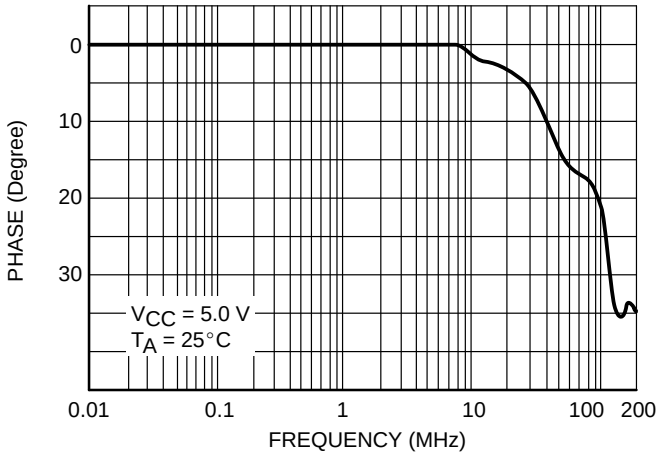


Figure 11. Phase versus Frequency

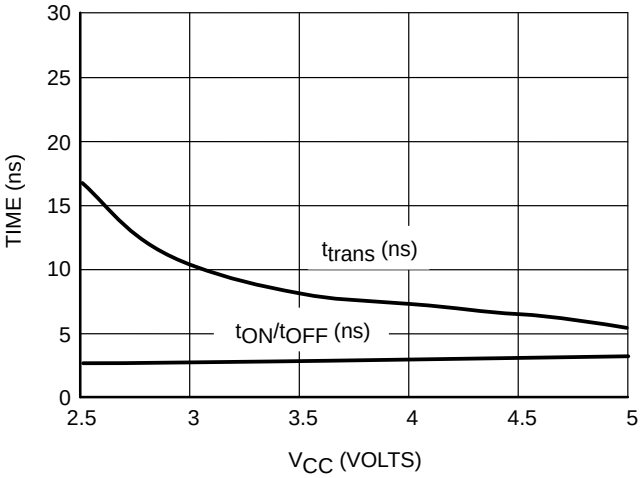


Figure 12. t_{ON} and t_{OFF} versus V_{CC} at 25°C

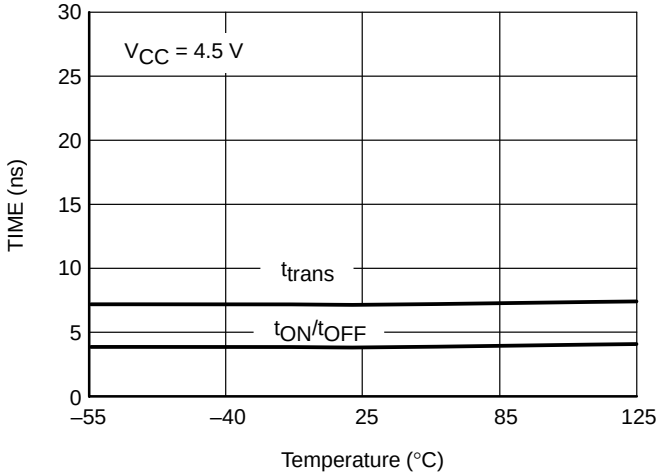


Figure 13. t_{ON} and t_{OFF} versus Temp

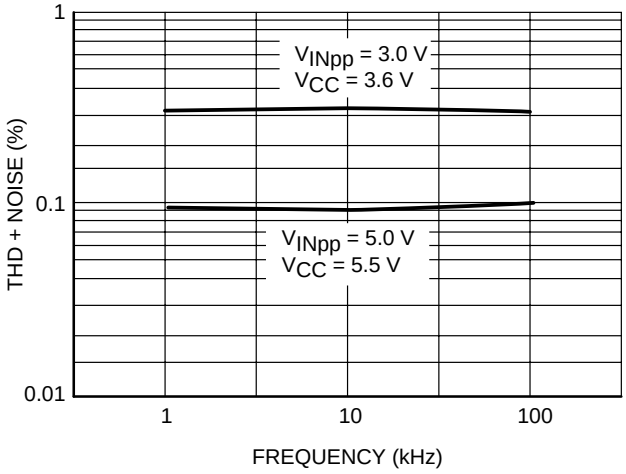


Figure 14. Total Harmonic Distortion Plus Noise versus Frequency

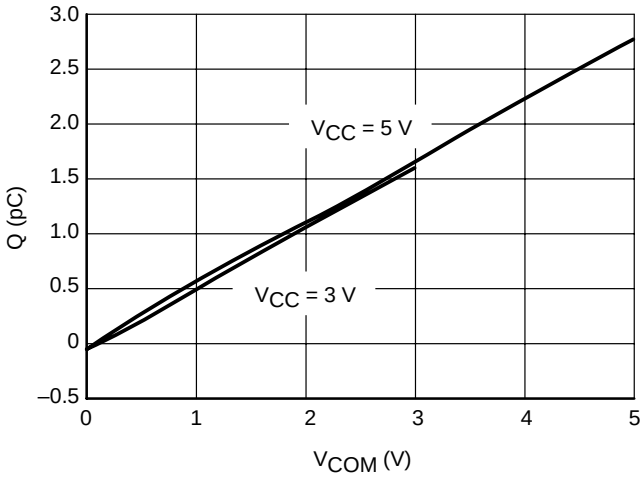


Figure 15. Charge Injection versus COM Voltage

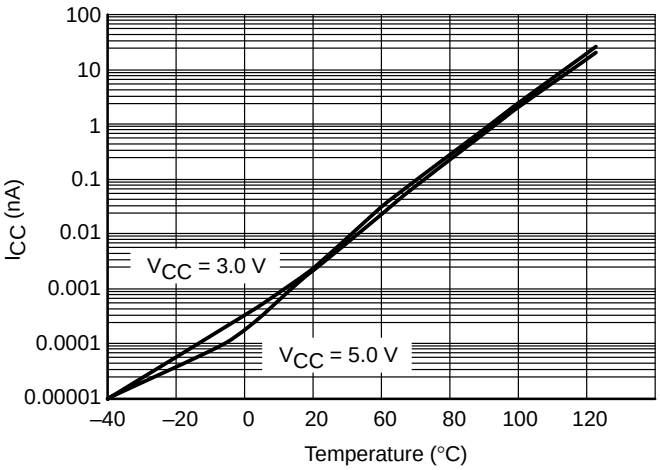


Figure 16. I_{CC} versus Temp, V_{CC} = 3 V & 5 V

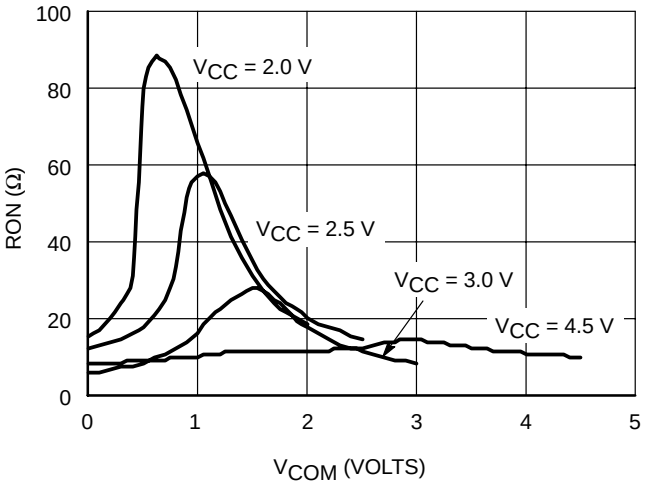


Figure 17. R_{ON} versus V_{COM} and V_{CC} (@ 25°C

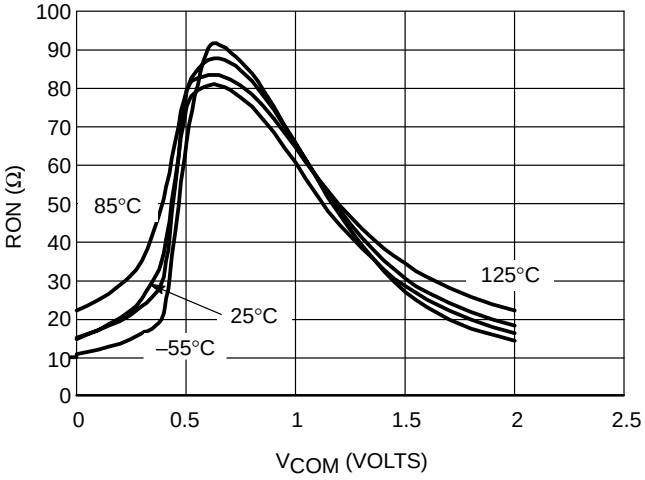


Figure 18. R_{ON} versus V_{COM} and Temperature, V_{CC} 2.0 V

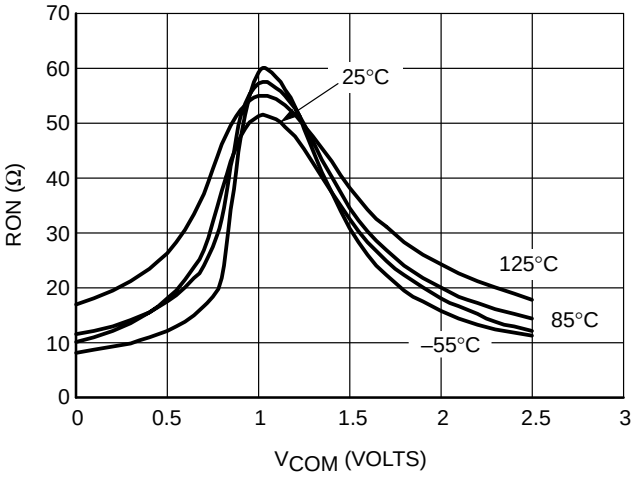


Figure 19. R_{ON} versus V_{COM} and Temperature, V_{CC} = 2.5 V

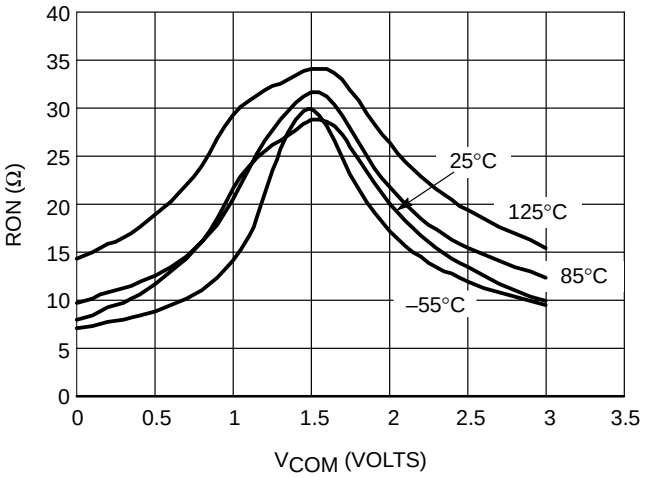


Figure 20. R_{ON} versus V_{COM} and Temperature, V_{CC} = 3.0 V

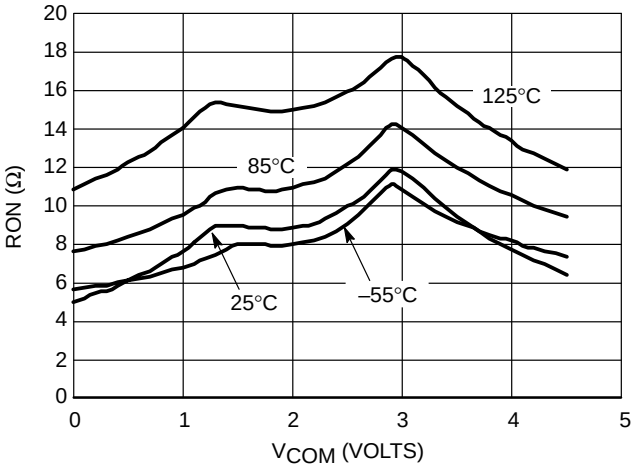


Figure 21. R_{ON} versus V_{COM} and Temperature, V_{CC} = 4.5 V

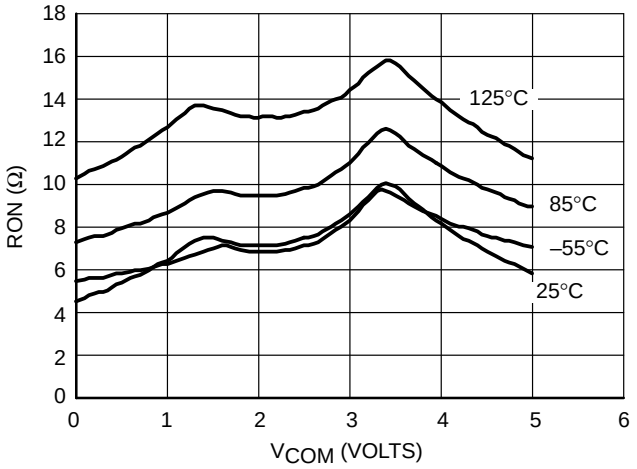


Figure 22. R_{ON} versus V_{COM} and Temperature, V_{CC} = 5.0 V

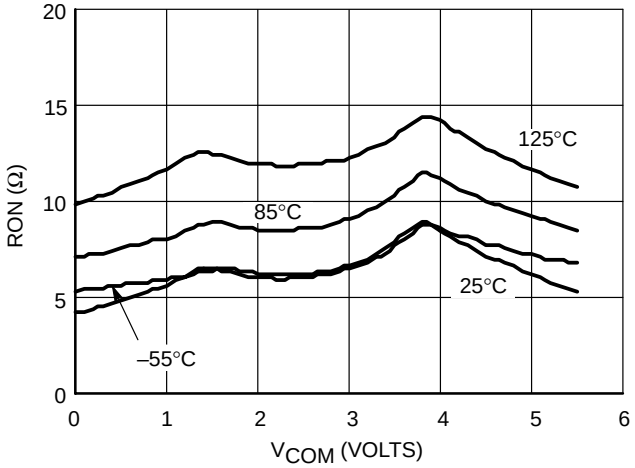


Figure 23. R_{ON} versus V_{COM} and Temperature, V_{CC} = 5.5 V

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature				Package Type	Tape and Reel Size
	Circuit Indicator	Technology	Device Function	Package Suffix		
NLAS1053US	NL	AS	1053	US	US8	178 mm (7″) 3000 Unit

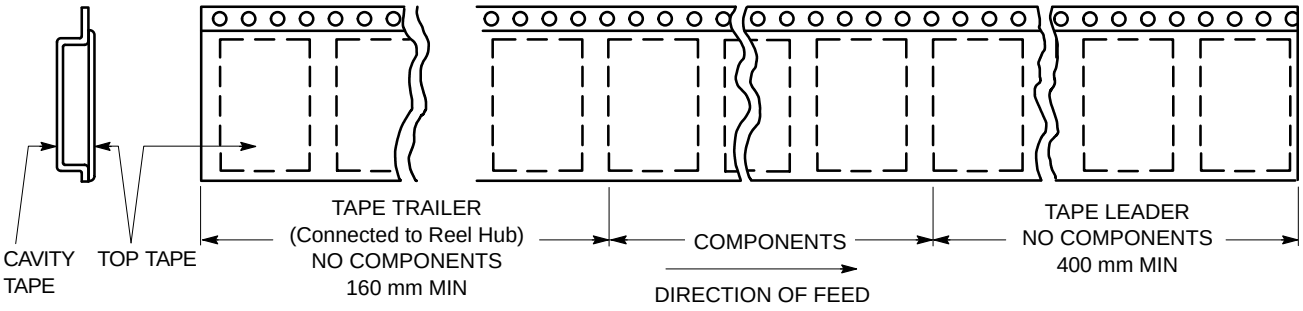


Figure 24. Tape Ends for Finished Goods

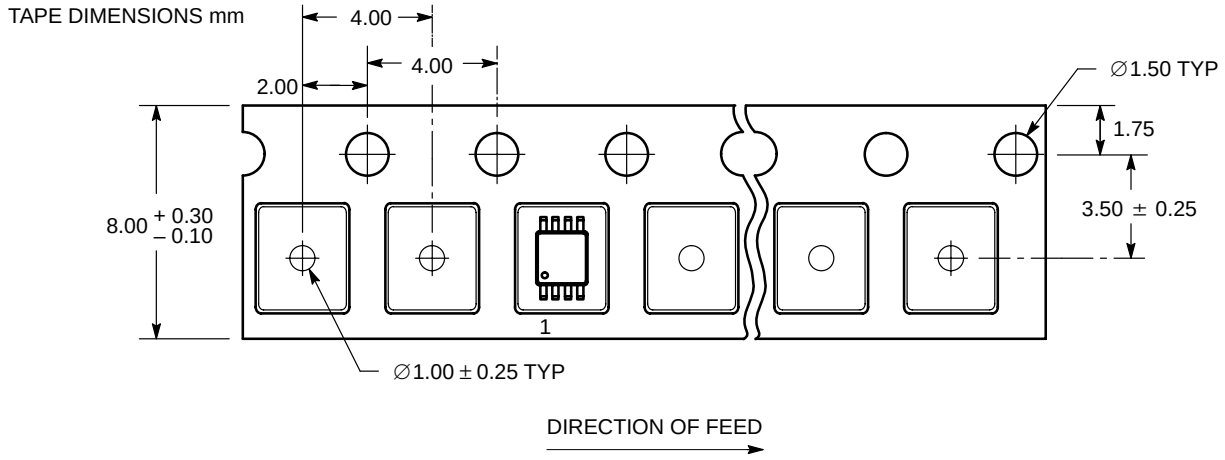


Figure 25. US8 Reel Configuration/Orientation

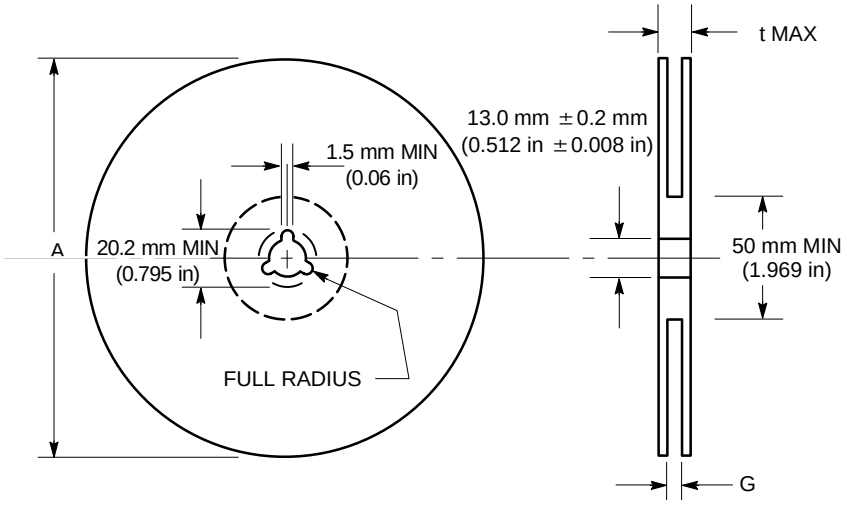


Figure 26. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, –0.0 (0.33 in + 0.059 in, –0.00)	14.4 mm (0.56 in)

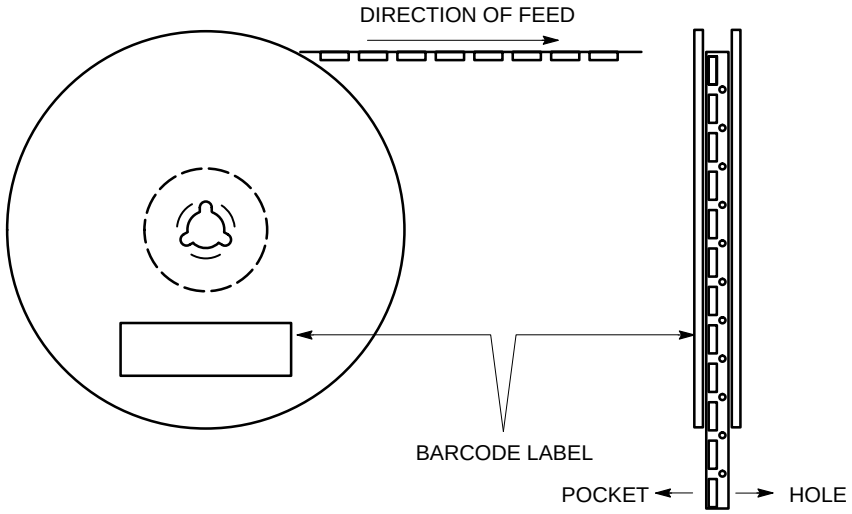
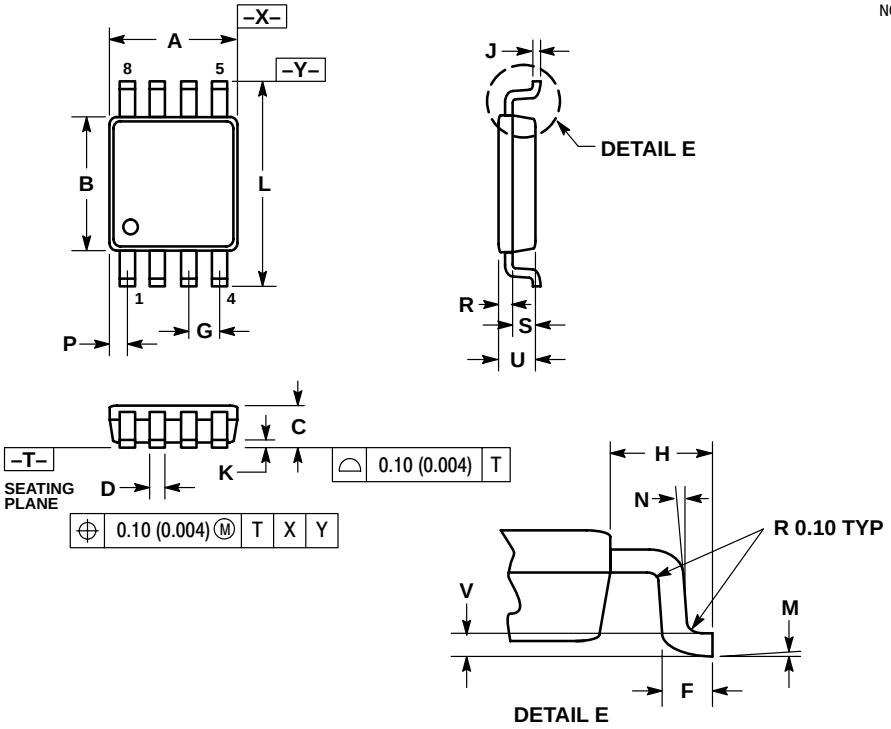


Figure 27. Reel Winding Direction

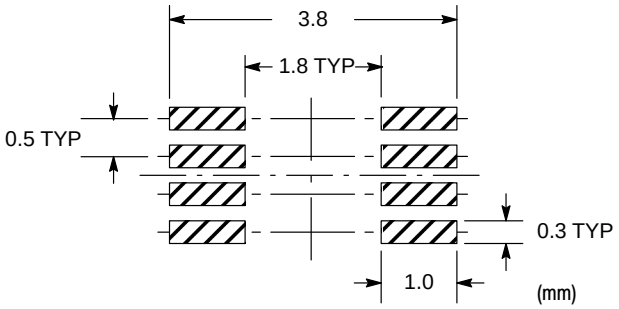
PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSION. INTER–LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0. 0203 MM. (300–800 INCH).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002").

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.28	0.44	0.011	0.017
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	



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