MiMagic™ NMS7041 System-on-Chip
For 3D Handheld Internet Appliances

PRODUCT BRIEF

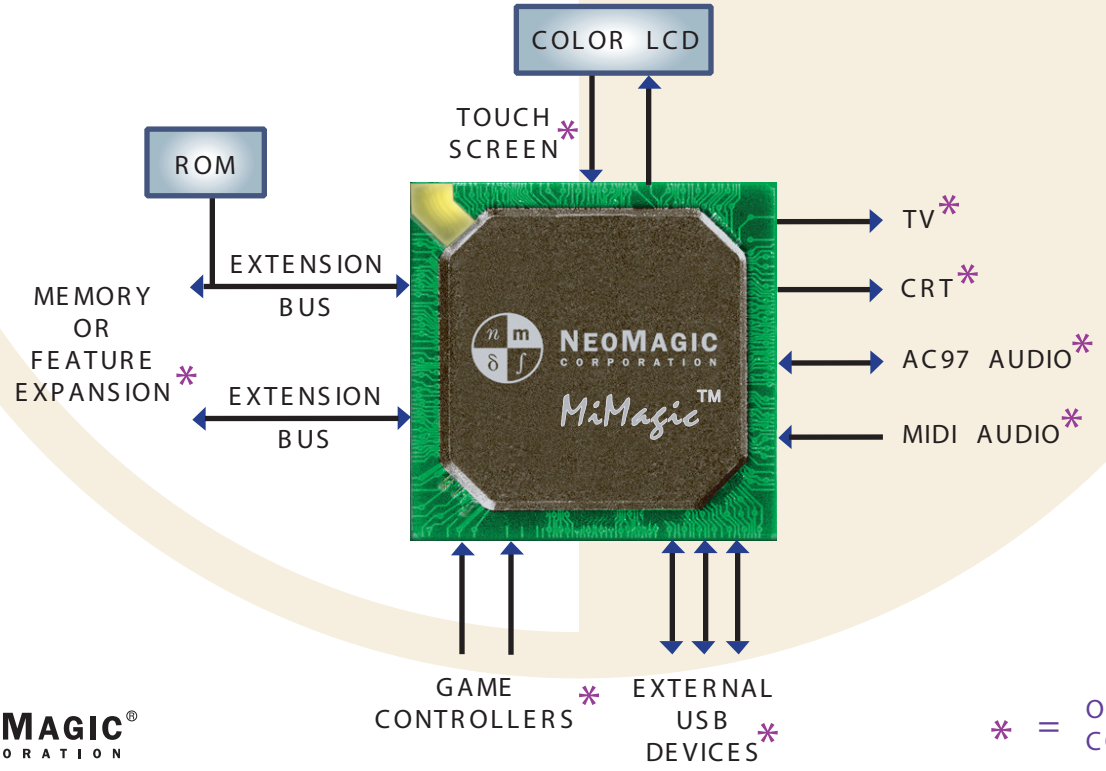
DESCRIPTION

MiMagic™ is NeoMagic's family of highly integrated System-on-Chip solutions, enabling a new generation of handheld Internet appliances with the lowest power, smallest form-factor, and best multimedia features. The heart of the MiMagic™ NMS7041 SOC incorporates a 32-Bit MIPS 4Kc RISC CPU core, a powerful 3D graphics engine that includes both triangle set-up and rendering pipelines, high performance 128-bit hardware BitBLT engine for speedy processing and display of 2D graphics, and 4MBytes of 256-bit wide embedded synchronous DRAM. The SOC also integrates DMA, memory, interrupt, and touch screen controllers, LCD and TV-output (requires an external TV encoder), multi-channel audio controller, three-port USB host core with integrated transceivers, and a variety of timers and peripherals. The SOC system solution can be expanded with external SFLASH, SMROM, and SDRAM memory up to a total of 512MBytes in any combination of up to nine separate devices. The primary user interface is through touch screen input and two game controller inputs with integrated ADCs. This MiMagic™ SOC is an ideal candidate for smart handheld devices such as handheld gaming and media playback entertainment systems, PDAs and WebPads with gaming capability, and a wide variety of mobile systems requiring efficient 3D multimedia processing.

SYSTEM-LEVEL SPECIFICATION

- Memory-mapped architecture
- 32-Bit RISC CPU
- 3D graphics accelerator
- 4MB of embedded DRAM
- 2.5V ± 5% core voltage
- 3.3V ± 5% I/O voltage
- First samples in 329-pin PBGA package

FIGURE 1: SYSTEM DIAGRAM



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SYSTEM-ON-CHIP FEATURES

MIPS32 4Kc CPU
- MMU/TLB
- 16KB 4-way set-associative I-cache
- 16KB 4-way set-associative D-cache
- 32 x 16 Multiply & Divide Unit

3D graphics engine
- Triangle set-up engine
- 3D Rendering pipeline
- Double buffering to prevent image tearing
- 16-Bit Z buffer for depth processing
- Bilinear filtering
- Trilinear filtering
- Flat and Gouraud shading
- Perspective-correct texture mapping
- MIP mapping
- 4/8-Bit Palletized and non-palletized texture
- Streaming texture cache
- Source alpha blending
- Rectangular clipping (both Z and color)
- Vertex fog
- Specular highlight
- Texture blending
- Color dithering

Graphics controller drives LCD/CRT or TV- out (with external TV encoder)
- LCD display resolution from 120 x 160 up to 1024 x 768 x 24 bpp
- RGB 5:6:5 TV output resolution up to 800 x 600 x 16 bpp with horizontal linear interpolation and vertical line doubling for 320 x 240 resolution
- Hardware cursor and hardware icon

Embedded DRAM controller with 4MB of eDRAM
- Peak memory bus bandwidth of 3.2GB/sec. through 256-bit memory bus at 100MHz

Memory controller support for up to 512MB of external memory
- SFLASH devices: 4/8/16/32/64MB
- SMROM devices: 4/8/16/32MB
- SDRAM devices: 1/2/4/8/16/32/64MB
- Burst mode reads
- Control for up to nine external devices

Audio controller
- 8-channel ADPCM decode/playback
- 1-channel record
- Interface to external AC97-CODEC
- MIDI/I2C interface to external wave-table synthesis IC
- Digital volume control
- 8KHz to 48KHz input sample rates

Interrupt controller

DMA controller
- DMA transfer from external memory device to embedded DRAM
- DMA 3D texture transfer from external memory device to 3D texture FIFO
- DMA 3D vertex data from embedded DRAM to 3D vertex FIFO

USB Version 1.1 host controller
- 3 device ports with on-chip USB tranceivers

Analog touch screen controller

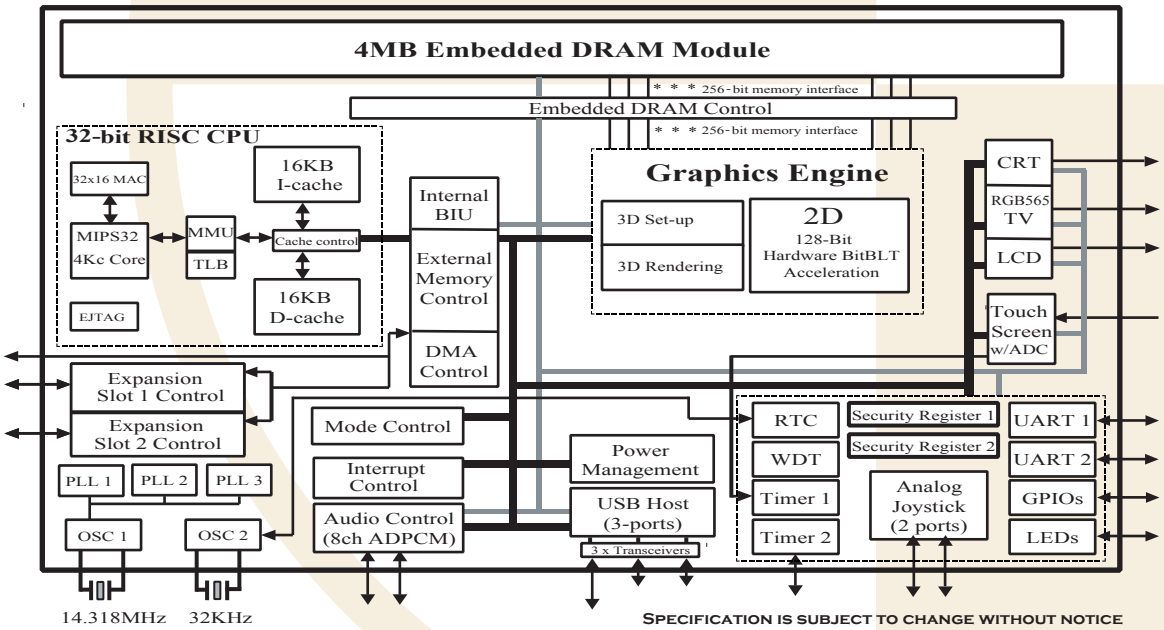
Dual RS-232 compatible UARTs

Dual 32-bit timers, RTC and WDT

Dual analog joysticks & GPIO digital interface

Three modes of power management

FIGURE 2: SYSTEM-ON-CHIP BLOCK DIAGRAM



SPECIFICATION IS SUBJECT TO CHANGE WITHOUT NOTICE

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