MiMagic™ NMS7040 System-on-Chip
For Handheld Internet Appliances

PRODUCT BRIEF

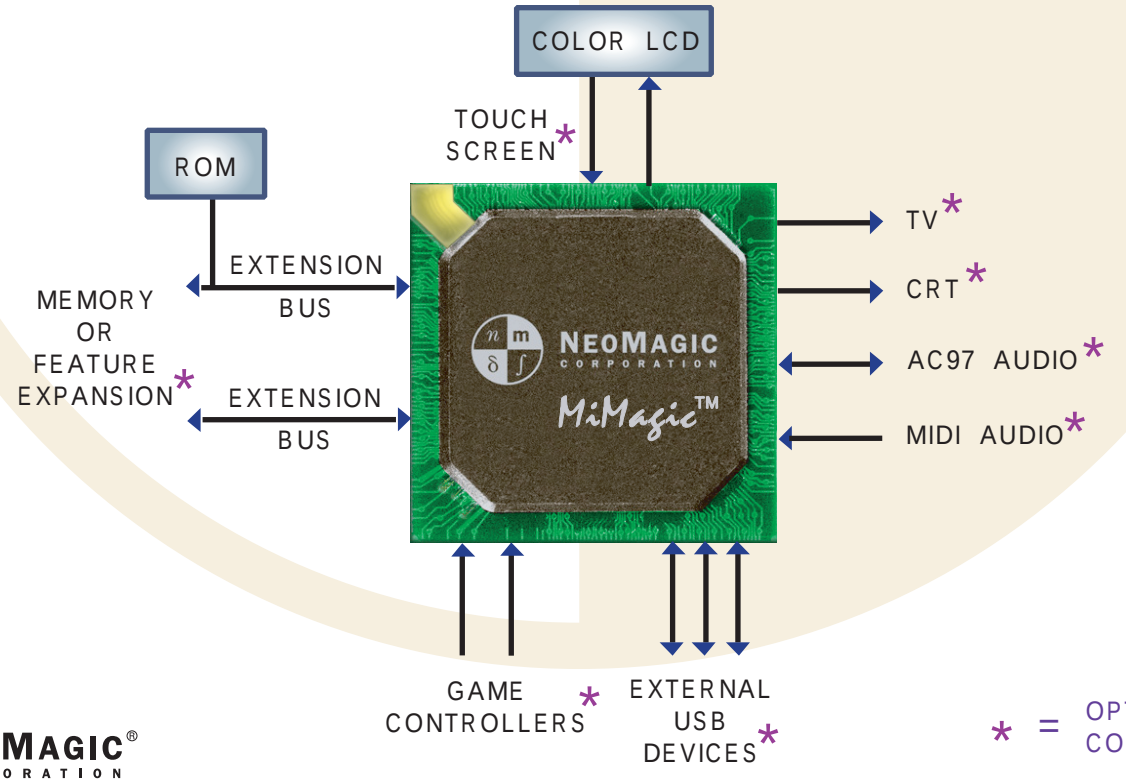
DESCRIPTION

MiMagic™ is NeoMagic's family of highly integrated System-on-Chip solutions, enabling a new generation of handheld Internet appliances with the lowest power, smallest form-factor, and best multimedia features. The heart of the MiMagic™ NMS7040 SOC incorporates a 32-Bit MIPS 4Kc RISC CPU core; a high performance 128-bit hardware BitBLT engine for speedy processing and display of 2D graphics, graphical user interfaces, and images; and 4MBytes of 256-bit wide embedded synchronous DRAM. The SOC also integrates DMA, memory, interrupt, and touch screen controllers, LCD and TV-output (requires an external TV encoder), multi-channel audio controller, three-port USB host core with integrated transceivers, and a variety of timers and peripherals. The SOC system solution can be expanded with external SFLASH, SMROM, and SDRAM memory up to a total of 512MBytes in any combination of up to nine separate devices. The primary user interface is through touch screen input with integrated ADCs. This MiMagic™ SOC is an ideal candidate for smart handheld devices such as PDAs, WebPads, handheld gaming and media playback entertainment systems, and a wide variety of mobile systems requiring efficient multimedia processing.

SYSTEM-LEVEL SPECIFICATION

- Memory-mapped architecture
- 32-Bit RISC CPU
- 2D graphics accelerator
- 4MB of embedded DRAM
- 2.5V ± 5% core voltage
- 3.3V ± 5% I/O voltage
- First samples in 329-pin PBGA package

FIGURE 1: SYSTEM DIAGRAM



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SYSTEM-ON-CHIP FEATURES

MIPS32 4Kc CPU
- MMU/TLB
- 16KB 4-way set-associative I-cache
- 16KB 4-way set-associative D-cache
- 32 x 16 Multiply & Divide Unit

2D graphics acceleration
- 128-Bit hardware BitBLT
- 256-Bit data path to memory
- Color expansion
- XY coordinate addressing
- Rectangle clipping
- Patterning
- Integrated raster operations

Graphics controller drives LCD/CRT or TV- out (with external TV encoder)
- LCD display resolution from 120 x 160 up to 1024 x 768 x 24 bpp
- RGB 5:6:5 TV output resolution up to 800 x 600 x 16 bpp with horizontal linear interpolation and vertical line doubling for 320 x 240 resolution
- Hardware cursor and hardware icon

Embedded DRAM controller with 4MB of eDRAM
- Peak memory bus bandwidth of 3.2GB/sec. through 256-bit memory bus at 100MHz

Interrupt controller

Memory controller support for up to 512MB of external memory
- SFLASH devices: 4/8/16/32/64MB
- SMROM devices: 4/8/16/32MB
- SDRAM devices: 1/2/4/8/16/32/64MB
- Burst mode reads
- Control for up to nine external devices

Audio controller
- 8-channel ADPCM decode/playback
- 1-channel record
- Interface to external AC-97 CODEC
- MIDI/I2C interface to external wave-table synthesis IC
- Digital volume control
- 8KHz to 48KHz input sample rates

USB Version 1.1 host controller
- 3 device ports
- On-chip USB transceivers

Analog touch screen controller

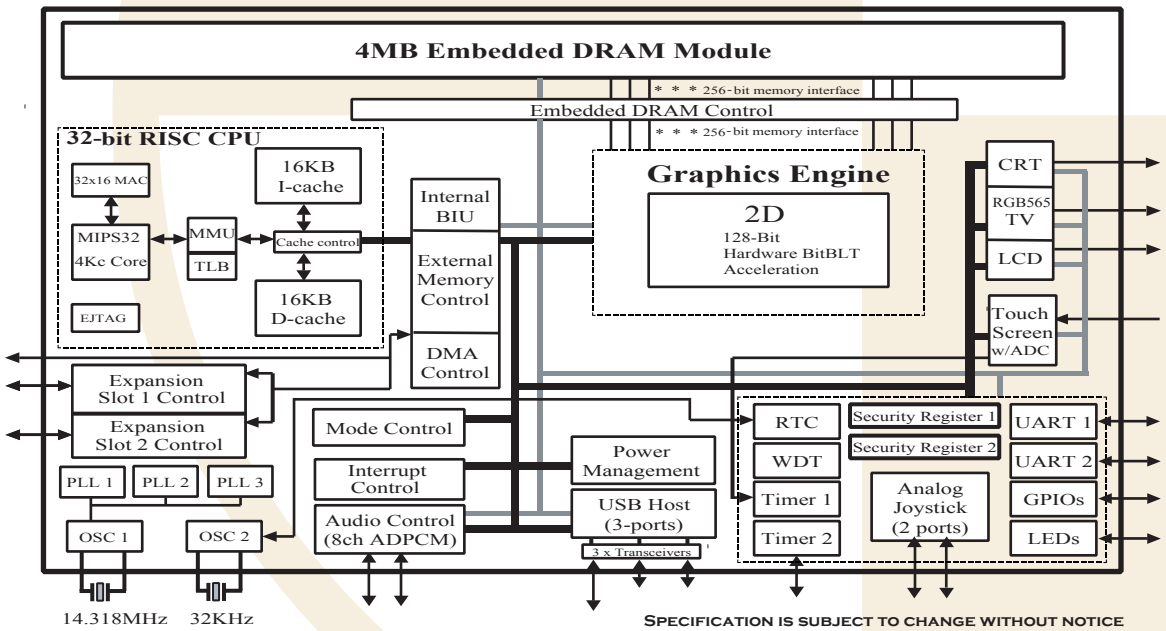
Dual RS-232 compatible UARTs

Dual 32-bit timers, RTC and WDT

Dual analog joysticks & GPIO digital interface

Three modes of power management
- Normal operation with inactive modules
- Standby (also disables LCD display)
- Suspend (only 32KHz oscillator running)

FIGURE 2: SYSTEM-ON-CHIP BLOCK DIAGRAM



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