GaInP/GaAs HBT MMIC Distributed Amplifier
DC-15 GHz

NDA-320-D

6000051 Rev. 1

1

Features

- Reliable Low-Cost HBT Design
- 9 dB Gain
- High P1dB
- Distributed amplifier with fixed gain or Automatic Gain Control (AGC) operation
- 50 Ω Input/Output matched for high-frequency utilization
- Incorporation of a secondary ground-via for better thermal management

Description

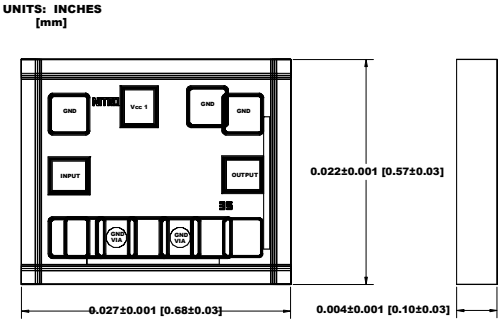
RF Nitro's NDA-320-D Cascadable Broadband GaInP/GaAs MMIC amplifier is a low-cost high-performance solution for your high-frequency RF, Microwave, or Optical amplification needs. This 50-Ohm gain block is based upon a reliable HBT (Heterojunction Bipolar Transistor) proprietary MMIC design, providing unsurpassed performance for small-signal applications.

The NDA-320-D incorporates external dc decoupling capacitors, which limit the low-frequency response. Designed with an external bias resistor, the NDA-310-D provides flexibility and stability to your requirement. In addition, the NDA-320-D chip was designed with an additional grounding-via, providing improved thermal resistance performance. The NDA series of distributed amplifiers also provide design flexibility by incorporating AGC functionality into their designs.

Applications

- Narrow & broadband commercial & military radio designs.
- Linear & Saturated amplifier applications.
- Gain stage or driver amplifiers, providing AGC capability, utilized in microwave radio and optical designs such as PTP, PMP, LMDS, UNII, VSAT, WLAN, cellular, and 10 & 20 Gbps optical modulator systems.

Chip Dimension 0.027" X 0.022" X 0.004"



Electrical Specifications

V_{cc1}= +10V, V_{cc2}= +10V, V_{c1}=+4.75 V, V_{c2}= +2.98V, I_{cc2} = 40 mA, Zo = 50Ω, T_A = +25 °C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Power Gain – S_{21}	f=0.1 to 10.0 GHz f=10.0 to 14.0 GHz f=14.0 to 15.0 GHz	dB dB dB	8.0 6.0	9.0 8.5 (avg.) 7.0	
Gain Flatness - G_F	f=0.1 to 8.0 GHz	dB		±0.6	
Input and Output VSWR	f=0.1 to 12.0 GHz f=12.0 to 15.0 GHz			1.5 1.7	
Bandwidth - BW	BW3 (3dB)	GHz		12.5	
Output Power @ 1-dB Compression	f=2.0 GHz f=6.0 GHz f=14.0 GHz	dBm dBm dBm		TBD	
Noise Figure - NF	f=2.0 GHz	dB		5.5	
3rd Order Intercept – IP3	f=2.0 GHz	dBm		TBD	
Reverse Isolation – S_{12}	f=0.1 to 12.0 GHz	dB		-15	
Device Voltage - Vd		V	3.6	3.9	4.2
Gain Temperature Coefficient $\frac{dG_T}{dT}$		$dB/°C$		-0.0015	

Absolute Maximum Ratings

Exceeding any one or a combination of these limits may cause permanent damage.

Parameter	Absolute Maximum
RF Input Power	+20 dBm
Power Dissipation	300 mW
Device Current, I_{cc1}	42 mA
Device Current, I_{cc2}	48 mA
Junction Temperature, Tj	200° C
Operating Temperature	-45 °C to +85 °C
Storage Temperature	-65 °C to +150 °C

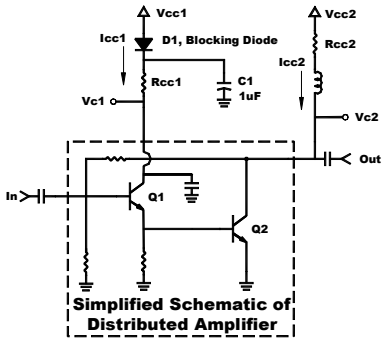
MTTF vs. Junction Temperature

For Tj < 150 °C, MTTF > 1,000,000 hours

Ordering Information

Part Number	Package
NDA-410-D	Chip

Typical Bias Configuration



Suggested Voltage Supply:

$V_{CC1} \geq$ 4.7V

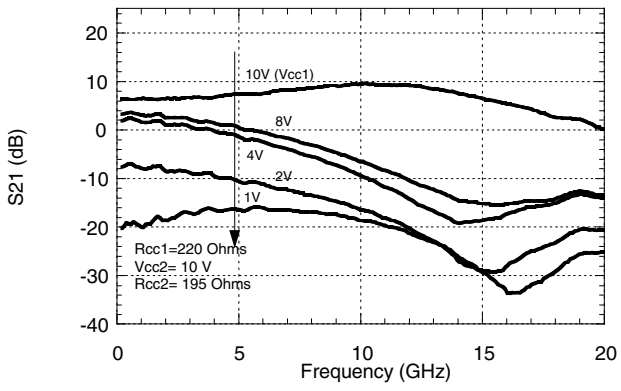
$V_{CC2} \geq$ 5.0V

Bias Resistor Selection
R_{cc1} : For 4.7V<V_{cc1}<5.0V R_{cc1}= 0Ω For 5.0<V_{cc1}<10.0V R_{cc1}= (Vcc1 – 4.7) / 0.024 Ω
R_{cc2} : For 5.0<V_{cc2}<10.0V Ω R_{cc1}= (Vcc2 – 2.98) / 0.040

Typical Bias Parameters for Vcc1=Vcc2=10V:

V_{cc1} (V)	V_{cc2} (V)	I_{cc1} (mA)	V_{c1} (V)	R_{cc1} (Ω)	I_{cc2} (mA)	V_{c2} (V)	R_{cc2} (Ω)
10	10	24	4.75	220	40	3.98	150

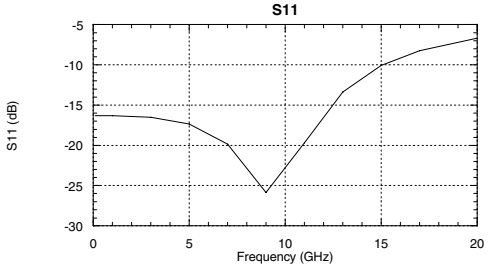
Gain (S21) for AGC mode operation

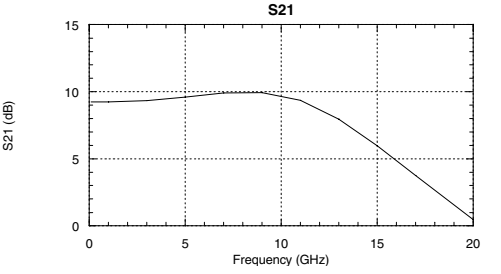


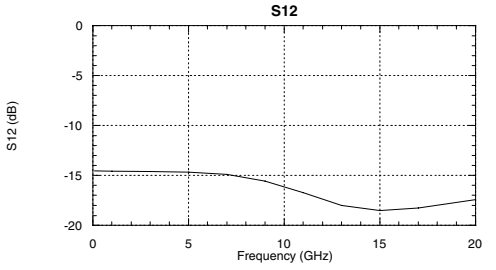
Typical S-Parameter Data V_{cc1}= +10V, V_{cc2}= +10V, V_{c1}=+4.75 V, V_{c2}= +2.98V, I_{cc2} = 40 mA, Zo = 50Ω, T_A = +25 °C

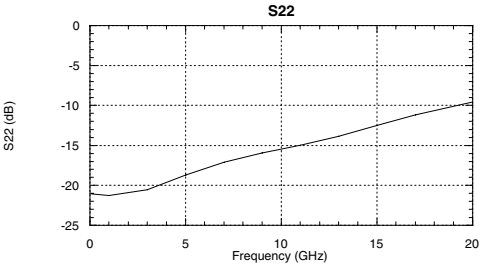
Freq. GHz	S11 (dB)	S11 Mag	S11 Ang	S21 (dB)	S21 Mag	S21 Ang	S12 (dB)	S12 Mag	S12 Ang	S22 (dB)	S22 Mag	S22 Ang
0.1	-16.30	0.15	178.54	9.24	2.90	178.91	-14.52	0.19	-0.29	-21.06	0.09	176.62
1	-16.32	0.15	165.21	9.22	2.89	169.23	-14.55	0.19	-2.77	-21.29	0.09	148.56
3	-16.52	0.15	134.83	9.33	2.93	147.96	-14.60	0.19	-8.01	-20.53	0.09	103.43
5	-17.36	0.14	103.17	9.60	3.02	125.58	-14.66	0.18	-13.92	-18.71	0.12	67.42
7	-19.86	0.10	65.72	9.90	3.12	101.06	-14.91	0.18	-20.80	-17.09	0.14	31.37
9	-25.85	0.05	-8.24	9.94	3.14	73.82	-15.56	0.17	-27.92	-15.92	0.16	-9.70
11	-19.67	0.10	-120.48	9.35	2.93	44.81	-16.74	0.15	-32.50	-14.96	0.18	-56.46
13	-13.35	0.21	-164.28	7.95	2.50	17.02	-18.00	0.13	-31.11	-13.83	0.20	-102.66
15	-10.10	0.31	167.33	5.97	1.99	-6.86	-18.51	0.12	-25.61	-12.49	0.24	-140.72
17	-8.25	0.39	146.35	3.76	1.54	-26.32	-18.24	0.12	-21.28	-11.18	0.28	-169.13
20	-6.64	0.47	123.42	0.45	1.05	-48.85	-17.39	0.13	-19.83	-9.51	0.33	161.34

Typical Performance Measurements V_{cc1}= +10V, V_{cc2}= +10V, V_{c1}=+4.75 V, V_{c2}= +2.98V, I_{cc2} = 40 mA, Zo = 50Ω, T_A = +25 °C





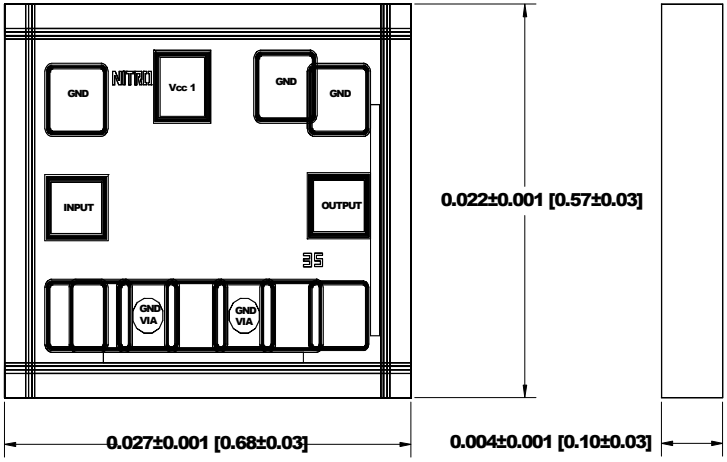




NDA-320-D (Die)

Chip Dimensions: 0.027" X 0.022" X 0.004" Back of chip is ground.

UNITS: INCHES
[mm]



Application Notes

Die Attach:

The die attach process mechanically attaches the die to the circuit substrate. In addition, it electrically connects the ground to the trace on which the chip is mounted, and establishes the thermal path by which heat can leave the chip.

Wire Bonding:

Electrical connections to the chip are made through wire bonds. Either wedge or ball bonding methods are acceptable practices for wire bonding.

Assembly Procedure:

Epoxy or eutectic die attach are both acceptable attachment methods. Top and bottom metalization are gold. Conductive silver-filled epoxies are recommended. This procedure involves the use of epoxy to form a joint between the backside gold of the chip and the metalized area of the substrate. A 150°C cure for 1 hour is necessary. Recommended epoxy is Ablebond 84-1LMI from Ablestik.

Bonding Temperature (Wedge or Ball):

It is recommended that the heater block temperature be set 160°C +/- 10°C.

ESD Sensitive Device