GaInP/GaAs HBT MMIC Distributed Amplifier

DC-11 GHz

NDA-412

6000054 Rev. 1

Features

- Reliable low-cost HBT-based design
- 12 dB Gain, +14.6 dBm P1dB @ 2 GHz
- High P1dB of +14.5 dBm at 6.0 GHz and +10.8 dBm at 14.0 GHz
- Distributed amplifier with fixed gain or Adjustable Gain Control (AGC) operation
- 50 Ω input/output matched for high-frequency utilization
- Low-cost surface mount ceramic package

Description

RF Nitro's NDA-412 GaInP/GaAs HBT MMIC distributed amplifier is a low-cost high-performance solution for your high-frequency RF, microwave, or optical amplification needs. This 50-Ohm matched distributed amplifier is based upon a reliable HBT (Heterojunction Bipolar Transistor) proprietary MMIC design, providing unsurpassed performance for small-signal applications.

The NDA-412 incorporates external dc decoupling capacitors, which limit the low-frequency response. Designed with an external bias resistor, the NDA-412 provides flexibility and stability to your requirement. In addition, the NDA-412 chip was designed with an additional ground via to enable low junction temperature operation. NDA-series distributed amplifiers provide design flexibility by incorporating AGC functionality into their designs.

Applications

- Narrow & broadband commercial & military radio designs.
- Linear & Saturated amplifier applications.
- Gain stage or driver amplifiers, providing AGC capability, utilized in microwave radio and optical designs such as PTP, PMP, LMDS, UNII, VSAT, WLAN, cellular, and 10 & 20 Gbps optical modulator systems.

Package **Ceramic MPGA (Multi-Pin Grid Array)**

Electrical Specifications

V_{cc1}= +10V, V_{cc2}= +10V, V_{c1}=+4.7 V, V_{c2}= +2.98V, I_{cc2} = 36 mA, Zo = 50Ω, T_A = +25 °C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Power Gain, S_{21}	f=0.1 to 4.0 GHz f=4.0 to 6.0 GHz f=6.0 to 8.0 GHz f=8.0 to 11.0 GHz	dB dB dB dB	12.0 10.0	13.0 13.0 13.0 (avg.) 11.0 (avg.)	
Input and Output VSWR	f=0.1 to 4.0 GHz f=4.0 to 8.0 GHz f=8.0 to 11.0 GHz			1.25 2.10 3.50	
Bandwidth - BW	BW3 (3dB)	GHz		12.5	
Output Power @ 1-dB Compression	f=2.0 GHz f=6.0 GHz f=14.0 GHz	dBm dBm dBm		14.6 14.0 10.8	
Noise Figure, NF	f=2.0 GHz	dB		5.0	
3rd Order Intercept, IP3	f=2.0 GHz	dBm		+29.0	
Reverse Isolation, S_{12}	f=0.1 to 11.0 GHz	dB		-16.0	
Output Device Voltage, V_{c2}	.	V	2.70	2.98	3.2
AGC Control Voltage, V_{c1}		V		4.7	
Gain Temperature Coefficient $\partial G_T / \partial T$		$dB/°C$		-0.0015	

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Absolute Maximum Ratings

Exceeding any one or a combination of these limits may cause permanent damage.

Parameter	Absolute Maximum
RF Input Power	+15 dBm
Power Dissipation	300 mW
Device Current, I_{cc1}	42 mA
Device Current, I_{cc2}	42 mA
Junction Temperature, Tj	200° C
Operating Temperature	-45 °C to +85 °C
Storage Temperature	-65 °C to +150 °C

MTTF vs. Temperature @ $P_{TOT, DIS}$ = 245mW

Case Temperature	Junction Temperature	MTTF (hrs)
85 °C	144°C	>1,000,000

Thermal Resistance

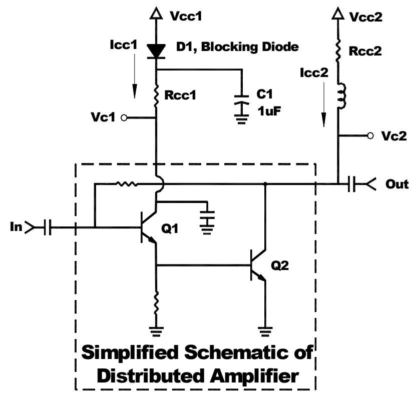
Thermal Resistance, at any temperature (in °C/Watt) can be estimated by the following equation: θ_{JC}(°C/Watt) = 250[T_J(°C) /144]

θ_{JC}	Thermal Resistance	250°C/Watt Typical

Ordering Information

Part Number	Package
NDA-412	Ceramic MPGA

Typical Bias Configuration



Suggested Voltage Supply:

$V_{CC1} \geq 4.7V$

$V_{CC2} \geq 5.0V$

Typical Bias Parameters for Vcc1=Vcc2=10V:							
V_{cc1} (V)	V_{cc2} (V)	I_{cc1} (mA)	V_{c1} (V)	R_{cc1} (Ω)	I_{cc2} (mA)	V_{c2} (V)	R_{cc2} (Ω)
10	10	29	4.75	180	36	2.98	195

Bias Resistor Selection:

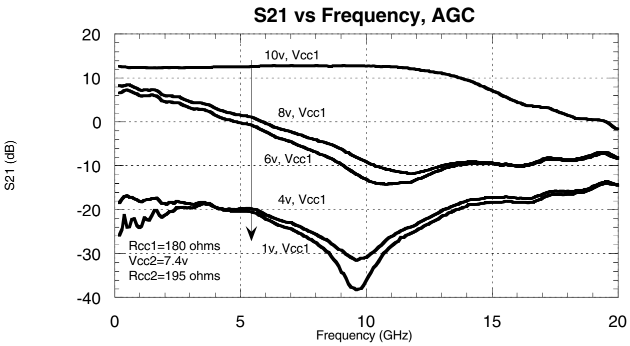
R_{cc1} :

For 4.7V<V_{cc1}<5.0V
R_{cc1}= 0Ω

For 5.0<V_{cc1}<10.0V
$$R_{cc1} = \frac{Vcc1 - 4.7}{0.029}\ \Omega$$

R_{cc2} :

For 5.0<V_{cc2}<10.0V
$$R_{cc1} = \frac{Vcc2 - 2.98}{0.036}\ \Omega$$



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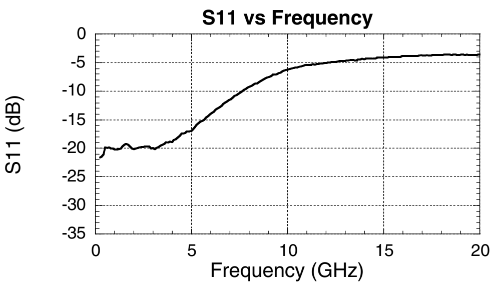
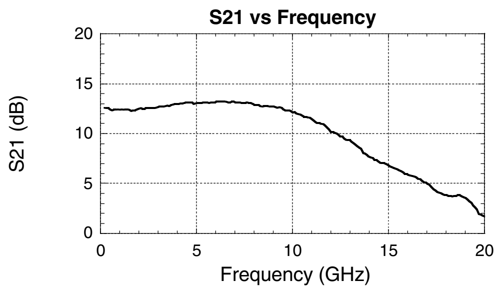
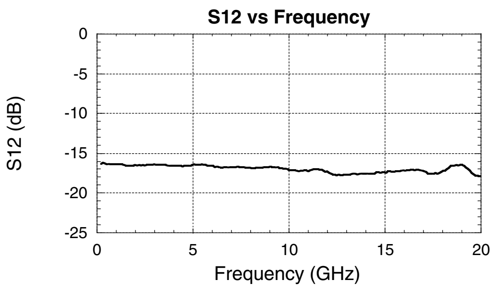
Typical S-Parameter Data V_{cc1}= +10V, V_{cc2}= +10V, V_{c1}=+4.7 V, V_{c2}= +2.98V, I_{cc2} = 36 mA, Zo = 50Ω, T_A = +25 °C

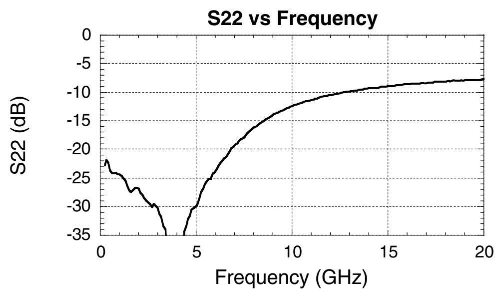
Freq. GHz	S11 (dB)	S11 Mag	S11 Ang	S21 (dB)	S21 Mag	S21 Ang	S12 (dB)	S12 Mag	S12 Ang	S22 (dB)	S22 Mag	S22 Ang
.10	-21.9	0.08	-175.40	12.6	4.28	178.87	-16.5	0.15	-1.02	-23.1	0.07	170.98
.25	-21.9	0.08	-178.27	12.6	4.27	177.30	-15.9	0.16	-1.08	-21.9	0.08	168.14
.50	-20.0	0.10	-176.42	12.4	4.19	174.51	-16.5	0.15	-2.36	-23.1	0.07	153.66
1.0	-20.0	0.10	169.79	12.5	4.20	168.67	-16.5	0.15	-3.32	-24.4	0.06	140.06
2.0	-20.0	0.10	155.45	12.6	4.25	157.56	-16.5	0.15	-4.95	-28.0	0.04	121.34
4.0	-18.4	0.12	141.84	13.0	4.47	135.95	-16.5	0.15	-9.59	-40.0	0.01	147.70
6.0	-13.6	0.21	114.00	13.2	4.58	106.46	-16.5	0.15	-14.98	-23.1	0.07	151.99
8.0	-9.1	0.35	63.91	12.9	4.42	76.16	-17.1	0.14	-18.66	-15.9	0.16	98.44
10.0	-6.2	0.49	3.49	12.2	4.06	45.10	-17.1	0.14	-23.52	-12.4	0.24	33.99
11.0	-5.4	0.54	-30.06	11.4	3.70	29.14	-17.1	0.14	-23.45	-11.4	0.27	0.68

Typical Performance Measurements V_{cc1}= +10V, V_{cc2}= +10V, V_{c1}=+4.7 V, V_{c2}= +2.98V, I_{cc2} = 36 mA, Zo = 50Ω, T_A = +25 °C









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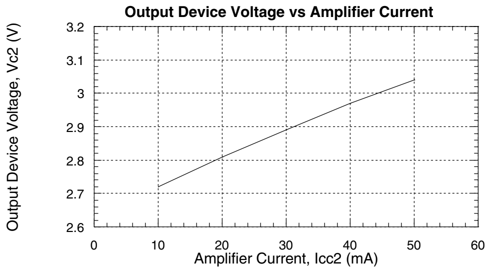
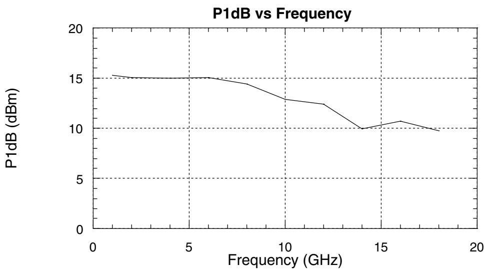
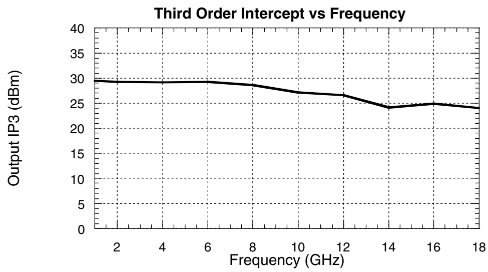
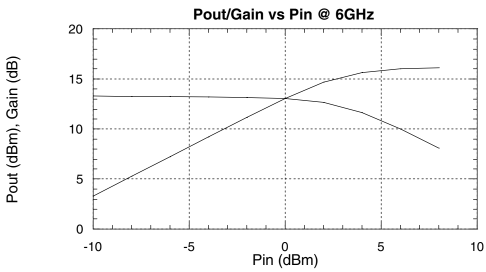
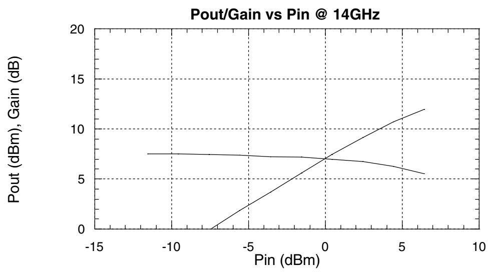

Output Device Voltage vs Amplifier Current
Output Device Voltage, Vc2 (V)
3.2
3.1
3
2.9
2.8
2.7
2.6
0
10
20
30
40
50
60
Amplifier Current, Icc2 (mA)

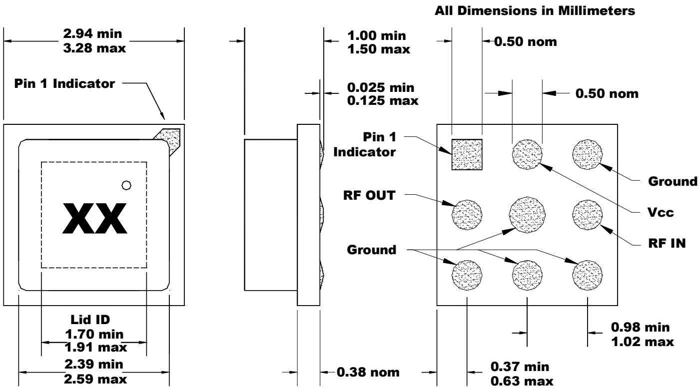

P1dB vs Frequency
P1dB (dBm)
20
15
10
5
0
0
5
10
15
20
Frequency (GHz)


Third Order Intercept vs Frequency
Output IP3 (dBm)
40
35
30
25
20
15
10
5
0
2
4
6
8
10
12
14
16
18
Frequency (GHz)


Pout/Gain vs Pin @ 6GHz
Pout (dBm), Gain (dB)
20
15
10
5
0
-10
-5
0
5
10
Pin (dBm)


Pout/Gain vs Pin @ 14GHz
Pout (dBm), Gain (dB)
20
15
10
5
0
-15
-10
-5
0
5
10
Pin (dBm)

Package Drawing   Ceramic MPGA



Notes: 1. Solder pads are coplanar to within +/- 0.025 mm
2. Lid will be centered relative to frontside metalization with a tolerance of +/-0.13 mm
3. Mark to include two characters and dot to reference pin 1

3 x 3 CERAMIC MPGA - Bowtie Design with Vcc

Application Notes

Die Attach:

The die attach process mechanically attaches the die to the circuit substrate. In addition, it electrically connects the ground to the trace on which the chip is mounted, and establishes the thermal path by which heat can leave the chip.

Wire Bonding:

Electrical connections to the chip are made through wire bonds. Either wedge or ball bonding methods are acceptable practices for wire bonding.

Assembly Procedure:

Epoxy or eutectic die attach are both acceptable attachment methods. Top and bottom metalization are gold. Conductive silver-filled epoxies are recommended. This procedure involves the use of epoxy to form a joint between the backside gold of the chip and the metalized area of the substrate. A 150°C cure for 1 hour is necessary. Recommended epoxy is Ablebond 84-1LMI from Ablestik.

Bonding Temperature (Wedge or Ball):

It is recommended that the heater block temperature be set at 160°C +/- 10°C.

ESD Sensitive Device