Product Brief
June 2001

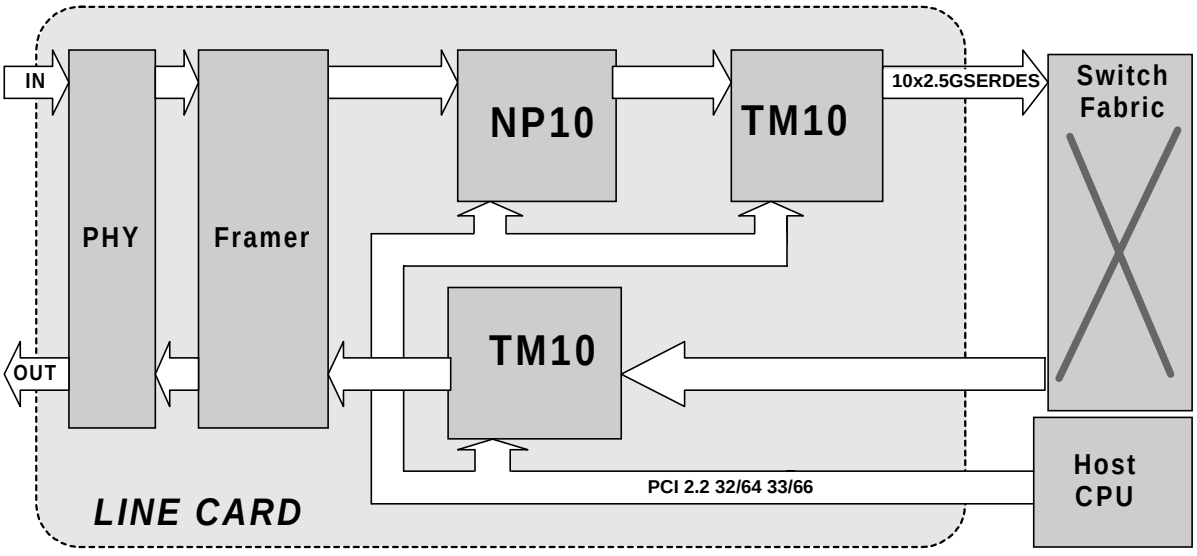
NP10 and TM10 Network Processors

Introduction

The Agere Systems *PayloadPlus*™ 10G Network Processor chip set provides wire-speed deep-packet processing for high performance packet-processing systems. This software-compatible, programmable chip set consists of two chips—the NP10 classification engine and the TM10 traffic manager—and follows the successful Agere Systems 2.5G *PayloadPlus* chip set.

This 10G chip set provides full carrier-class packet processing functionality, including classification, policing, statistics, queueing, scheduling, shaping, buffer management and packet/cell modification. A three-chip configuration—one NP10 and two TM10s—provides full duplex 10 Gb/s packet processing functionality. An additional NP10 can be added if egress classification is required. The 10G *PayloadPlus* solution requires only DRAM and a small amount of SRAM for external memory to provide high-performance functionality. No content addressable memory (CAM) is required.

The chip set supports complex packet classification policies, including multifield IPv4/IPv6 classification, PPPoE, L2TP, MPLS, etc., with a large amount of headroom for future classification needs. OEMs use the Agere Systems high-level Functional Programming Language (FPL) to specify packet classification policies. Statistics, policing, and packet modification functions are performed by on-chip compute engines that are programmed using the C-like Agere Scripting Language (ASL).



10G Network Processor System Diagram

Features

- Full line-rate performance with all packet sizes greater than or equal to 40 bytes long
  - — Supports complex multifield packet classification with a large amount of headroom for future classification needs.
  - — Supports wire-speed access control list (ACL) processing, even with thousands of ACL rules.
- Multiprotocol customer-programmable classification:
  - — POS, MPLS, IPv4/v6, ATM, Frame Relay, Ethernet, VLANs, access control lists, link aggregation, etc. OEMs can easily supplement the protocols and standards they support with simple software upgrades.
- DRAM-based classification rule memory supports over 1 million IPv4 routes with separate information for each VPN. No CAMs are required.
- Uses high-level network processor programming languages—Functional Programming Language (FPL) and Agere Scripting Language (ASL)—preserving investments in classification, policing, statistics, and packet modification programming. FPL provides an order of magnitude reduction (compared to C/C++) in the number of lines of code required to specify packet classification policies. FPL eliminates the need for complex hand-optimization of assembly or microcode to achieve wire-speed performance.
- Programmable per-flow statistics and policing allows OEMs to implement highly differentiated admission control and billing policies.
- Full carrier-class traffic management functionality to help maximize the amount of premium traffic that can be reliably served, with support for:
  - — Hierarchical weighted fair queuing (WFQ) with bandwidth and delay guarantees
  - — VPNs with traffic isolation and service-level agreements (SLAs)
  - — Dynamic bandwidth and QoS/CoS modification to enable real-time dynamic service provisioning
  - — 2 million packet handling behavior types with 3 buffer management profiles per behavior type to allow fine-grained service differentiation
  - — Random early detection (RED) and weighted RED (WRED)
  - — Up to 256 MB of external packet buffer memory per direction
  - — External scheduling port to allow OEMs to support proprietary switch fabric implementations (for example, credit-based flow control, global scheduling) and/or proprietary packet scheduling implementations.
- Programmable packet modification, including support for:
  - — Adding/removing software-defined headers and trailers
  - — Modifying data anywhere in the packet
  - — Forward congestion marking
- Wire-speed IP fragmentation
- Full multicast support with ability to individually schedule and modify each packet/cell copy
- Port based rate shaping for up to 256 media ports
  - — Configurations include OC192c, 4xOC48c, 1G/10G Ethernet, 192xDS3, etc.
- PCI 2.2 compliant 66-MHz, 32-/64-bit host interface to allow easy interfacing to a variety of host microprocessors and other support logic
- Both cell- and frame-based fabrics supported with programmable classification/segmentation/reassembly. OEMs can readily interface to a wide variety of switch fabrics with minimal glue logic effort.
- Support for simple interface to third-party fabrics using the Agere Systems Field Programmable System-on-a-Chip devices
- Complete Agere Systems 10G fiber-to-fabric line card reference design with supporting software
- FPGA-based hardware emulation system and software simulator provides complete pre-silicon hardware and software development support.

Applications

Target applications include multiprotocol core and edge switches and routers, multiservice optical core and edge devices and service-aware switches and provisioning platforms.

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PB01-137NP