NLB0136

NEL
NTT Electronics corp.

Advanced product information

QoS-Monitor LSI for SDH signals (Version4.2)

Suggested Spec.

Description

The NLB0136 detects B1 errors in STM-1 (155.52Mbps)／STM-4 (622.08Mbps)／STM-16 (2.488Gbps) in the received SDH signals using B1 byte to check the quality of the transmission system. It also extracts the section trace messages (J0 byte).

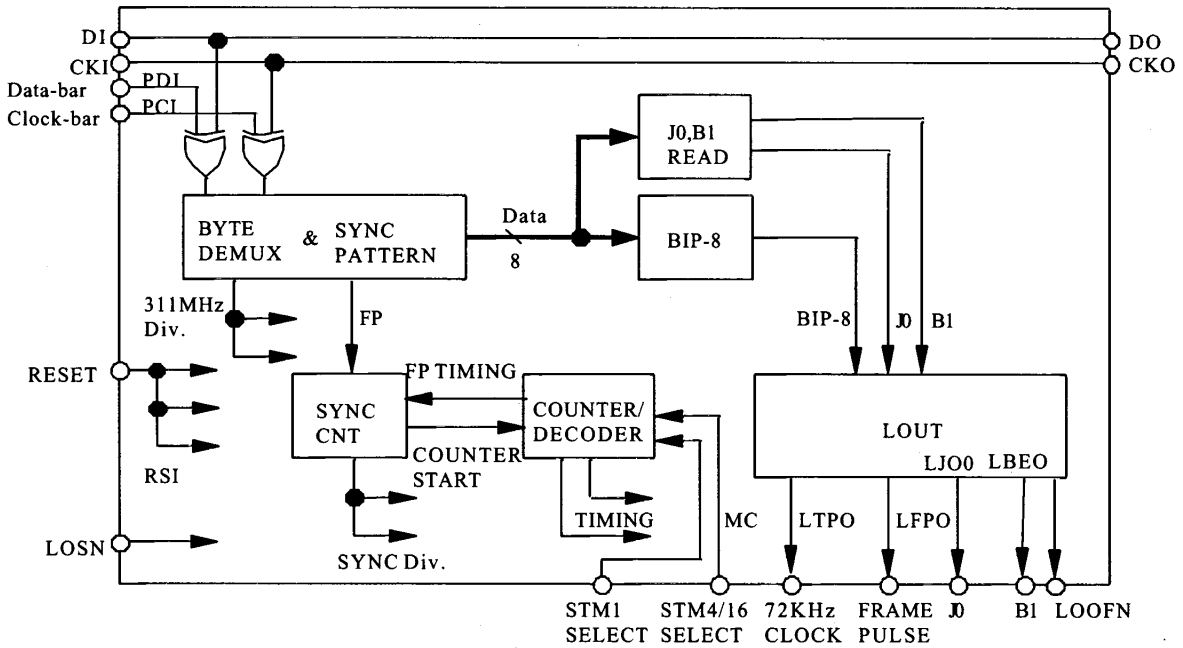
Features

1. Provides a serial interface of speeds up to 2.488Gbps
2. Synchronizes the SDH frame using A1 and A2 byte
3. Calculates BIP-8 code to detect B1 errors
4. Extracts the section trace messages (J0 byte)
5. Provides PECL／LVTTL logic levels
6. Supplies +3.3V
7. Packaged in 48-pin-QFP

Applications

1. SONET／SDH Add／Drop Multiplexers
2. SONET／SDH Terminal Multiplexers
3. SONET／SDH Routers and Switches

Block Diagram



Functional Description

1. Byte DEMUX

Detects the byte boundary of the received serial data searching the framing bytes (A1,A2) and demultiplexes (1:8) the data. Once the framing bytes are detected, it continues to demultiplexes the data with the same timing. When it comes back to the initial state of the state-machine, it restarts to search the DEMUX timing.

2. Synchronization Pattern Detector / Synchronization Control

Informs the detection that demultiplexed succeeding four bytes are A1, A1, A2 and A2 to synchronization control circuit. It is impossible to restart the synchronization capturing immediately after frame off-synchronization situation, because frame synchronization is executed after byte synchronization.

Backward protection of two stages and forward protection of five stages are implemented.

3. Section BIP-8 Error Monitoring (B1)

The B1 byte implements a BIP-8 error code, which is a bit interleaved calculation using even parity. The BIP-8 code is computed over all bits in the previous frame after scrambling and then compared with the extracted B1 error code from the following incoming frame. Any bit mismatches indicate an error.

4. Extraction of J0 and B1 byte

Extracts J0 and B1 byte from the incoming frame.

5. Low speed output

Outputs the following five signals.

(1) LTPO : 72kHz clock output

(2) LFPO : Frame pulse output (8kHz) synchronized to the rising edge of LTPO

(3) LOOFN : Frame synchronization status

When LOOFN is high, the frame is detected.

When LOOFN is low, the frame is not detected.

(4) LJ0O : Frame synchronization status and serial J0 data output synchronized to the rising edge of LTPO.

LOOFN(b0 bit) comes first and then serial J0 data (8 bit) comes after b0 bit.

9 bits are transmitted in 125us.

(5) LBEO : Frame synchronization status and serial BIP-8 result output synchronized to the rising edge of LTPO.

LOOFN(b0 bit) comes first and then serial BIP-8 result (8 bit) comes after b0 bit.

9 bits are transmitted in 125us.

6. Inversion of clock and data inputs

Asserts PCI to invert the clock input (CKI).

Asserts PDI to invert the data input (DI).

Pin Connection Table

Pin	Signal Name	I/O	Level	Function
No.1	VCC	PWR	+3.3V	
2	GND	PWR	0V	
3	LOOFN	O	LVTTL	Out of Frame Output Signal. (In Low level)
4	LBEO	O	LVTTL	Error detection value
5	LJ0O	O	LVTTL	J0 read out value
6	GND	PWR	0V	
7	VCC	PWR	+3.3V	
8	LFPO	O	LVTTL	Frame pulse
9	LTPO	O	LVTTL	Serial output clock
10	(VCS1)	I	—	(Will be Vref1 Input for Internal cell)
11	GND	PWR	0V	
12	VCC	PWR	+3.3V	
13	(VCS2)	I	—	(Will be Vref2 Input for I/O cell)
14	GND	PWR	0V	
15	TDCK	I	LVTTL	Test Pin (Normary OPEN)
16	TCCK	I	LVTTL	Test Pin (Normary OPEN)
17	VCC	PWR	+3.3V	
18	LOSN	I	LVTTL	Loss of Signal (In Low level)
19	GND	PWR	0V	
20	TMD	I	LVTTL	Test Pin (Normary GND)
21	PCI	I	LVTTL	Clock inverse (In high level)
22	VCC1	PWR	+3.3V	Power supply for Clock Output buffer
23	CKO	O	AC	Clock through output (AC-coupling)
24	VCC2	PWR	+3.3V	Power supply for Clock Output buffer
25	VCC	PWR	+3.3V	
26	GND	PWR	0V	
27	VTT1	PWR	+2.0V	Reference Voltage for CKI (VTT=2.0V)
28	CKI	I	AC	Clock Input (Internal 50Ω to VTT)
29	VTT2	PWR	+2.0V	Reference Voltage for CKI (VTT=2.0V)
30	VCC	PWR	+3.3V	
31	GND	PWR	0V	
32	VTT3	PWR	+2.0V	Reference Voltage for DI (VTT=2.0V)
33	DI	I	AC	Data Input (Internal 50 Ω to VTT)
34	VTT4	PWR	+2.0V	Reference Voltage for DI (VTT=2.0V)
35	GND	PWR	0V	
36	VCC	PWR	+3.3V	
37	VCC3	PWR	+3.3V	Power supply for Data Output buffer
38	DO	O	AC	Data through output (AC-coupling)
39	VCC4	PWR	+3.3V	Power supply for Data Output buffer
40	PDI	I	LVTTL	Data inverse (In high level)
41	RSI	I	LVTTL	Reset (In high level)
42	VCC	PWR	+3.3V	
43	GND	PWR	0V	
44	VCC	PWR	+3.3V	
45	MC	I	LVTTL	Selection of STM-4 or STM-16.H:STM-16 L:STM-4
46	STM1	I	LVTTL	Selection of STM-1 H:STM-1 L:Depend on MC
47	VCC	PWR	+3.3V	
48	GND	PWR	0V	

Suggested Spec.

Absolute Maximum Ratings

GND=0V

Symbol	Parameter	Ratings	Unit
V_{CC}	V_{CC} Supply Voltage to GND pin	-0.3 ~+4.0	V
V_{TT}	V_{TT} Supply Voltage to GND pin	-0.3 ~+3.6	V
V_{IAC}	AC Input Voltage	2.6	Vpp
V_{ITTL}	TTL Input Voltage	-0.3 ~+4.0	V
I_{OTTL}	TTL Output Current	-24	mA
T_{stg}	Storage Temperature	-65~+150	℃
T_j	Maximum Junction Temperature	+150	℃

Stress greater than these conditions may cause permanent damage to the device or affect its reliability.

Recomended Operating Conditions

GND=0V

Symbol	Parameter	Ratings	Unit
V_{CC}	Power Supply Voltage	+3.3±5%	V
V_{TT}	AC Input Termination Voltage	+2.0	V
Rt	AC Output Termination Resistor	50	Ω
T_c	Operating Case Temperature	0~+85	℃

The device should be operated under these conditions,beyond which the parametric values are not specified.

DC Characteristics

Power Supply Current

V_{CC}=+3 .3V±5%, GND=0V, V_{TT}=+2.0V, Tc=0 ~85℃

Sym.	Characteristics	Min.	Typ.	Max.	Unit	Conditions
I_{cc}	Power Supply Current	TBD	395	TBD	mA	Outputs Open

TTL Inputs and Outputs

T.B.D:To Be Determined

V_{CC}=+3.3V, GND=0V, V_{TT}=+2.0V, Tc=0 ~85℃

Sym.	Characteristics	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.2	–	–	V	I_{OH}=-0.4mA
V_{OL}	Output Low Voltage	0	–	0.4	V	I_{OL}=8mA
V_{IH}	Input High Voltage	2.0	–	Vcc	V	---
V_{IL}	Input Low Voltage	0	–	0.8	V	---
I_{IH}	Input High current	–	–	40	μA	V_{IN}=2.4V
I_{IL}	Input Low current	-0.4	–	–	mA	V_{IN}=0.4V

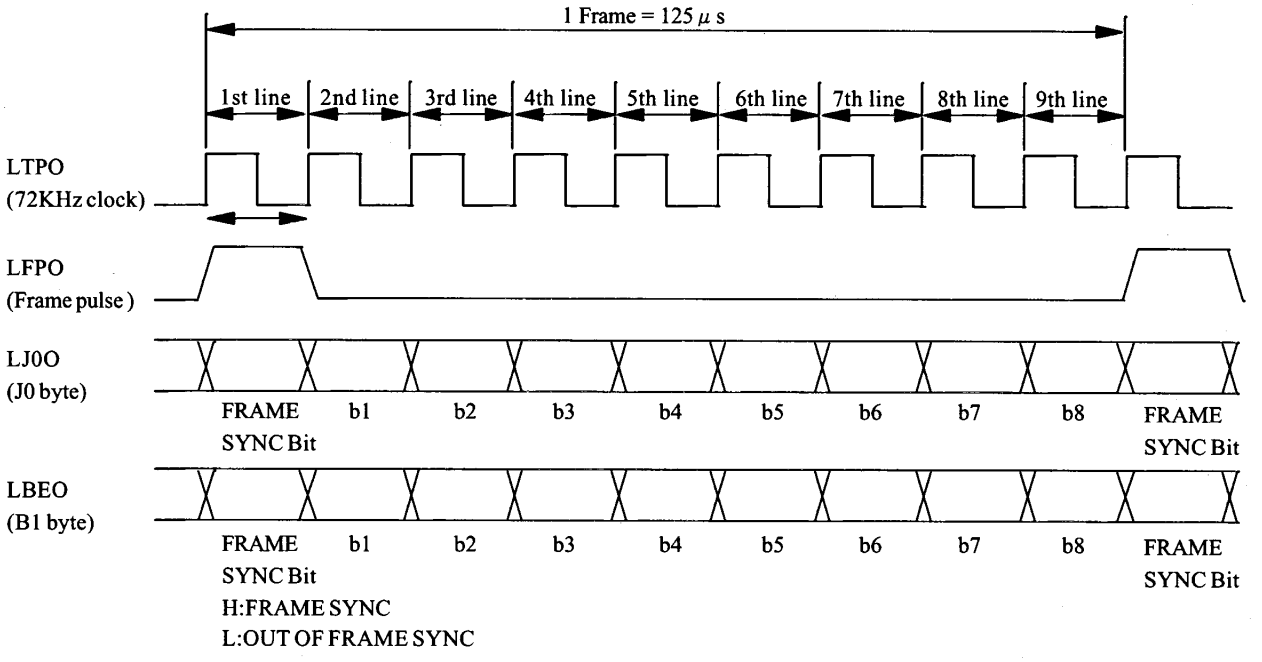
AC Characteristics

V_{CC}=+3.3V, GND=0V, V_{TT}=+2.0V, Tc=0 ~85℃

Sym.	Characteristics	Min.	Typ.	Max.	Unit	Conditions
V_{ODO}	Data Output Voltage Swing	T.B.D	600	T.B.D	mVpp	AC Coupled
V_{OCO}	Clock Output Voltage Swing	T.B.D	600	T.B.D	mVpp	AC Coupled
V_I	Input Voltage Swing	350	–	T.B.D	mVpp	AC Coupled
t_{rd}	Output Rise Time	–	150	T.B.D	ps	CKO, 2.48832GHz, 20-80%
t_{fd}	Output Fall Time	–	150	T.B.D	ps	CKO, 2.48832GHz, 20-80%
t_{rc}	Output Rise Time	–	80	T.B.D	ps	DO, 2.48832Gbps, 20-80%
t_{fc}	Output Fall Time	–	80	T.B.D	ps	DO, 2.48832Gbps, 20-80%
t_s	Minimum Setup Time	–	0	T.B.D	ps	DI to CKI, 2.48832GHz
t_h	Minimum Hold Time	–	130	T.B.D	ps	CKI to DI, 2.48832GHz
phm	Phase Margin	T.B.D	270	–	ps	CKI, 2.48832GHz
skwv	Skew Variation	T.B.D	20	T.B.D	ps	CKO to DO

T.B.D:To Be Determined

Timing Chart



Behavior of low speed output signals

- LFPO,LFPO,LJ0O and LBEO change at the rising edge of LTPO.
- CPU reads LFPO, LJ0O and LBEO at the falling edge of LTPO.
- LFPO becomes "1" in the cycle of 9 bits (100000000100...). But not in the case of synchronization capture.
- LJ0O and LBEO make their first bit when LFPO is "1", 9 bits are put out in each frame.
- The first bit of LJ0O and LBEO are synchronization bit.
- The synchronization bit = "1" means the synchronized status, on the other hand, the synchronization bit ="0" means off-synchronized status.
- The second bit of LJ0O is the MSB of J0 byte, and the ninth bit of LJ0O is the LSB of J0 byte.
- The second bit of LBEO is the MSB of B1 error byte, and the ninth bit of LBEO is the LSB of B1 error byte.
- The number of code error in one frame equals to the number of bit "1" in the resultant byte of the above Ex- OR operation.

Package Dimension (mm)