

NLB6221

NEL
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Quad D Flip-Flop with Master Reset

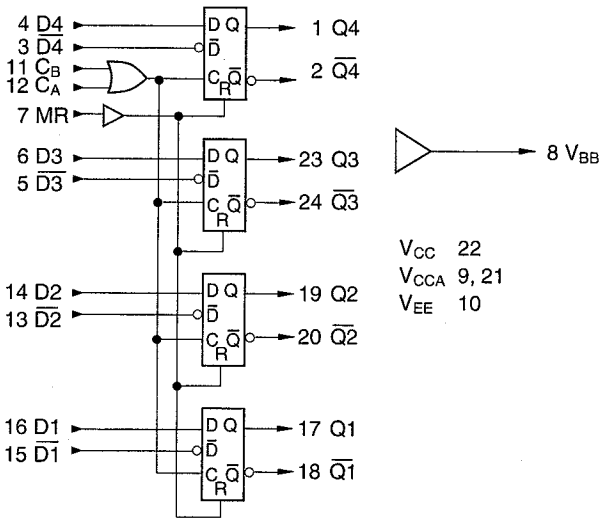
Description

The NLB6221 is an ultra high-speed monolithic quad D Flip-Flops with common 2 clock inputs and a direct master reset.

Features

- Typical clock rate up to 3.7 GHz.
- Internal pull down resistors on input pins (MR, C_A, C_B, D_n) to maintain logic LOW level with the pins left open.
- Internal pull up resistor on input pin ($\overline{D_n}$) to maintain logic HIGH level with the pin left open.
- ECL 100K compatible I/O levels.
- Differential outputs.

Logic Symbol

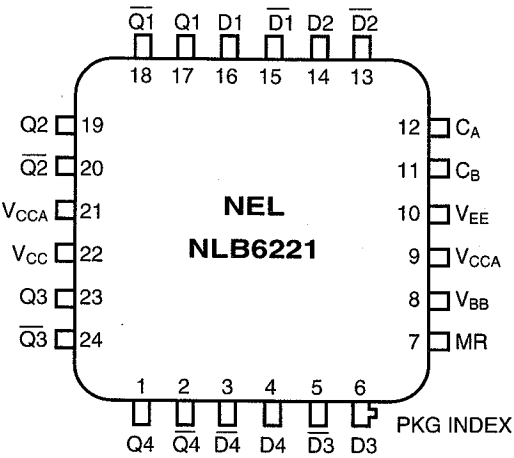


Truth table

Input			output			
MR	C _A	C _B	Q ₁	Q ₂	Q ₃	Q ₄
H	X	X	L	L	L	L
L	$\lceil$	L	D ₁	D ₂	D ₃	D ₄
L	L	$\lceil$	D ₁	D ₂	D ₃	D ₄
L	$\lceil$	$\lceil$	D ₁	D ₂	D ₃	D ₄

H : High voltage level
L : Low voltage level
X : Arbitrary
 $\lceil$: L to H transition

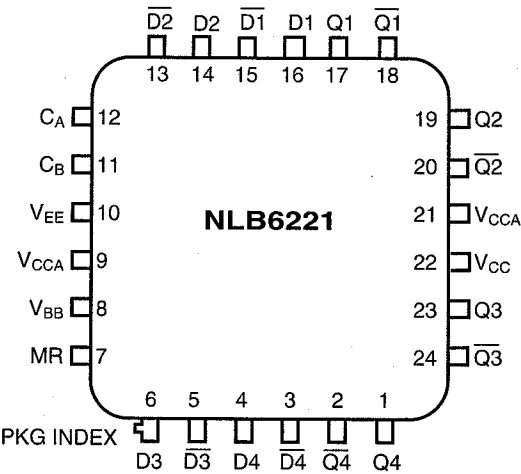
Pin Assignment Top View (Ceramic)



Pin Name

D _n , $\overline{D_n}$	Data inputs
C _A , C _B	Clock inputs
MR	Master direct reset
Q _n , $\overline{Q_n}$	Data outputs
V _{BB}	Reference voltage output
V _{CC}	Circuit GND
V _{CCA}	Circuit GND for outputs
V _{EE}	-4.5V

Back View (Metal Cap)



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DC Characteristics

$V_{EE} = -4.5V \pm 0.3V$, $V_{CC} = V_{CCA} = GND$, $V_{TT} = -2V$, $T_c = 0^{\circ}C$ to $+85^{\circ}C$, $R_T = 50\Omega$ to V_{TT}

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}	100	170	225	mA

AC Characteristics

$V_{EE} = -4.5V \pm 0.3V$, $V_{CC} = V_{CCA} = GND$, $V_{TT} = -2V$, $T_c = 0^{\circ}C$ to $+85^{\circ}C$, $R_T = 50\Omega$ to V_{TT}

Characteristics	Symbol	Input	output	Test condition	Min.	Typ.	Max.	Unit
Propagation delay time	t _{PLH}	Cx	Qn			630	840	ps
	t _{PHL}					590	780	
	t _{PLH}	MR				670	890	
	t _{PHL}					690	910	
Setup time	t _s	Dn,Cx			110	70		
Hold time	t _h	Dn,Cx			250	180		
Release time	t _r	MR,Cx			600	450		
Minimum pulse width	t _{pw}	MR			490	370		
Maximum operating frequency	f _{max}	Cx		2.8	3.7		GHz	
Rise time	t _r	Cx	20 to 80%		140	190	ps	
Fall time	t _f				140	190		