NLB6223 Quad Flip Flop with 2 : 1 Selector

NEL SELIC

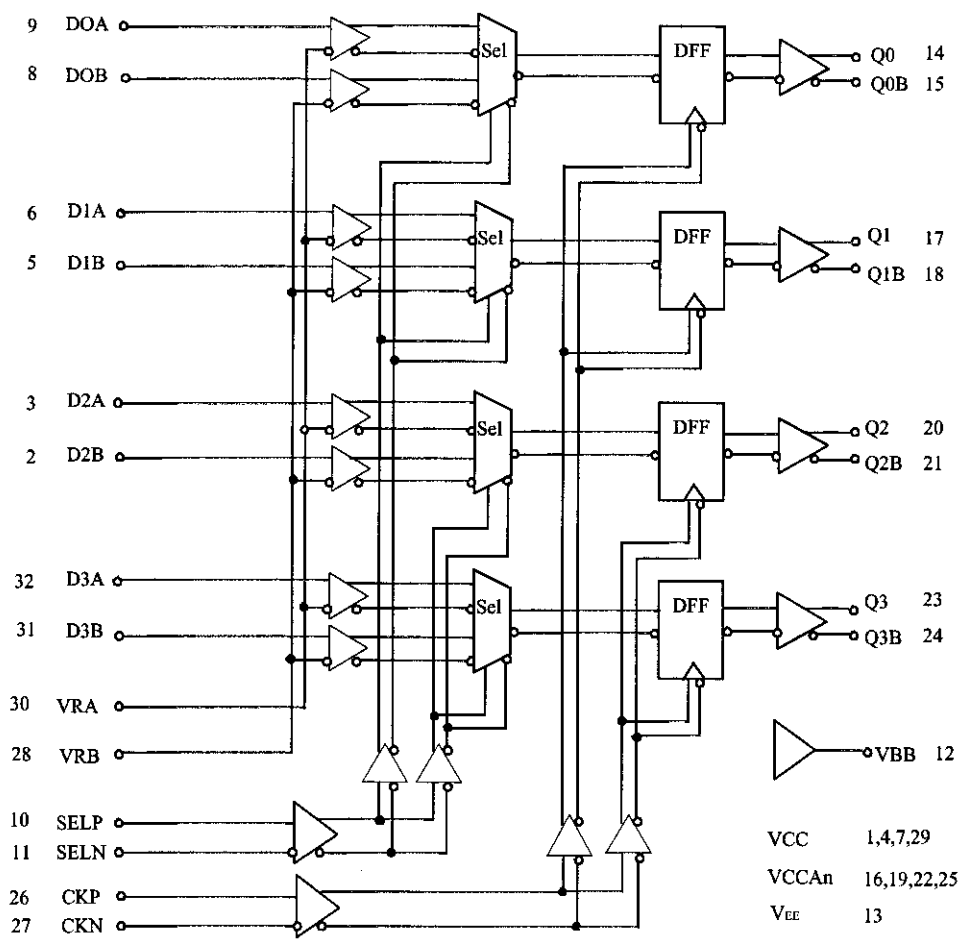
Description

The NLB6223 is an ultra high-speed monolithic quad D Flip-Flops with 2:1 Selector.

Features

- Typical clock rate up to 2.0 GHz.
- Internal pull down resistors on input pins (DnA, DnB,SELP, CKP) to maintain logic LOW level with the pins left open.
- Internal pull up resistor on input pin (SELN, CKP) to maintain logic HIGH level with the pin left open.
- ECL100K compatible I/O levels.
- Differential outputs.

Logic Symbol



Truth table

NLB6223 Truth table

Input						Output	
DnA	DnB	SELP	SELN	CKP	CKN	Qn	QnB
X	0	0	1	↑	↓	0	1
X	1	0	1	↑	↓	1	0
0	X	1	0	↑	↓	0	1
1	X	1	0	↑	↓	1	0

Pinconection Table

Pin No	Pin Name	I/O	Function	Pin No	Pin Name	I/O	Function
1	VCC	P	Circuit GND	17	Q1	O	Data output
2	D2B	I	Data input	18	Q1B	O	Data output
3	D2A	I	Data input	19	VCCA1	P	Ajust for Q1/Q1B(GND)
4	VCC	P	Circuit GND	20	Q2	O	Data output
5	D1B	I	Data input	21	Q2B	O	Data output
6	D1A	I	Data input	22	VCCA2	P	Ajust for Q2/Q2B(GND)
7	VCC	P	Circuit GND	23	Q3	O	Data output
8	D0B	I	Data input	24	Q3B	O	Data output
9	D0A	I	Data input	25	VCCA3	P	Ajust for Q3/Q3B(GND)
10	SELP	I	Select data input (True)	26	CKP	I	Clock Input(True)
11	SELN	I	Select data input (Comp.)	27	CKN	I	Clock Input(Comp.)
12	VBB	O	Reference voltage output	28	VRB	I	Reference voltage input
13	VEE	P	VEE(-4.5V)	29	VCC	P	Circuit GND
14	Q0	O	Data output	30	VRA	I	Reference voltage input
15	Q0B	O	Data output	31	D3B	I	Data input
16	VCCA0	P	Ajust for Q0/Q0B(GND)	32	D3A	I	Data input

P : Power Supply, I : Inputs, O : Outputs

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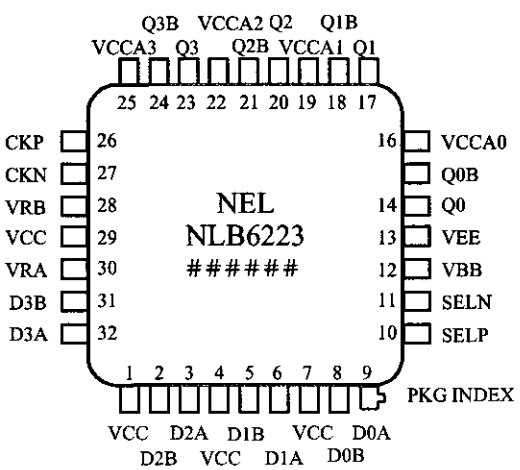
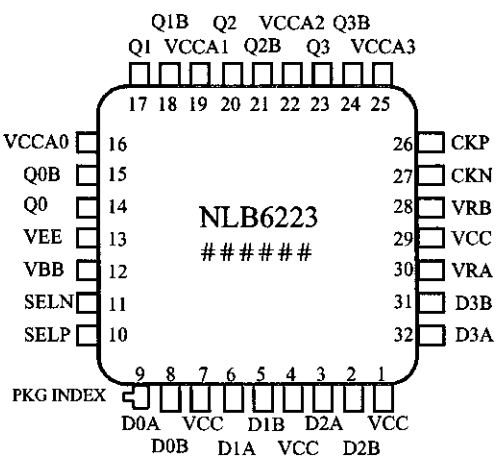
PinAssignment

Top View(Ceramic)



Back View(Metal Cap)



Pin name

VCC	Circuit GND
VEE	Supply voltage -4.5V
VBB	Reference voltage output
VRA	Reference voltage input for DnA
VRB	Reference voltage input for DnB
SELP	Select data Input(True)
SELN	Select data Input(Comp.)
CKP	Clock Input(True)
CKN	ClockInput(Comp.)
DnA/DnB	Data input
Qn/QnB	Data output
VCCAn	Ajust for Qn/QnB(GND)

Electric Characteristics

Absolute Maximum Ratings

V_{CC}=GND

Symbol	Parameter	Ratings	Unit
V_{EE}	V_{EE} Supply Voltage to GND pin	+0.3~-6.0	V
V_I	Input Voltags	0~-3	V
Io	Output Current	-50	mA
T_{stg}	Storage Temperature	-65~+150	℃
T_j	Maximum Junction Temperature	+150	℃
V_{CCAn}	Input Voltags	-200~+200	mV

Stress greater than these conditions may cause permanent damage to the devices or affect their reliability. Input teminal should not be connected to V_{EE} for logic LOW level. Low voltage level is maintained with input pins left open.

Recommended Operating Conditions

V_{CC}=V_{CCAn}=GND

Symbol	Parameter	Ratings	Unit
V_{EE}	Power Supply Voltage	-4.5±0.3	V
R_T	Output Temination to V_{TT} = -2V	45~50	Ω
T_c	Operatinig Case Temperature	0~+85	℃

The device should be operated under these conditions,beyond which the parametric values are not specified.

DC Characteristics

V_{EE}=-4.5V V_{CC}=GND, R_L=50Ω to V_{TT}=-2.0V, Tc=0~85℃

Sym.	Characteristics	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	-1025		-880	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=GND
V_{OL}	Output Low Voltage	-1810		-1620	mv	
V_{OH}	Output High Voltage	-825		-680	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=+200mV
V_{OL}	Output Low Voltage	-1610		-1420	mv	
V_{OH}	Output High Voltage	-1225		-995	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=-200mV
V_{OL}	Output Low Voltage	-2010		-1820	mv	
V_{IH}	Input High Voltage	-1165		-880	mv	Guaranteed H Signal for ALL Input
V_{IL}	Input Low Voltage	-1810		-1475	mv	Guaranteed L Signal for ALL Input
I_{IH}	Input High Current		130	230	μA	V_{IN}=V_{IH}(max)

Notes:V_{CCAn} refere to fig.1

V_{EE}=-4.2V V_{CC}=GND, R_L=50Ω to V_{TT}=-2.0V, Tc=0～85℃

Sym.	Characteristics	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	-1020		-870	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=GND
V_{OL}	Output Low Voltage	-1790		-1605	mv	
V_{OH}	Output High Voltage	-820		-670	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=+200mV
V_{OL}	Output Low Voltage	-1590		-1405	mv	
V_{OH}	Output High Voltage	-1220		-985	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=-200mV
V_{OL}	Output Low Voltage	-1990		-1805	mv	
V_{IH}	Input High Voltage	-1150		-870	mv	Guaranteed H Signal for ALL Input
V_{IL}	Input Low Voltage	-1790		-1475	mv	Guaranteed L Signal for ALL Input
I_{IH}	Input High Current			230	μA	V_{IN}=V_{IH}(max)

Notes:V_{CCAn} refere to fig.1

V_{EE}=-4.8V V_{CC}=GND, R_L=50Ω to V_{TT}=-2.0V, Tc=0～85℃

Sym.	Characteristics	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	-1035		-880	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=GND
V_{OL}	Output Low Voltage	-1840		-1620	mv	
V_{OH}	Output High Voltage	-835		-680	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=+200mV
V_{OL}	Output Low Voltage	-1640		-1420	mv	
V_{OH}	Output High Voltage	-1235		-1005	mv	V_{IN}=V_{IH}(max)orV_{IL}(min),V_{CCAn}=-200mV
V_{OL}	Output Low Voltage	-2040		-1820	mv	
V_{IH}	Input High Voltage	-1165		-880	mv	Guaranteed H Signal for ALL Input
V_{IL}	Input Low Voltage	-1840		-1495	mv	Guaranteed L Signal for ALL Input
I_{IH}	Input High Current			230	μA	V_{IN}=V_{IH}(max)

Notes:V_{CCAn} refere to fig.1

V_{EE}=-4.5V±0.3v,V_{CC}=GND,V_{CCAn}=0v±0.3v, R_L=50Ω to V_{TT}=-2.0V, Tc=0～85℃

Charactaristics	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current	I_{EE}	137	205	273	mA

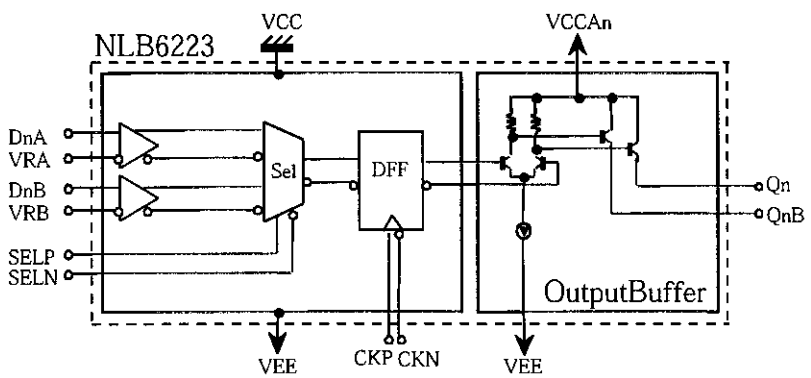


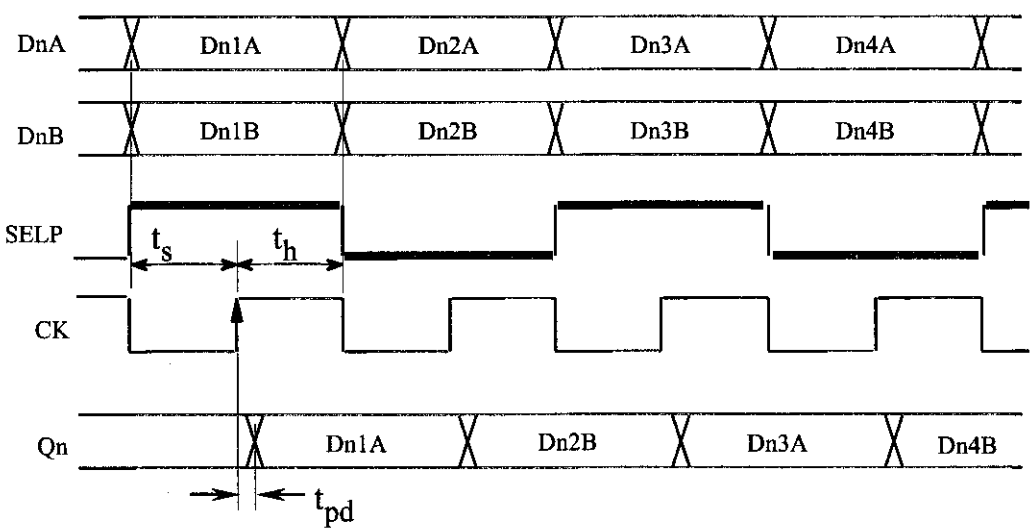
fig.1 VCCAn and Output Buffer circuit

AC Characteristics

V_{EE}=-4.5V±0.3V, V_{CC}=V_{CCAn}=GND, R_T=50Ω to GND, Tc=0~85℃

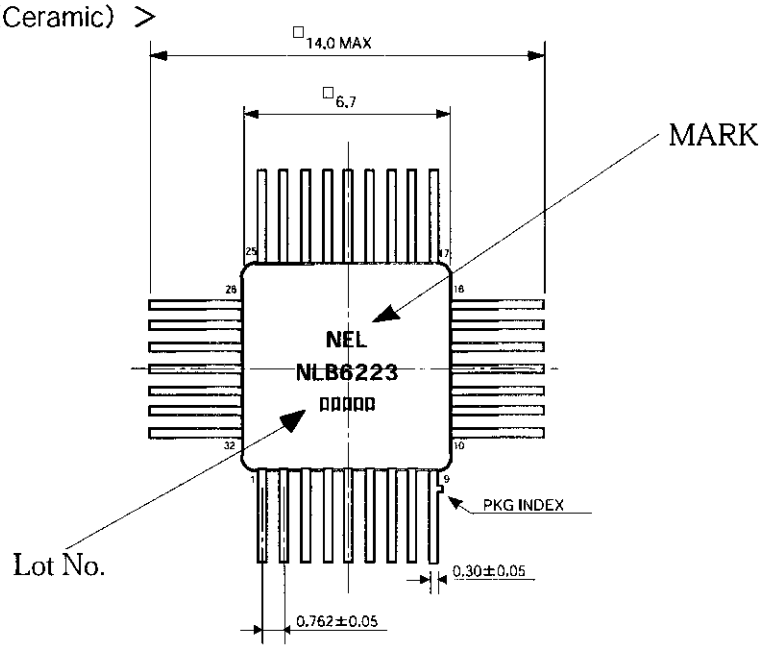
Chracteristics	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time	t_{PLH}	CK	Q_n	SELP=H	—	510	680	ps
	t_{PHL}				—	480	640	
	t_{PLH}	CK		SELP=L	—	500	670	
	t_{PHL}				—	480	640	
Setup time	t_s	DnA,CK		SELP=H	—	60	80	
		DnB,CK		SELP=L	—	60	80	
Hold time	t_h	DnA,CK		SELP=H	—	160	220	
		DnB,CK		SELP=L	—	160	220	
Maximum operating frequancy	f_{max}	CK			1.6	2.0	—	GHz
Rise time	t_r	DnA,DnB		20% to 80%	—	130	180	ps
Fall time	t_f	DnA,DnB		20% to 80%	—	130	180	

Timing Chart

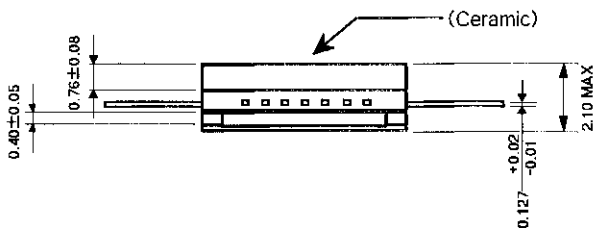


Package Dimension

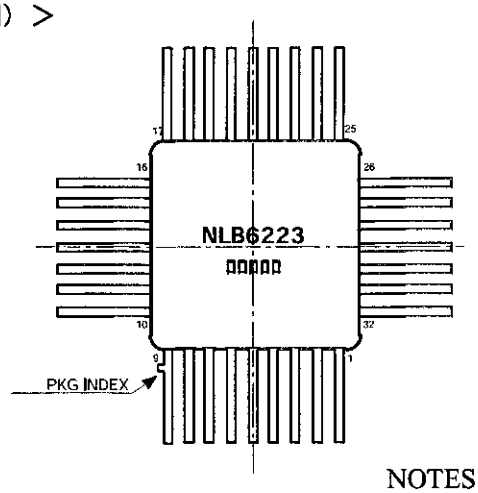
<TOP VIEW (Ceramic) >



<SIDE VIEW>



<BACK VIEW (Metal) >



NOTES
1.DIMENSIONS ARE SPECIFIED IN mm.
2.TOLERANCES : XX±0.10