NLB6255

NEL
SELIC

8 bit Demultiplexer

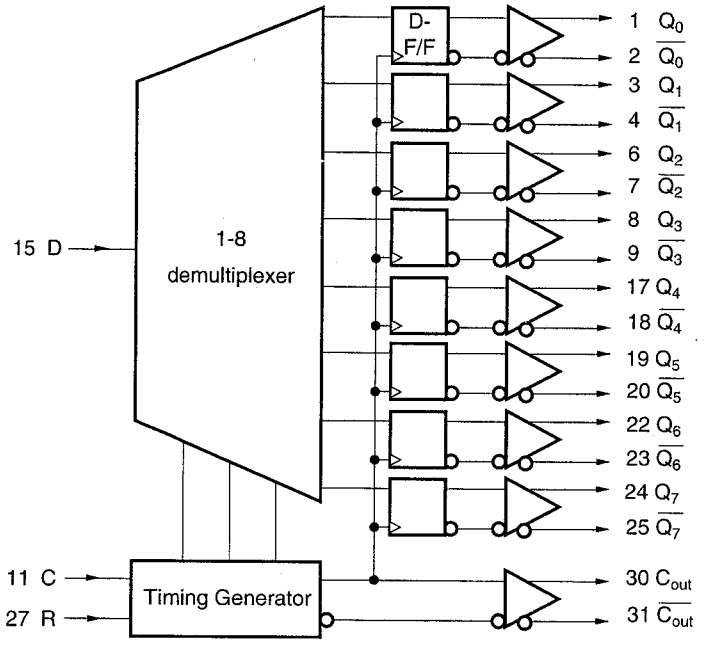
Description

The NLB6255 is an ultra high-speed monolithic 8 bit demultiplexer.

Features

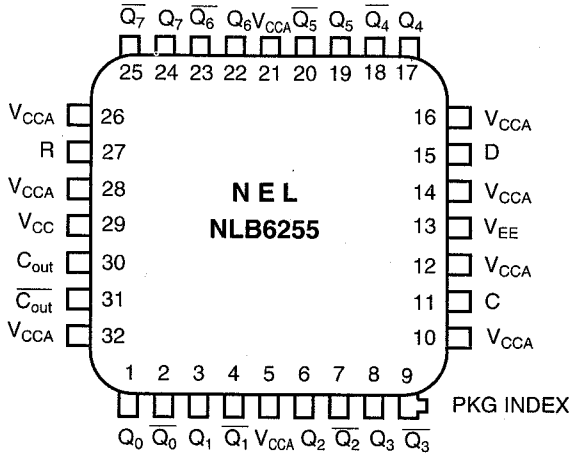
- Typical AC characteristics
  Clock rate up to 3 GHz.
  t_r=165ps
  t_f=165ps
- Internal pull down resistors on input pins (R, D, C) to maintain logic LOW level with the pins left open.
- ECL 100K compatible I/O levels.
- Differential outputs.

Logic Symbol



V_{CC}	29
V_{CCA}	5,10,12,14,16,21,26,28,32
V_{EE}	13

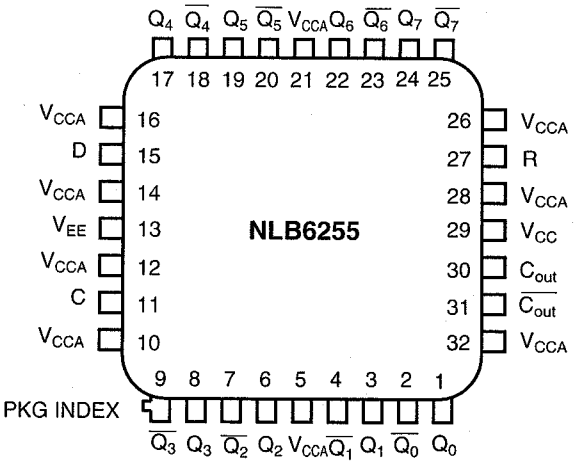
Pin Assignment
Top View (Ceramic)



Pin Name

D	Serial data input
C	Clock input
R	Reset input
Q_n, $\overline{Q_n}$	Parallel data output
C_{out}, $\overline{C_{out}}$	1/8 clock output
V_{CC}	Circuit GND
V_{CCA}	Circuit GND for outputs
V_{EE}	-4.5V

Back View (Metal Cap)



NLB6255 8 bit Demultiplexer

DC Characteristics

V_{EE}=-4.5V±0.3V, V_{CC}=V_{CCA}=GND,V_{TT}=-2V, T_C=0°C to +85°C, R_T=50Ω to V_{TT}

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}	185	305	430	mA

AC Characteristics

V_{EE}=-4.5V ±0.3V, V_{CC}=V_{CCA}=GND, V_{TT}=-2V,T_C=0°C to +85°C, R_T=50Ω to V_{TT}

Characteristics	Symbol	Input	output	Test condition	Min.	Typ.	Max.	Unit
Propagation delay time	t_{pd}	C	Qn	Fig.1 ②		1300	1730	ps
			Cout	Fig.1 ①		1000	1330	
Set up time	t_s	D,C	Qn	R=Low		70		
Hold time	t_h			R=Low		270		
Release time	t_R	R,C				50		
Minimum pulse width	t_{pw}	R			385	300		
Rise time	t_r	C		20 to 80%		165	220	
			Cout			165	220	
Fall time	t_f		Qn			165	220	
			Cout			165	220	
Maximum operating frequency	f_{max}	D,C	Qn		2.6	3.0		GHz

Timing Chart