CHIP-CEIVER™ - Single Chip FM Transceiver

100 - 1000 MHz

NT2904

FEATURES

- **Direct-Conversion, Zero-IF, Architecture**
- **Full or Half-Duplex Operation**
- **Suitable for FM/FSK Modulation**
- **Dual, On-Chip PLL Synthesizers/VCOs**
- **3-wire serial interface**
- **2.7 - 3.3V Operation / Standby Mode**
- **No Tune "Tankless" Detector**
- **RF Output +3.0 dBm**
- **Low Cost, Thin-Quad Flat Package, (TQFP-48)**

APPLICATIONS

Analog/Digital "900 MHz" Cordless Phones
AMR/Telemetry/Data Radios
Wireless Security Products
ISM Band (868, 915 MHz) Wireless Voice/Data Products

GENERAL DESCRIPTION

The NT2904 **CHIP-CEIVER**™ is a complete, single-chip, FM/FSK transceiver solution, which will operate in any 26 MHz band from 100-1000 MHz, including the Industrial Scientific Medical (ISM) band (902-928 MHz). Utilizing a unique direct-conversion, zero-intermediate frequency (zero-IF) receiver architecture, the NT2904 **CHIP-CEIVER**™ provides radio designers with a "simple" RF path design solution. The device is fabricated as a single, monolithic, BiCMOS, integrated circuit.

The receiver section of the NT2904 provides all of the required RF synthesis, down-conversion, filtering, automatic gain control (AGC), automatic frequency control (AFC), and demodulator functions. The transmitter section contains a directly modulated VCO and RF power amplifier (PA). Internal, dual, high-performance phase locked loop (PLL) synthesizers/VCOs allow full-duplex Tx/Rx operation over the entire RF tuning range. Tuning, power management, and gain control (manual) functions are accomplished via a standard 3-wire serial interface.

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PRODUCT DESCRIPTION

The BiCMOS construction of the NT2904 **CHIP-CEIVER**™ provides a high level of integration, with high performance operation and low power consumption. The CHIP-CEIVER™ operates over an industrial temperature range of -20°C to +65°C and over the supply voltage of +2.7 V to +3.3 V. The device is available in an industry standard plastic package as a thin-quad flat package (TQFP).

FUNCTIONAL DESCRIPTION

A functional block diagram of the NT2904 **CHIP-CEIVER**™ is shown in Fig.(1). The receive section of the device consists of several major function blocks, including a switchable RF input attenuator, quadrature mixer (down-conversion), differential to single-ended, variable gain amplifiers (VGAs), PLL synthesizer / voltage controlled oscillator (VCO), I/Q low-pass filters, variable gain amplifiers (VGAs), DC offset correction circuitry, quadrature mixer (up-conversion), zero-crossing detector, Period-to-Digital converter (P/D), Linearization ROM, and a Digital-to-Analog converter (DAC). Additionally, the device contains a reference crystal oscillator / automatic frequency control (AFC) circuitry and associated reference frequency synthesiser. The transmit section of the device consists of a PLL synthesizer / directly modulated voltage controlled oscillator (VCO), and a RF power amplifier (PA).

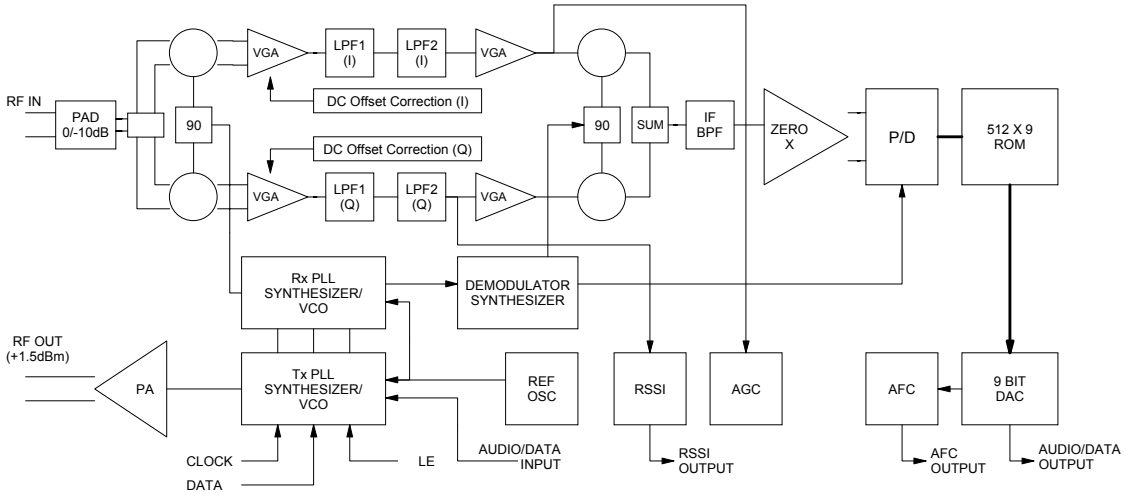


Figure (1), NT2904 **CHIP-CEIVER**™ - Functional Block Diagram

The receiver section of the NT2904 **CHIP-CEIVER**™ utilizes a quadrature mixer in a direct-conversion, zero-intermediate frequency (zero-IF) approach. After quadrature down-conversion and baseband filtering, a quadrature mixer up-converts the complex baseband signal to an intermediate frequency (IF) for demodulation. Direct conversion to zero-IF has several advantages over super-heterodyne approaches. First, the image frequency is eliminated because the IF is zero. Second, the use of active, low pass, filters provide a high level of integration, while eliminating the need for external IF filters and IF transformers.

FUNCTIONAL DESCRIPTION - Cont.

The transmitter section of the NT2904 **CHIP-CEIVER**™ is comprised of a modulation input circuit, a PLL synthesizer / VCO, and a RF power amplifier (PA) capable of providing +3.0 dBm into a 50Ω load.

A description of each major function block follows:

RF Input Attenuator Pad – A switchable 0/-10dB attenuator pad allows high signal level capability at the RF Input of the receiver. This pad is located prior to the quadrature mixer (down-conversion) and can be either manually controlled via the 3-wire interface, or automatically controlled via the AGC section of the device.

Quadrature Mixer (down-conversion) - The quadrature mixer is a critical part of the **CHIP-CEIVER**™ zero intermediate-frequency (zero-IF) design. The main advantage of the quadrature mixer is its ability to translate the RF frequency directly to a zero-IF, thereby eliminating the image frequency. Consequently, the image filter between the external LNA and the RF input to the **CHIP-CEIVER**™ can be eliminated in most designs. The design requirements for the duplexer and RF bandpass filter may also be relaxed. In addition, the quadrature mixer achieves a lower overall noise figure by virtue of image frequency elimination. The balanced mixers in the quadrature mixer are designed to closely track each other in both amplitude and phase response. Additionally, the quadrature LO signal is generated by direct division of the receiver LO, thereby eliminating external phase shifting networks. Furthermore, for improved noise immunity all internal RF signal paths are fully differential, thereby providing common mode noise rejection. The gain of the mixer can be adjusted via the 3-wire interface (see RF Mixer Attenuation).

Crystal Oscillator and Reference Synthesizer - The crystal oscillator circuit can be trimmed externally and, with the addition of an external varactor, an Automatic Frequency Control function can be implimented by using the AFC output pin (46). (see AFC in the application section)

The reference synthesizer is comprised of an 13 bit counter which provides the PLL reference frequency for both the receiver and transmitter synthesizers. The crystal oscillator circuit normally provides the input to the reference synthesizer, however, external frequency source can be used as a reference for the synthesizer. All 13 bits of the synthesizer are fully programmable, to allow a large degree of flexibility in the choice of either the reference crystal or external reference frequency.

PLL Synthesizer (Receive) - The receive (Rx) on-chip PLL synthesizer with voltage controlled oscillator (VCO), is designed to provide a low phase noise, local oscillator. The RxVCO operates in a balanced mode at 2X the Rx local oscillator frequency. The VCO frequency is immediately divided by a factor of 2, to provide the in-phase and quadrature L.O. for the down-conversion RF mixer. This signal also drives the receive

FUNCTIONAL DESCRIPTION - Cont.

synthesizer and demodulator synthesizer. The synthesizer is 17 bits in total (excluding the proceeding divide by 2). These 17 bits are split into 14 bits to provide the input to the PLL phase detector to be compared with the reference frequency, with an additional 3 bits providing fractional-n capability, to allow channel frequency definition of ½, ¼ and 1/8 of the PLL reference frequency.

The Rx VCO center frequency is determined by an external tank circuit comprised of an external, center-tapped, inductor. The tank circuit is connected to RVCO (41) and /RVCO (42) respectively. An external PLL loop filter network, connected to the RPLL pin (39), filters the VCO control voltage. This control voltage (K_{VCO} 52 MHz/V @ 1.8GHz) is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair. The receive frequency for the **CHIP-CEIVER**™ is programmed via a 3-wire compatible, serial interface (Data, Clock, and Load Enable).

Demodulator Synthesizer – This sythesizer consisits of programmable and fixed dividers which determine the IF frequency and the demodulator clock frequency for the digital demodulator. (refer to Fig 2). This feature enables the demodulator bandwidth to be programmed between 0.08% and 0.0018% of the receiver local oscillator frequency (up to a maximum of 150kHz). The demodulator synthesiser is controlled by 3-bits of the reference frequency register.

Variable Gain Amplifiers - The gain of the receiver can be dynamically adjusted via the 3-wire interface to maintain signal linearity before the demodulator. This enables the achievement of high values of SINAD for an analog FM link. An Automatic Gain Control (AGC) function is also available on-chip. The gain can be manually adjusted in 3 locations by the following:

1. A 10dB RF pad before the Quadrature mixer (PAD in figure 1)
2. Four step baseband attentuators in the RF quadrature I and Q mixer load circuits giving nominal voltage conversion gains of 18, 8, -2, -13dB for each channel.
3. Three step baseband Variable Gain Amplifiers after the baseband I and Q low pass filters giving voltage gains of 40, 30, 20 and 10 dB.

In addition, each VGA provides differential to single-ended conversion and amplification of the baseband signal, prior to the I/Q low-pass filters. These gain stages are referenced to pre-filter ground (PFGND), an internally generated virtual ground.

LPF1 (I/Q) – This first stage of the I/Q baseband low pass filter (LPF) section consists of active, Sallen-key type filters. These filters provide a combination of low noise figure and gain along with a wide dynamic input range. The purpose of these filters is to provide preliminary rejection of the out-of-band interfereres. The reduction of out-of-band interferer levels, reduce the dynamic range requirements for the following filter stages in LPF2. The –3dB corner frequency of these LPFs are set via external RC values.

FUNCTIONAL DESCRIPTION - Cont.

LPF2 (I/Q) – This second stage of the I/Q baseband low pass filter (LPF) section consists of active, transconductance (gm) type filters. Combined with LPF1, these filters provide the required channel selectivity by passing the entire desired frequency spectrum, while attenuating noise and adjacent channel interference (ACI), outside of the desired signal's bandwidth.

DC Offset Correction – A proprietary DC offset correction circuit is used in the NT2904 to control DC offset voltages. The use of DC offset correction improves dynamic range, minmises LO feed-through (Up-convesion mixer), and reduces signal distortion. The correction circuit operates automatically and in a continuous mode.

Quadrature Mixer (up-conversion) - The quadrature up-conversion mixer forms yet another important part of the overall **CHIP-CEIVER**™ design. This quadrature mixer translates the filtered baseband signal from one frequency to another i.e. the zero-IF, complex, baseband spectrum is translated by the quadrature up-conversion mixer to a frequency centered about the up-conversion LO mixer frequency. The resultant up-converted IF signal is low enough in frequency to provide adequate SNR at the output of the period-to-digital converter (P/D), yet high enough to satisfy signal sampling criterion.

IF BPF - The intermediate frequency (IF), bandpass filter (BPF) after the quadrature up-conversion mixer passes the lowest frequency signal components and rejects the even / odd harmonic components of the up-conversion mixer's local oscillator (LO). The IF bandpass filter is comprised of cascaded, active, transconductance filters with Butterworth response characteristics.

RSSI - The receive signal strength indication (RSSI) measurement circuitry incorporates a log amplifier and detector for the purpose of measuring the received RF carrier power level. The output is a DC voltage, which is linear over a 65 dB dynamic range. The RSSI measurement range is from -100dBm to -35dBm, with the RF input pad bypassed (0dB) and the quadrature mixer gain stage set to high. This range is extended as the receiver gain is reduced. The RSSI conversion factor is ≅ (-30mV/dB), with a voltage range of 2.0 Vdc.

AFC – Automatic Frequency Control of the receive local oscillator (LO) frequency is used to improve receiver performance. Without AFC, frequency offsets cause a reduction in SINAD due to filter distortion. A reduction in SINAD of 4-5dB is typical at a frequency offset of ±20kHz. Additionally, due to the zero-IF architecture of the NT2904 AFC is used to reduce beat note levels.

The AFC correction signal, which is generated internally in the NT2904 is available as a DC current at the AFC (46) output pin. A series RC network connected from AFC pin (46) to VSS, along with decoupling capacitors connected to AFCC pin (47) from VDD and VSS respectively, determine the attack time of the AFC integration (double) loop.

FUNCTIONAL DESCRIPTION - Cont.

Zero Crossing Detector - A high speed BiCMOS comparator performs the basic function of a "Limiter" and is used to detect the intermediate frequency (IF) zero-crossing events. Each "half-cycle" interval of the IF is output from the comparator as a pulse, which is subsequently measured by the Period-to-Digital (P/D) converter. Complimentary outputs from the comparator provide alternating "half-cycle" gating signals to the P/D converter.

Period-to-Digital (P/D) Converter - The digitizer used in the **CHIP-CEIVER**™ employs the NUMA Technologies' Period-to-Digital (P/D) converter as the digitizer. The basic principal of the P/D relies on it's ability to integrate and dump sequential half-cycle intervals of the IF signal with high resolution. The numerical output from the P/D is the form of 1/f or period of the intermediate frequency (IF) signal.

The clock signal for the P/D (Fpd) is derived from the RxVCO oscillator. The P/D clock frequency is function of a programmable divide ratio.(PDR) As an example, a functional block diagram of the P/D clock generation is shown in Fig. (2), for a PDR divide ratio of 12. (Refer to the "Demodulator" section under "Bandwidth Adjustment" in the application notes for further information)

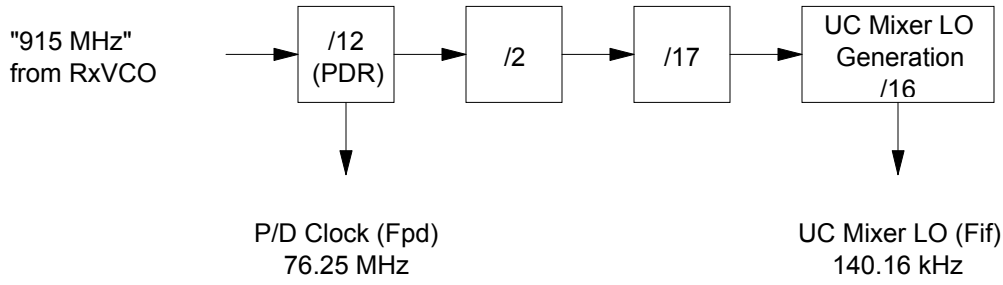


Figure (2), P/D Converter Clock Generation - Functional Block Diagram

Linearization ROM – The information from the period-to-digital converter (P/D) is in the form of a period measurement (1/f) of each half cycle of the IF signal. Each data value from the P/D is used to address a pre-programmed value in the linearization ROM. In this manner, the linearization ROM is used as a look-up table which provides the required 1/p conversion to convert the period information of the P/D to frequency, in a linear fashion. The ROM maybe programmed with different numerical values, thereby providing different detector response characteristics, for use in either analog or digital modulation schemes.

D/A Converter - The Digital-to-Analog (DAC) converter along with the output from the P/D converter form a "tankless discriminator". A digital-to-analog converter (DAC) provides a special transfer function, which is required to linearize the digital data "period" value from the P/D converter. The resultant analog signal is the recovered audio (demodulated FM).

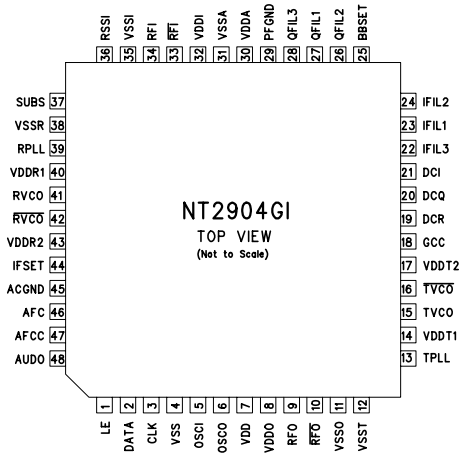
FUNCTIONAL DESCRIPTION - Cont.

PLL Synthesizer (Transmit) - The transmit (Tx) on-chip PLL synthesizer is identical to the receive PLL synthesiser except that it does not contain the fixed divide by 2 directly after the VCO. The transmit VCO frequency is therefore identical with the transmitter local oscillator. The transmit PLL accepts modulation audio to provide a frequency modulated (FM) RF carrier. Utilizing a direct modulation approach, the modulation voltage is directly applied to the PLL loop filter. The VCO center frequency is determined by an external tank circuit comprised of two inductors connected to the TVCO (15) and /TVCO (16). An external PLL loop filter network, connected to the TPLL pin (13), filters the VCO control voltage. This control voltage (K_{VCO} 26 MHz/V for 900MHz Tx LO) is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair. The transmit frequency for the **CHIP-CEIVER**™ is programmed via a three (3) wire compatible, serial interface (Data, Clock, and Load Enable).

PA - The on-chip RF power amplifier is a differential gain stage capable of RF output power levels of up to +3.0 dBm. In most cases an external PA is not required, however, in the event additional RF output power is required the internal PA can play the role of a pre-driver. For additional information regarding the internal PA refer to the pin descriptions of RFO and /RFO.

PIN CONFIGURATION

Plastic Thin Quad Flat Package (TQFP-48 pin)



PIN DESCRIPTIONS

This section summarizes the pin descriptions of the NT2904 **CHIP-CEIVER**™ by pin name.

Pin Name	Pin Number	Description
LE	(1)	Load Enable: This CMOS compatible input when HIGH allows data to be shifted into the internal shift register.
DATA	(2)	Serial Data Input: This CMOS compatible input accepts data MSB first. Refer to page 17, for additional information on the programming format.
CLK	(3)	Serial Clock: This CMOS compatible input shifts serial data into the internal 23-bit serial shift register, upon the rising edge of the clock signal.
VSS	(4)	Digital ground: This is the ground pin for the internal CMOS digital circuitry, CMOS sections of the Tx/Rx synthezier dividers, Tx/Rx PLL charge pumps, crystal oscillator, AFC, period-to-digital (P/D) converter, ROM, and Digital-to-Analog converter (DAC).
OSCI	(5)	Oscillator Input: This CMOS input is the reference frequency input for both the Tx and Rx PLLs. When used with an external reference oscillator, the signal level should be within the range of 200-400mV peak. Additionally, this input can be used with the OSCO pin to form a Colpitts crystal oscillator.

PIN DESCRIPTIONS - Cont.

OSCO	(6)	Oscillator Output: This output is used in conjunction with OSCIN to form a Colpitts oscillator using an external, low cost, crystal (parallel-resonant).
VDD	(7)	Digital power supply: This is the power supply pin for the internal CMOS digital circuitry, CMOS sections of the Tx/Rx synthezier dividers, Tx/Rx PLL charge pumps, crystal oscillator, AFC, period-to-digital (P/D) converter, ROM, and Digital-to-Analog converter (DAC). This pin should be de-coupled to VSS (as close to the pin as possible), with a pair of high quality ceramic capacitors (1nF ‖ 100nF)
VDDO	(8)	RF output power supply: This is the power supply pin for the internal power amplifier (PA) and transmit VCO prescaler. This pin should be de-coupled to VSSO (as close to the pin as possible), with a high quality ceramic 100pF capacitor.
RFO, /RFO	(9, 10)	RF Amplifier Outputs: The RF output of the NT2904 consists of a differential current source. The differential output impedance of the power amplifier (PA) is ≈700Ω ‖ 1.2 pF (915MHz). An RF transformer (Mini-Circuits JTX-4-10T) can be used to convert the differential signal to a single-ended 50Ω load. See figure (3) in the applications section. Discrete components can also be used to provide the required phase split, as well as impedance matching.
VSSO	(11)	RF output ground: This is the ground pin for the internal power amplifier (PA) and transmit TxVCO prescaler.
VSST	(12)	Transmit VCO ground: This is the ground pin for the internal transmit voltage controlled oscillator. This pin provides the de-coupling point for VDDT.
TPLL	(13)	Transmit Voltage Controlled Oscillator: This pin connects to an external PLL loop filter. This filtered tuning voltage provides the tuning voltage for the internal varactor tuning diodes. The PLL loop dynamics are controlled by the loop filter component values. Transmitter modulation is accomplished by directly applying the modulating signal (Audio/Data) to the PLL loop, via an external coupling network.

PIN DESCRIPTIONS - Cont.

VDDT1 **VDDT2**	(14,17)	Transmit power supply: These are the power supply pins for the internal transmit voltage controlled oscillator (VCO) and transmit PLL charge pump. These pins should be de-coupled to VSST, as close to each pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.
TVCO **/TVCO**	(15,16)	Transmit VCO Tank: These single-end outputs drive external balanced inductors, which form the VCO resonant tank circuit. This tank circuit establishes the overall oscillation frequency of the TxVCO. Careful layout is required to prevent RF leakage to the RxVCO tank circuit, and the associated receive input circuitry. (See applications section for recommend values)
GCC	(18)	Gain Control Capacitor: This pin connects to an external 100 nF capacitor connected to VDDA, which provides de-coupling for the internal gain control circuitry.
DCR	(19)	DC Offset RSSI: This pin is connected to an external 330 nF capacitor connected to VDDA, which removes residual DC offset from the RSSI measurement circuitry.
DCQ	(20)	DC Offset (Q): This pin is connected to an external 330 nF capacitor connected to ACGND, which removes residual DC offset from the baseband signal Q(t).
DCI	(21)	DC Offset (I): This pin is connected to an external 330 nF capacitor connected to ACGND, which removes residual DC offset from the baseband signal I(t).
IFIL1,2,3	(23, 24, 22)	Baseband In-phase (I) Filter: These pins connect to an external RC network referenced to PFGND, which set the corner frequency of the first baseband (I), Sallen-key, filter stage. (See “Bandwidth Adjustment” for component tolerances).
BBSET	(25)	Baseband Filter Set: This pin connects to an external resistor connected to VDDA, which sets the corner frequency of the transconductance (gm) baseband (I/Q) filter stages. (See applications section for recommended values)

PIN DESCRIPTIONS - Cont.

QFIL1,2,3	(27, 26, 28)	Baseband Quadrature (Q) Filter: These pins connect to an external RC network referenced to PFGND, which set the corner frequency of the first baseband (Q), Sallen-key, filter stage. (See "Bandwidth Adjustment" for component tolerances).
PFGND	(29)	Pre-Filter Ground: This pin connects to an external 100 nF capacitor connected to VDDA, which provides de-coupling for the internal pre-filter buffer ground nodes.
VDDA	(30)	Baseband and IF Filter power supply: This is the power supply pin for the I/Q filters, amplifiers, RSSI, up-conversion mixer, and IF filter. This pin should be de-coupled to VSSA, as close to the pin as possible, with a high quality .1µF and 1nF ceramic capacitors.
VSSA	(31)	Baseband and IF Filter ground: This is the ground pin for the I/Q filters, amplifiers, RSSI, up-conversion mixer, and IF filter.
VDDI	(32)	RF Input power supply: This is the power supply pin for the internal RF Quadrature mixer. This pin should be de-coupled to VSSI, as close to the pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.
/RFI **RFI**	(33, 34)	RF Input: This is the small signal RF differential inputs to the NT2904. The differential input impedance is 60Ω ‖ 0.9pF @ 915MHz. An RF transformer (Mini-Circuits JTX-2-10T) can be used to convert the differential signal to a single-ended 50Ω load. See figure (3) in the applications section. Discrete components can also be used to provide the required phase split, as well as impedance matching.
VSSI	(35)	RF Input ground: This is the ground pin for the internal RF Quadrature mixer. This pin should be connected to an RF ground plane using through-hole vias.

PIN DESCRIPTIONS - Cont.

RSSI	(36)	Receive Signal Strength Indicator: This output pin provides a current output, into an external shunt resistor and capacitor (48kΩ || 10nF) connected to VSS, to develop a filtered voltage level, proportional to the receive RF signal strength. The output is linear over a 65 dB range with an output swing of 0.1 to 2.1 Vdc. The active range of the RSSI is from low signal strength, i.e. –100dBm to –35dBm (GC_{HIGH}).
SUBS	(37)	Substrate: This pin is connected to the silicon substrate and should be connected to a "clean" ground plane.
VSSR	(38)	Receive VCO ground: This is the ground pin for the internal receive voltage controlled oscillator. This pin provides the de-coupling point for VDDT.
RPLL	(39)	Receive Voltage Controlled Oscillator: This pin connects to an external PLL loop filter. This filtered tuning voltage provides the tuning voltage for the internal varactor tuning diodes. The PLL loop dynamics are controlled by the loop filter component values.
VDDR1 **VDDR2**	(40,43)	Receive VCO power supply: These are the power supply pins for the internal receive voltage controlled oscillator and receive PLL charge pump. These pins should be de-coupled to ground, as close to each pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.
RVCO **/RVCO**	(41,42)	Receive VCO Tank: These single-end outputs drive external balanced inductors, which form the RxVCO resonant tank circuit. This tank circuit establishes the overall oscillation frequency for the RxVCO. (See applications section for recommended values) The RxVCO tank frequency is 2X the desired Rx LO frequency, since the on-chip quadrature generation circuitry divides this LO signal by 2. The **CHIP-CEIVER**™ is a direct conversion, Zero-IF receiver, therefore the quadrature LO frequency is the same as the receive frequency, (i.e. no IF offsets). Careful layout is required to prevent RF leakage to the TxVCO tank circuit and associated transmit circuitry.

PIN DESCRIPTIONS - Cont.

IFSET	(44)	IF Filter: This pin connects to an external resistor referenced to VDDA, which sets the corner frequencies of the IF transconductance (gm) filter stages. (See applications section for recommended values)
ACGND	(45)	AC Ground: This pin connects to an external 100 nF capacitor connected to VSSA, which provides de-coupling for the internal baseband and IF filter ground nodes.
AFC	(46)	Automatic Frequency Control: This output pin connects to an external filter, which provides the DC control voltage for the automatic frequency control (AFC) circuitry. The component values of the filter establish the AFC loop delay or “attack time”. (See applications section for recommended component values)
AFCC	(47)	Automatic Frequency Control Capacitor: This pin connects to a pair of external 150 nF de-coupling capacitors connected to VDD and VSS respectively, which provide filtering for an internal reference voltage.
AUDO	(48)	Audio Output: In the Analog mode, this output pin provides the recovered, demodulated audio signal. The audio signal level is 175 mVrms. (typ). In the Digital mode, this CMOS compatible output provides serial data from the internal data slicer.

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS: (Overall)					
Power Supply Voltage	Vdd	2.7	3	3.3	Vdc
Operating Temperature	Topr	-20		65	C
Frequency of Operation[1]	Fopr	100		1000	MHz
Reference Frequency[2]	Fref	5		20	MHz
Supply Current (Receive Only)	Iddr		34		mA
Supply Current (Transmit Only)	Iddt		20		mA
Supply Current, Total (Rx + Tx)	Idd	50	54	60	mA
Standby Current	Istb			5	µA
GENERAL SPECIFICATIONS: (Receiver Section)					
Input Sensitivity (12dB SINAD)[4]	$Pmin_A$	-102	-104	-106	dBm
Input Sensitivity (10^{-3} BER)[5]	$Pmin_D$	-91	-94	-97	dBm
Noise Figure	NF				dB
Input IP3[6]	IIP[3]		-1		dBm
Receiver Channel Bandwidth (-3dB)[3]	Rbw	16		150	kHz
RSSI Voltage Range (-100 to -35dBm)[6]	RSSI	0.1		2.1	Vdc
RSSI Conversion Factor (Log)		-27	-32	-37	mV/dB
Audio Response - HP Cutoff (-3dB)	Fhp			0.15	kHz
Audio Response - LP Cutoff (-3dB)	Flp	50			kHz
Channel Spacing	Csp	6.25			kHz
Channel Step Size	Css	6.25			kHz
GENERAL SPECIFICATIONS: (Transmitter Section)					
Transmitter Output Power[7]	Po	0	3	5	dBm
Harmonic Level (2nd)[8]			-50		dBc
Harmonic Level (3rd)[8]			-40		dBc
Harmonic Level (4th)[8]			-70		dBc
Channel Spacing	Csp	6.25			kHz
Channel Step Size	Css	6.25			kHz

[1]Frequency of operation for both Rx and Tx is determined by external VCO tank circuit inductors.
[2]The PLL reference can be either an external signal or supplied by the on-chip oscillator in conjunction with an external crystal.
[3]Some restrictions on the combination of receiver bandwidth and receive frequency band. (see user notes).
[4]CCITT receive audio filter. Sensitivity increases slightly with decreasing receiver channel bandwidth (*not* inversely proportional), see user notes; figure given is for a 140kHz bandwidth.
[5]56.7kbps 511 PRBS, FSK modulation, 80kHz low pass receive filter. Sensitivity increases slightly with decreasing receiver channel bandwidth (*not* inversely proportional), see user notes; figure given is for a 140kHz bandwidth.
[6]For maximum receiver gain (increases as the receiver gain is reduced).
[7]Transmitter output power can be varied via an external bias resistor.
[8]Transmitter harmonic levels are for applications board using Mini-Circuits baluns.

PERFORMANCE SPECIFICATIONS

NT2904 Evaluation Board (NUMA drawing # 4001101)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYSTEM:					
Tx-Rx Frequency Band			902.0 to 928.0		MHz
Tx-Rx Duplex Split			22.75		MHz
Channel Spacing			300		kHz
Channel Step Size			50		kHz
PLL Reference Frequency (External)			12		MHz
Audio Response - HP Cutoff (-3dB)	Fhp			0.15	kHz
Audio Response - LP Cutoff (-3dB)	Flp	50			kHz
RECEIVER OPERATION:					
Input Sensitivity (12dB SINAD)[1]	$Pmin_A$	-101	-104	-107	dBm
Input Sensitivity (10^{-3} BER)[2]	$Pmin_D$	-91	-94	-97	dBm
SINAD (-85dBm)[1]	SINAD	40	48		dB
Maximum RF Input (12dB SINAD)[1]			-5		dBm
Noise Figure	NF				dB
Input IP3[3]	IIP3	-3	-1		dBm
Input 1dB Compression Point[3]	ICP	-20	-18		dBm
Receive Channel Bandwidth	Rbw	125	140	160	kHz
Adjacent Channel Rejection	ACI	55	60	65	dB
Tx Carrier Rejection		65	70		dB
RxLO Spurious Level (@RFIN, /RFIN)				-80	dBc
RxLO Spurious Level (2nd Harmonic)				-55	dBc
Audio Output Level[4]		150	175	200	mVrms
Output Impedance (AUDO, Pin 48)		2		10	kohm
AFC Correction Range			22		kHz
AFC Center Frequency Tolerance			0.5	2	kHz
RSSI Voltage Range (-100 to -35dBm)[3]	RSSI	0.1		2.1	Vdc
RSSI Conversion Factor (Log)		-27	-32	-37	mV/dB
RSSI Detection Range (Min-Max)	RSSI	-100		-35	dBm
PLL Charge Pump Current (Hi)		0.7	1	1.3	mA
LO Gain		18	27	36	MHz/v
LO Phase Noise (10kHz Offset)			-87		dBc/Hz
LO Phase Noise (10MHz Offset)			-143		dBc/Hz

[1]CCITT receive audio filter (external).
[2]56.7kbps 511 PRBS, FSK modulation, 80kHz low pass receive filter. Sensitivity increases slightly with decreasing receiver channel bandwidth (*not* inversely proportional), see user notes; figure given is for a 140kHz bandwidth.
[3]For maximum receiver gain (increases as receiver gain is reduced).
[4]RF input 1kHz modulation, ±25kHz peak FM deviation.

PERFORMANCE SPECIFICATIONS – Cont.

NT2904 Evaluation Board (NUMA drawing # 4001101)

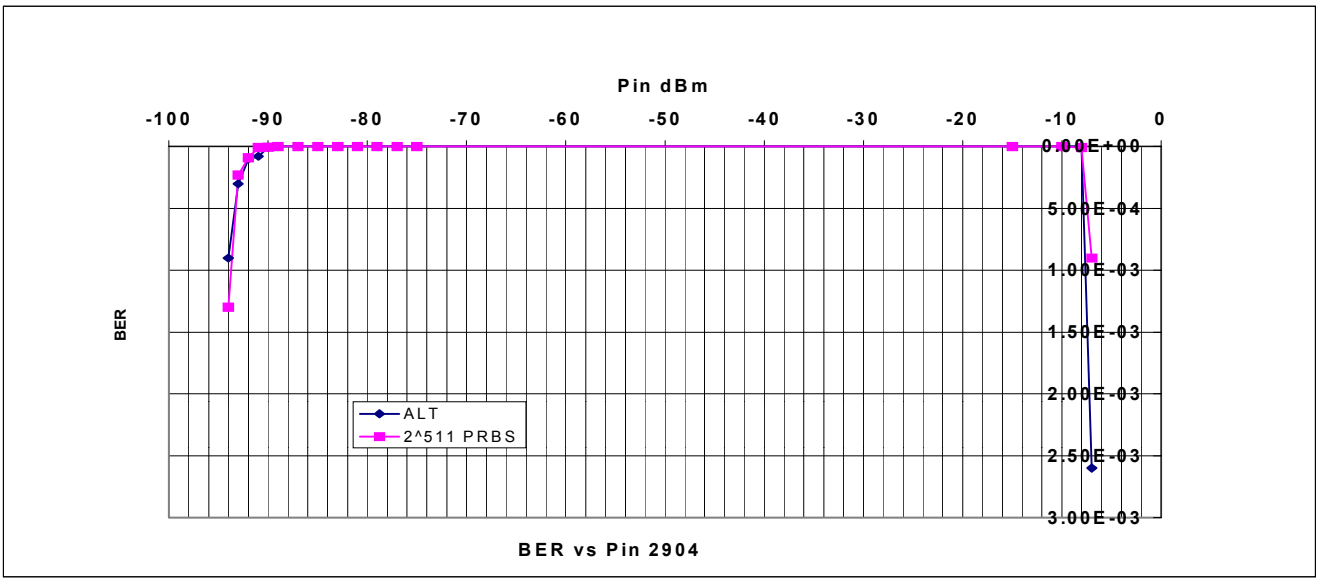
TRANSMITTER OPERATION:					
Power Output		0	1.5	3	dBm
Harmonic Level (2nd) @ 915MHz			-50	-40	dBc
Harmonic Level (3rd)			-40	-29	dBc
Harmonic Level (4th)			-70	-60	dBc
Intermodulation Prod. (2*RxLO-TxLO)			-58		dBc
Intermodulation Prod. (Other)				-60	dBc
LO Phase Noise (10kHz Offset)			-87	-82	dBc/Hz
LO Phase Noise (10MHz Offset)			-150		dBc/Hz
LO Gain		18	26	36	MHz/v
PLL Charge Pump Current (Low)		0.14	0.2	0.26	mA
Audio Input Level[5]			175		mVrms
Audio Input Impedance		1		2	kohm

[5]On board potentiometer (R33) is used to set FM deviation at ±25kHz peak for 1kHz modulation

Digital Receiver, Test Measurements (BER)

Test Conditions (NT2904 Evaluation Board):

FM Deviation: 20kHz (RMS) / 28kHz (Pk)
Data Rate: 56.7kbps
Data: 511 (prbs)
Mode: Digital
AGC: On
AFC: On
Transmitter: On (CW)

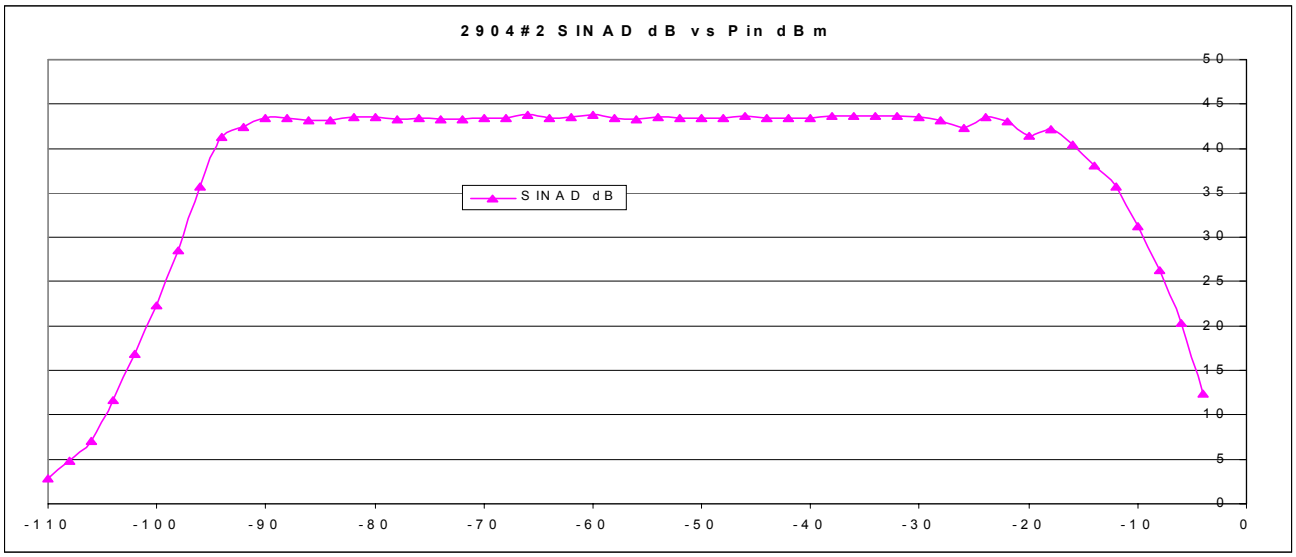


PERFORMANCE SPECIFICATIONS – Cont.

Analog Receiver, Test Measurements (SINAD)

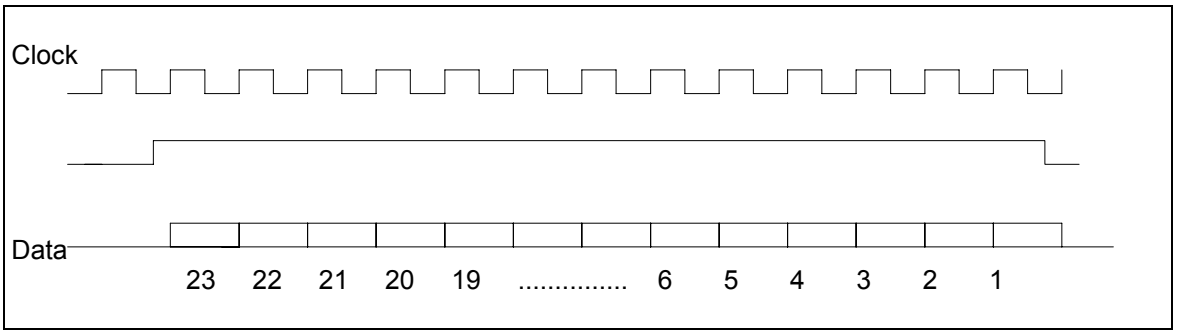
Test Conditions (NT2904 Evaluation Board):

Rx Frequency:	915MHz
FM Deviation:	25kHz (RMS) / 35kHz (Pk)
Modulation Tone:	1kHz
Audio Filter:	CCITT C-Message
Mode:	Analog
AGC:	On
AFC:	On
Transmitter:	On (CW)



Tx/Rx PLL PROGRAMMING and SERIAL INTERFACE

The Tx/Rx frequencies, reference oscillator frequency selection, along with the operational and test modes of the NT2904, are controlled by a standard 3-wire bus comprised of Clock, Load Enable, and Data inputs. The programming word contains 16, 22, or 23 bits, the first two bits select the programming of the receive VCO frequency, the transmit VCO frequency, the reference frequency or the device operational modes. The remaining bits contain the data to be programmed. The timing diagram below, shows the relationship between Data, Clock, and Load Enable.



Data is clocked into the internal shift registers on the positive edge of the CLOCK (3) pin, while Load Enable (1) pin is held HIGH. Data is loaded from the shift registers into the data registers on the negative edge of the Load Enable (LE). This load is NOT synchronized with the programmable divider, i.e. the load is controlled directly by the negative falling edge of the Load Enable.

Data Register Programming

REFERENCE Frequency Select

Bit 1 (last bit loaded)		Load control bit 1 = (0)
Bit 2		Load control bit 2 = (0)
Bit 3	Ref(1) LSB	Reference divide register (count 1 to 2048)
Bit 4	Ref(2)	Reference divide register (count 1 to 2048)
Bit 5	Ref(3)	Reference divide register (count 1 to 2048)
Bit 6	Ref(4)	Reference divide register (count 1 to 2048)
Bit 7	Ref(5)	Reference divide register (count 1 to 2048)
Bit 8	Ref(6)	Reference divide register (count 1 to 2048)
Bit 9	Ref(7)	Reference divide register (count 1 to 2048)
Bit 10	Ref(8)	Reference divide register (count 1 to 2048)
Bit 11	Ref(9)	Reference divide register (count 1 to 2048)
Bit 12	Ref(10)	Reference divide register (count 1 to 2048)
Bit 13	Ref(11) MSB	Reference divide register (count 1 to 2048)
Bit 14	PDR(1)	P/D Converter reference clock frequency select
Bit 15	PDR(2)	P/D Converter reference clock frequency select
Bit 16	PDR(3)	P/D Converter reference clock frequency select

PDR (3)	PDR (2)	PDR (1)	Divide ratio, PDR
0	0	0	2
0	0	1	6
0	1	0	12
0	1	1	24
1	0	0	36
1	0	1	48
1	1	0	72
1	1	1	96

Internal Reference Frequency = (Reference Oscillator Frequency) / Ref(11:1)

e.g. 12MHz crystal, REF ratio 240, gives 50kHz internal reference frequency

Demodulator bandwidth, BWdm = (Receiver LO)/(580*PDR)

e.g. 915MHz frequency, PDR of 12, gives 131kHz demodulator bandwidth

Programming word = 010 00011110000 00

Data Register Programming - Cont.

<u>RECEIVE</u> VCO Frequency Select

Bit 1 (last bit loaded)		Load control bit 1 = (1)			
Bit 2		Load control bit 2 = (0)			
Bit 3	LSB	VCO frequency	F	Rf(1)	F register
Bit 4		VCO frequency	F	Rf(2)	F register
Bit 5	MSB	VCO frequency	F	Rf(3)	F register
Bit 6	LSB	VCO frequency	A	Ra(1)	A register
Bit 7		VCO frequency	A	Ra(2)	A register
Bit 8		VCO frequency	A	Ra(3)	A register
Bit 9		VCO frequency	A	Ra(4)	A register
Bit 10	MSB	VCO frequency	A	Ra(5)	A register
Bit 11	LSB	VCO frequency	M	Rm(1)	M register
Bit 12		VCO frequency	M	Rm(2)	M register
Bit 13		VCO frequency	M	Rm(3)	M register
Bit 14		VCO frequency	M	Rm(4)	M register
Bit 15		VCO frequency	M	Rm(5)	M register
Bit 16		VCO frequency	M	Rm(6)	M register
Bit 17		VCO frequency	M	Rm(7)	M register
Bit 18		VCO frequency	M	Rm(8)	M register
Bit 19		VCO frequency	M	Rm(9)	M register
Bit 20	MSB	VCO frequency	M	Rm(10)	M register
Bit 21		Rx VCO Trim bit 1			
Bit 22		Rx VCO Trim bit 2			
Bit 23		Not Used			

Rx VCO Trim Bits		**Trim Number**
2	**1**	
0	0	0 – minimum C
0	1	1
1	0	2
1	1	3 – maximum C

RxVCO Frequency = Internal Reference Frequency x ((32 x M) + A + (F/8))
Note: A>M

e.g. 903.50625MHz RF, 50kHz reference frequency; div ratio 18070.125, trim 2

Programming word = X10 1000110100 10110 001 01

PLL Data Register Contents - Cont.

<u>TRANSMIT</u> VCO Frequency Select

Bit 1 (last bit loaded) Load control bit 1 = (0)
Bit 2 Load control bit 2 = (1)

Bit 3	LSB	VCO frequency	F	Tf(1)	F register
Bit 4		VCO frequency	F	Tf(2)	F register
Bit 5	MSB	VCO frequency	F	Tf(3)	F register
Bit 6	LSB	VCO frequency	A	Ta(1)	A register
Bit 7		VCO frequency	A	Ta(2)	A register
Bit 8		VCO frequency	A	Ta(3)	A register
Bit 9		VCO frequency	A	Ta(4)	A register
Bit 10	MSB	VCO frequency	A	Ta(5)	A register
Bit 11	LSB	VCO frequency	M	Tm(1)	M register
Bit 12		VCO frequency	M	Tm(2)	M register
Bit 13		VCO frequency	M	Tm(3)	M register
Bit 14		VCO frequency	M	Tm(4)	M register
Bit 15		VCO frequency	M	Tm(5)	M register
Bit 16		VCO frequency	M	Tm(6)	M register
Bit 17		VCO frequency	M	Tm(7)	M register
Bit 18		VCO frequency	M	Tm(8)	M register
Bit 19		VCO frequency	M	Tm(9)	M register
Bit 20	MSB	VCO frequency	M	Tm(10)	M register

Bit 21 Tx VCO Trim bit 1
Bit 22 Tx VCO Trim bit 2
Bit 23 Tx VCO Trim bit 3

Tx VCO Trim Bits			
3	**2**	**1**	**Trim Number**
0	0	0	0 – Minimum C
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 – Maximum C

TxVCO Frequency = Internal Reference Frequency x ((32 x M) + A + (F/8))
Note: A>M
e.g. 935.0625MHz RF, 50kHz reference frequency, div ratio 18700.125, trim 2
Programming word = 010 1001001000 01100 001 10

PLL Data Register Contents - Cont.

NORMAL and TEST Mode Select

Bit 1	Load Control Bit 1	(Last bit loaded)	
Bit 2	Load Control Bit 2		
For Mode and Test Mode select (BIT 2 = 1, Bit 1 = 1,)			
Bit 3	Auto Gain Control	0 = Off	1 = On
Bit 4	Receive Section	0 = Off	1 = On
Bit 5	Transmit Section	0 = Off	1 = On
Bit 6	Receive Charge Pump Current	0 = 0.2mA	1 = 1.0mA
Bit 7	Transmit Charge Pump Current	0 = 0.2mA	1 = 1.0mA
Bit 8	Rx Charge Pump Polarity	0 = Normal	1 = Invert
Bit 9	Tx Charge Pump Polarity	0 = Normal	1 = Invert
Bit 10	Mixer Gain Control	(Bit 1)	
Bit 11	Mixer Gain Control	(Bit 2)	
Bit 12	Baseband Gain & RF Pad Cntrl	(Bit 1)	
Bit 13	Baseband Gain & RF Pad Cntrl	(Bit 2)	
Bit 14	Baseband Gain & RF Pad Cntrl	(Bit 3)	
Bit 15	AFC Polarity	0 = Normal	1 = Invert
Bit 16	AFC Enable	0 = Disable	1 = Enable
Bit 17	Audio/Data Output Select	0 = Analog	1 = Digital/Test
Bit 18	Mode	(Bit 1)	
Bit 19	Mode	(Bit 2)	
Bit 20	Mode	(Bit 3)	
Bit 21	Mode	(Bit 4) [Tse_0]	
Bit 22	Mode	(Bit 5) [Tse_1]	

Normal and Test Mode Programming

Mode Bits					Normal/Test Mode	
5	**4**	**3**	**2**	**1**	**I.D**	
X	X	0	0	0		Normal Mode
0	0	0	0	1	TeA	Divider outputs at AUDO (digital) - Rx on Rxsynth out; Tx on Tx synth out; Rx + Tx on Ref synth out
0	1	0	0	1	TeA	Divider outputs at AUDO (digital) Sine wave clock (P_D clock /34)
1	X	0	0	1	TeA	P_D Comparator output at AUDO (digital)
X	X	0	1	0	TeB	Digital Input to P_D from DATA and clock is from CLK
X	X	0	1	1	TeC	Demodulator test – IF filter input via AFC1, output at AUDO(analog), AFC disabled
X	X	1	0	0	TeD	I Baseband output routed to AUDO (analog)
X	X	1	0	1	TeE	Q Baseband output routed to AUDO (analog)
X	X	1	1	0	TeF	2nd Mixer output routed to AUDO (analog)
X	X	1	1	1	TeG	IF filter test – input at IF filter input via AFC1, filter output routed to AUDO (analog); AFC disabled

RECEIVER GAIN CONTROL

The receiver section includes a facility to switch overall gain to maintain linearity over a wide dynamic range of on channel signal levels. This can be done manually via the 3-wire programming interface, or automatically via an on-chip automatic gain control (AGC) circuit. The choice of manual (AGC off) or automatic (AGC on) setting of the receiver gain is controlled by bit 3 of the Mode Register.

Manual mode (AGC "Off"):

A. There is a 10dB RF pad that can be switched in before the RF input mixers
B. The RF mixer gain can be cut by 10, 20 or 30dB
C. The baseband gain can be cut by 10, 20, 30 or 40dB

See section on the Mode register for details of programming.

Manual Gain mode (Bit 3 = 0)

RF mixer Attenuation

Control Word Bits		RF Mixer Attenuation, dB
11	**10**	
0	0	30
0	1	20
1	0	10
1	1	0

Baseband and RF pad Attenuation Control Table

Control Word Bits			Baseband Stage Attenuation, dB				RF pad Attn, dB
14	**13**	**12**	**1st Block**	**2ndBlock**	**3rd Block**	**4th Block**	
0	0	0	10	10	10	10	10
0	0	1	10	10	10	10	0
0	1	0	10	10	10	0	0
0	1	1	0	10	10	0	0
1	0	0	0	10	0	0	0
1	0	1	0	0	0	0	0

e.g. Manual gain
Rx on, Tx off,
1.0mA Rx charge pump current
Normal Rx charge pump polarity,
10dB RF mixer attenuation, 20dB baseband attenuation, no RF pad
AFC enable, normal AFC polarity,
AUDO (Analog),
Normal mode,
Don't care signal evaluation period [Tse], (Auto Gain mode only)

Programming word = XX000 000 01110 X0 X1 01 0 11

RECEIVER GAIN CONTROL –Cont.

Automatic mode (AGC "On"):
Gain switches to maximum following any change made to the information in the programming registers. The gain then switches automatically according to the measured signal level (RSSI). In auto mode the mixer, RF pad, and baseband gain settings are ignored.

Signal Integration Period - Tsi
The received on channel signal is integrated in the baseband section before the second mixer. The signal integration time constant, Tsi, can be altered externally by changing the value of the capacitor, C_{GCC} attached to the pin GCC.

Tsi = 27ms * (C_{GCC}/330nF).

Signal Level Evaluation period - Tse
The integrated signal level is evaluated at intervals Tse. Tse is programmed by bits 21 & 22 of the Mode Register. The available Tse values increase with the demodulator bandwidth allowing for the signal evaluation over a similar number of baseband cycles of an on channel signal.

Possible values for Tse are:

Tse_1	***Tse_0***	***Period***
0	0	7ms * (130kHz/BWdm)
0	1	14ms * (130kHz/BWdm)
1	0	28ms * (130kHz/BWdm)
1	1	56ms * (130kHz/BWdm)

Recommendations for setting Tsi and Tse;

Tsi must be greater than the sum of the time necessary for: -
1. The baseband DC offset loop to slew to the linear region, fixed internally according to BWdm
2. Settling time of the baseband DC offset loop; loop bandwidth is100Hz
3. Integration time for the signal; ~300 cycles of the maximum in-band, baseband signal.

Recommended value for Tsi is: -
0.9ms*(130kHz/BWdm) + 1.6ms + 4.5ms*(130kHz/BWbb)
Recommended value for Tse is
>2x Tsi

If the channel is changed and the received signal is very strong necessitating a change from maximum gain to minimum gain the time taken will be 8 x Tse.

e.g. 1 For 130kHz BWbb; Tsi = 7ms;
Tse = >14ms, choose Tse2 which gives Tse=14ms for BWdm = 130kHz
Change from maximum to minimum gain 110ms.

e.g. 2 For 16kHz BWbb, Tsi = 45ms;
Tse = >45ms, choose Tse1 which gives Tse=56ms for BWdm = 16kHz.
Change from maximum to minimum gain 450ms.

RECEIVER GAIN CONTROL –Cont.

Auto Gain mode (Bit 3 = 1)

In the auto gain mode (AGC enabled), the mixer, RF pad, and baseband gain settings are ignored.

Auto Gain Switching Order

At the end of an RSSI evaluation interval, the receiver gain is left unchanged or stepped either up or down by one increment, according to the table below.

Nominal RF Signal Level		Voltage Attenuation dB					
		RF section		Baseband section			
Increasing	Decreasing	RF Pad	RF Mixer	1st Block	2nd Block	3rd Block	4th Block
	< -92dBm	0	0	0	0	0	0
> -86dBm	< -82dBm	0	0	0	10	0	0
> -76dBm	< -72dBm	0	0	0	10	10	0
> -66dBm	< -62dBm	0	10	0	10	10	0
> -56dBm	< -52dBm	0	10	10	10	10	0
> -46dBm	< -42dBm	0	20	10	10	10	0
> -36dBm	< -32dBm	0	20	10	10	10	10
> -26dBm	< -22dBm	10	20	10	10	10	10
>-16dBm		10	30	10	10	10	10

e.g. 1 Auto gain
Rx on, Tx on,
1.0mA Rx charge pump current, 0.2mA Tx charge pump polarity,
Normal Rx and Tx PLL charge pump polarity,
Don't care gain (manual gain only)
AFC enable, normal AFC polarity,
Analog AUDO,
Normal mode,
Signal evaluation period 14ms*(130kHz/BWdm)

Programming word = 01000 000 XXXXX 00 01 11 1 11

Rx/Tx PLL LOCK and RECEIVER ATTACK TIMES

Rx / Tx PLL Lock Time

The values shown below are based upon calculations using the component values shown in Fig (3).

Δ Frequency	Rx	Tx
From start up	8.5 ms	17 ms
10MHz frequency change	6.5 ms	14 ms
1.0MHz frequency change	5.0 ms	11 ms
0.1MHz frequency change	3.5 ms	7 ms

Note: The settling times for Tx are based upon a 150 Hz high pass filter (HPF) cut off frequency. This filter can be adjusted via the external TxVCO loop filter components, or by the on-chip Tx charge pump current selection. Settling time will be approximately inversely proportional to the required HPF for the tone/data signal.

Rx Baseband DC Offset Loop

Settling time is 2ms. for an effective receiver bandwidth HPF of 100Hz. The HPF can be adjusted with changing the external capacitors on DCI/DCQ. Settling time will be approximately inversely proportional to the required HPF for the data/information signal. (For additonal information refer to Bandwidth Adjustment under "Operational Frequency and Bandwidth")

RSSI Settling

If external gain control is used, a stable RSSI voltage is required at the input to the A/D converter. For a wideband signal (~25kHz deviation) the settling time to 20% accuracy is approximately 0.5ms. If the basic signal carried is varying significantly in amplitude (deviation in baseband channel) then integration over a longer time will be required. If the signal is narrow band integration will have to be increase proportionately.

Recommended 10nF external capacitor attached to RSSI gives a 20% accuracy for the received power measurement with a 130kHz bandwidth receiver. For a narrower bandwidth receiver the capacitor may need to be increased to integrate the received power over a longer time.

AFC

The AFC response time is approximately 16ms. with the component values shown in Fig. 3

Operational Frequency and Bandwidth of the CHIP-CEIVER™

Tx / Rx VCO Frequency Selection

While the NT2904 is well suited for use in the 902 to 928MHz ISM band, other frequencies outside of this band are also applicable. The transmitter or receiver can be used with RF frequencies from 100MHz to 1000MHz by suitable choice of an external inductor for the receiver and transmitter oscillator tank circuits. Approximate center frequency calculations are given below:

TxVCO f = 1/(2*PI*SQRT{(L+Lp)*4.6pF}
RxVCO f = 1/(2*PI*SQRT{(L+Lp)*1.7pF}
[Note RxVCO is 2x Rx RF local oscillator]

Were (L) is the external inductance connected to VDDT or VDDR, from both the true and inverse tank outputs. (Lp) is the parasitic inductance for the TQFP-48 package and has a value of 2.6nH (assumes negligible external capacitance)

Assuming a ±5% tolerance on L, the guaranteed oscillator range is 3% of the center frequency if the external inductor is set for devices from the center of the distribution. Devices at the edge of the distribution can be brought to the correct center frequency by selection of the appropriate oscillator trim. The Tx trim is programmed by bits 21, 22 and 23 of the transmitter frequency register; the Rx trim is programmed by bits 21 and 22 of the receiver frequency register. The VCO gains are between 2% and 4% of the total range per volt of the control voltage.

Choice of Receiver Bandwidth

The application circuit diagram is given for a 900MHz ISM band receiver with a 130kHz bandwidth. The device can be adjusted for bandwidths from 16kHz to 150kHz in the ISM band. There are 2 major elements to the receiver bandwidth: -

1. **BWbb**: the baseband bandwidth. This is defined by an 8-pole low-pass filter in both the I and Q baseband channels. The filtering in each channel is achieved by a 2-pole Sallen and Key filter, combined with and a 6-pole Gm filter. The defining resistors and capacitors for the Sallen and Key filters are off chip; the Gm filter is totally on-chip except for one bandwidth trimming resistor. Note that the bandwidth of the individual channels is 0.5*BWdm.

2. **BWdm**: the demodulator bandwidth. This is the bandwidth of the Period to Digital demodulator. It is a ‘brick wall’ filter centered on the IF frequency.

3. The DC offset correction feedback loop in the baseband section introduces an effective high-pass filter (100Hz) in the center of the RF band.

Operational Frequency and Bandwidth of the CHIP-CEIVER™ – Cont.

4. There is filtering in the IF section following the second mixer designed to attenuate mixer products prior to the demodulator. Filtering is defined by a 4-pole low-pass filter followed by a single-pole high-pass filter. The low-pass filter is an on-chip Gm design with an off chip bandwidth trimming resistor and the high-pass filter is on-chip and fixed in frequency.

Bandwidth Adjustment

A. Sallen and Key baseband filters

The R and C components for these filters are off chip. To set the baseband bandwidth, BWbb, adjust the C values. Choose values to provide a bandwidth equal to or slightly greater than the required bandwidth, according to the following formula. The recommended component tolerances for resistors should be 1%, with capacitor tolerances of 5%, or better.

The capacitor attached to IFIL2/QFIL2 = 1.8nF*(130kHz/BWbb).

The capacitor attached to IFIL3/QFIL3 = 0.68nF*(130kHz/BWbb).

e.g., for a required 32kHz bandwidth suggested values of 6.8nF and 2.6nF give a bandwidth of 34kHz.

B. Gm baseband filter

On-chip baseband filter bandwidth is adjusted by choice of the external resistor between VDDA and BBSET. Choose this resistor to give a bandwidth calculated from "A" above.

R = 22kΩ * (130kHz/BWbb).

e.g., for 34kHz bandwidth suggested value is 82kΩ.

C. Demodulator

Demodulator bandwidth, BWdm, is adjusted by the choice of the Period to Digital demodulator clock frequency, Fpd. The chip divides down the receiver local oscillator, Frf, by the divide ratio, PDR, to obtain Fpd. PDR is programmed by bits 14, 15 & 16 of the reference frequency register. Allowable PDR ratios are 2[1], 6[2], 12, 24, 36, 48, 72, 96.

The choice of Fpd directly sets the IF frequency, Fif, and BWdm: -

Fpd = Frf/PDR Fif = Fpd/544 BWdm = Fpd/580

Choose a value of PDR to give BWdm > BWbb.

[1]Ratio 2 can only be used with Frf < 180MHz
[2]Ratio 6 can only be used with Frf < 520MHz

Examples

Frf, MHz	PDR	Fpd	Fif	BWdm
915	12	76.25MHz	140.2kHz	131.5kHz
930	48	19.4MHz	35.6kHz	33.4kHz
430	6	71.7MHz	131.7kHz	123.6kHz

Operational Frequency and Bandwidth of the CHIP-CEIVER™ – Cont.

IF Filter

The bandwidth of the on-chip IF low-pass filter, which precedes the Period to Digital demodulator, should be optimised as follows. Following the calculation of Fif and BWdm from C. above, the filter bandwidth is adjusted by choice of the external resistor between VDDA and IFSET.

R = 22kΩ * 206kHz/(Fif+0.5*BWdm).

e.g., for Fif=35.6kHz, BWdm = 33.4kHz optimum bandwidth is 53kHz, therefore choose R=86KΩ.

The on-chip IF high-pass filter is fixed at 8kHz.

DC Offset Correction Loop (Effective High-Pass baseband filter)

The 3dB bandwidth is set to ±100Hz by the external 330nF capacitors connected to DCI and DCQ. Adjustment by increasing the capacitor value in inverse proprtion to the chose BWdm is possible. Reduction in the cut of with BWdm=130kHz may lead to instability in the Auto Gain set mode.

Impedance of NT2904 RF ports, Packaged and COB (Bare Die)

These results are from simulation at 915MHz using a SPICE based simulator. Results are given for chip alone, chip + bond wire and chip + bond wire + package.

48 pin TQFP Package model

The model includes bond wires with a length of 1.2 to 1.4mm, which is the bond wire length for the NT2904.

The total inductance per pin is 2.5nH.
The series resistance per pin is 0.1Ω.
There is a capacitance between adjacent pins is 96fF situated chip side.
There are capacitances of 50fF to ground chip side and PCB side
Approximately the mutual inductance coupling factors used are:-

Adjacent bond/package pin	0.4
Next adjacent bond/package pin	0.3
Next, next adjacent bond package pin	0.2
Next, next, next adjacent bond package pin	0.1

Chip On Board model

For COB, bond wire lengths of approximately 1.3mm have been assumed. This represents about 0.8nH. The total series inductance per pin in the model should be reduced to 1.0nH to approximate this situation. Mutual inductance coupling and capacitances are approximately the same.

Interface Impedance

This can be expressed simply as a ***parallel*** R/C or R/L combination between the differential ports. This is the two element combination which most closely represents the physical situation and is valid over ~±10% of the 915MHz center frequency(except for the receiver input with the RF pad switched in, here a ***series*** R and L would have been more representative).

Impedance of NT2904 RF ports, Packaged and COB – Cont.

Receiver Input, no RF pad	nH per pin[1]	Parallel R	Parallel C or L
Packaged 2904[2]	2.5	59Ω	0.93pF
COB 2904[2]	1.0	78Ω	1.55pF
2904 at IC pads	0	82Ω	1.45pF
Receiver Input, with 10dB RF pad			
Packaged 2904[2]	2.5	50Ω	5.5nH
COB 2904[2]	1.0	15Ω	9.7nH
2904 at IC pads	0	14Ω	0.83pF
Transmitter Output (exact balance)			
Packaged 2904[2]	2.5	3130Ω[3]	1.27pF
COB 2904[2]	1.0	3100Ω[3]	1.15pF
2904 at IC pad level	0	4400Ω[3]	0.92pF

[1]Excluding mutual inductance
[2]Approximate package/bond models
[3]This is for perfect balance, in reality any imbalance in the package, balun or chip will reduce the real part of the output impedance drastically, assume 700ohms.

For single ended modeling, (not differential) replace the differential combination by a parallel 0.5*R and 2*C(or 0.5*L) from each interface pin to ground.

VCO Inductor values for COB

Change the length of the external VCO tank inductors (Printed on PCB) to compensate for the change in bond wire/package inductance, while taking into account the coupling factor which reduces the inductance.

Changing from a NT2904 in a TQFP to a NT2904 COB the inductance per bond will decrease by approximately:-

$$[2.5*(1-0.4) – 1.0*(1-0.4)] = 0.9nH$$

Designs for the external inductors are given in the section under “Operational Frequency and Bandwidth”. Simulation predict for a 1mm thick dielectric, the inductor arms must be increased in length by 2.4mm to result in the same oscillation frequency. For a 0.6mm thick dielectric increase by 2.6mm.

GENERAL OPERATIONAL and USAGE INFORMATION

Board Layout

Designing ultra-high frequency (UHF) RF circuits requires careful attention to detail and layout. Careful attention to layout should be observed to minimize stray inductance and capacitance effects. This attention to detail will preserve RF sensitivity of the NT2904 **CHIP-CEIVER**™. At high frequencies, microstrip or strip-line transmission line techniques must be employed. Using "state-of-the-art" CAD techniques for PCB layout, standard FR-4 fiberglass PCB material (1.6-mm thickness) may be employed. For maximum performance, however, RF quality substrate material should be used.

Supply Decoupling

Positive supply connections for the NT2904 are nominally 2.7V to 3.3V. All supply pins must be bypassed to an RF, Analog, or Digital ground plane depending upon the type of supply pin. For RF supply pins, a 100 pF ceramic capacitor in parallel with a 1.0 nF ceramic capacitor, both RF quality, should provide adequate decoupling. For analog and digital supply pins, 0.01-0.1µF RF quality capacitors should be used. The bypass capacitors should be placed as close to all power supply pins as possible. An effort should be made to minimize the trace length between the capacitor leads and the respective NT2904 power supply and common pins.

Grounding

The circuit designer should attempt to locate the NT2904 **CHIP-CEIVER**™, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid RF analog ground should be placed around the LNA and associated RF filter circuitry, while a solid digital ground should be placed around the reference oscillator. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. Ground connections for the NT2904. Connect all ground pins together to a low impedance ground plane, as close to the device as possible. Observe proper RF grounding and shielding techniques. The NT2904 **CHIP-CEIVER**™ should be used with separate analog and digital ground planes. The digital and analog ground planes should be "summed" at one point, typically at the power supply filter capacitor.

GENERAL OPERATIONAL and USAGE INFORMATION – Cont.

Operating Precautions

NUMA Technologies' plastic molded BiCMOS LSI devices are designed and manufactured for trouble-free operation when used under normal operating conditions. Our products are subjected to stringent electrostatic, mechanical strength, and environmental tests for assured reliability. When working with our products the user should observe the following precautions:

(1) Use the product in the range of the rated operating voltage, operating temperature, operating input/output voltage and input/output current. If the product is used outside these operating parameters, the user may experience high failure rates.

(2) Do not expose the product to excessive mechanical vibration, repetitive shock, or rapid or cyclic temperature changes. These factors can cause the bond wires in the plastic package to break.

(3) Although all terminals have electrostatic protection, damage may still occur if very high electrostatic potentials are applied. Use of a conductive container or aluminum foil for packaging and transportation is recommended. (Untreated plastic containers are NOT recommended.) Use grounded soldering tools and test equipment.

(4) The NT2904 employs Electrostatic Discharge (ESD) protection. CMOS inputs shall be rated to 2Kv human body model / 1Kv charge contact model. Bipolar RF inputs shall be protected to the greatest extent possible and consistent with industry standards, while meeting RF performance parameters.

APPLICATION INFORMATION -- "900 MHz" Analog Cordless Telephone

A circuit diagram for a high performance, cordless telephone transceiver is shown in Figure (3). This circuit is applicable to cordless phones compliant for use in the USA operating in the 902-928 MHz ISM band. The circuit will operate with a supply voltage of 2.7V to 3.3V. The "adjustment free" discriminator of the **CHIP-CEIVER**™, along with the elimination of IF filters, provides a cost effective solution to cordless telephone applications.3

Tuning and power management functions for the NT2904 (U2) are accessed via an industry standard 3-wire compatible serial interface. The "printed" VCO inductors (L4, L5, L7, and L8) allow the transceiver to be tuned over the range of 902 to 928 MHz. An RF SAW filter (FL1) provides all of the required RF filtering. A low cost microprocessor with an analog-to-digital converter (A/D) input, can be used to measure the RSSI pin (36) of U2, which is proportional to the receive signal strength.

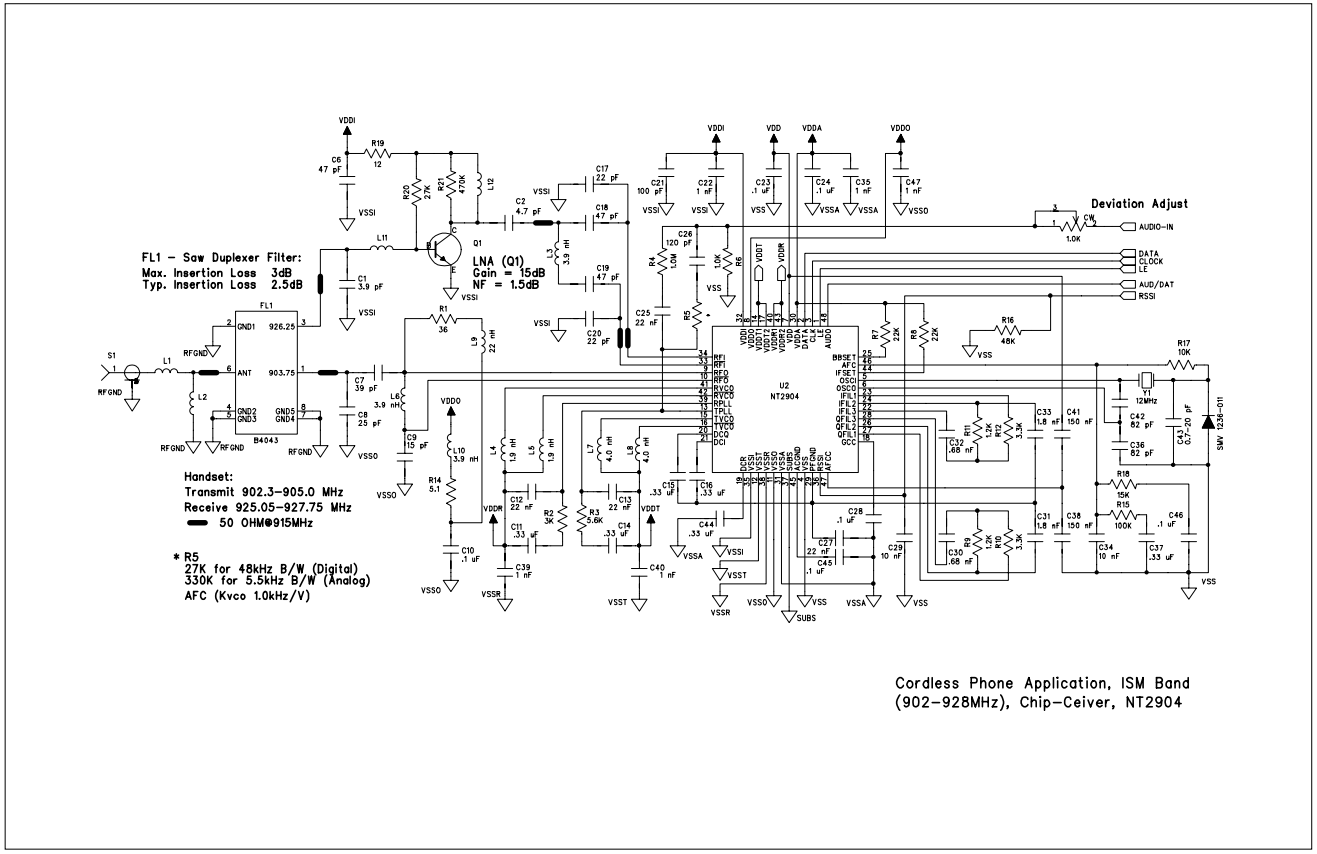


Figure (3), "900 MHz", High Performance, Cordless Telephone

Frequency Tables:

This section outlines the frequencies and corresponding channel numbers used by the handset and base unit of both 900 MHz analog and digital phones.

Handset:

Channel	Transmit	Receive	Rx LO
1	925.05	902.3	1804.6
2	925.35	902.6	1805.2
3	925.65	902.9	1805.8
4	925.95	903.2	1806.4
5	926.25	903.5	1807.0
6	926.55	903.8	1807.6
7	926.85	904.1	1808.2
8	927.15	904.4	1808.8
9	927.45	904.7	1809.4
10	927.75	905.0	1810.0

Base:

Channel	Transmit	Receive	Rx LO
1	902.3	925.05	1850.1
2	902.6	925.35	1850.7
3	902.9	925.65	1851.3
4	903.2	925.95	1851.9
5	903.5	926.25	1852.5
6	903.8	926.55	1853.1
7	904.1	926.85	1853.7
8	904.4	927.15	1854.3
9	904.7	927.45	1854.9
10	905.0	927.75	1855.5

ORDERING INFORMATION

Manufacturer
Device Identification

NUMA Technologies

Package Type		Example Prefix	Device	Suffix
B	Ball Grid Array	**NT**	**2904**	**G I**
C	Chip Scale Package (CSP)			
D	Die Form			
F	Flip-Chip			
G	Thin Quad Flat Pacakge (TQFP, LQFP)	Package		
Q	Quad Flat No Lead (QLP, QFN, MLF)	Temperature		
N	Special			
B	0 to 70°C			
I	-20 to 65°C			
J	-40 to 85°C			
K	-55 to 85°C			
S	Prototype Part			