NUD3112LT1

Integrated Relay, Inductive Load Driver

This device is used to switch inductive loads such as relays, solenoids incandescent lamps, and small DC motors without the need of a free-wheeling diode. The device integrates all necessary items such as the MOSFET switch, ESD protection, and Zener clamps. It accepts logic level inputs thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

- Provides a Robust Driver Interface Between D.C. Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays of 12 V Rail
- Capable of Driving Relay Coils Rated up to 6.0 W at 12 V
- Internal Zener Eliminates the Need of Free-Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter Systems Operation
- Low $V_{DS(ON)}$ Reduces System Current Drain

Typical Applications

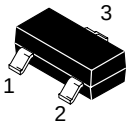
- Telecom: Line Cards, Modems, Answering Machines, FAX
- Computers and Office: Photocopiers, Printers, Desktop Computers
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders
- Industrial:Small Appliances, Security Systems, Automated Test Equipment, Garage Door Openers

ON Semiconductor®

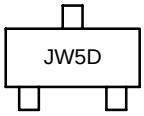
http://onsemi.com

Relay, Inductive Load Driver
Silicon SMALLBLOCK™
0.5 Ampere, 16 V Clamp

MARKING DIAGRAM

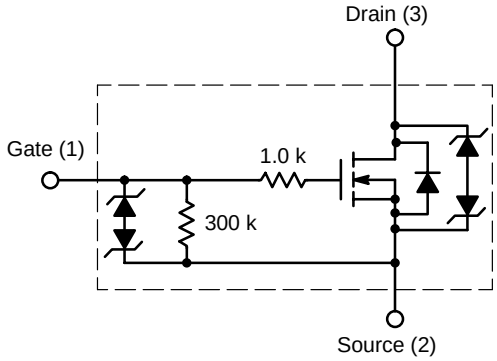


SOT-23 (TO-236)
CASE 318
Style 21



JW5 = Specific Device Code
D = Date Code

INTERNAL CIRCUIT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping
NUD3112LT1	SOT-23	3000 Units/Reels

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Rating	Value	Unit
V_{DSS}	Drain to Source Voltage – Continuous	14	V_{dc}
V_{GS}	Gate to Source Voltage – Continuous	6	V_{dc}
I_D	Drain Current – Continuous	500	mA
E_z	Single Pulse Drain-to-Source Avalanche Energy ($T_{Jinitial}$ = 25°C)	50	mJ
E_{zpk}	Repetitive Pulse Zener Energy Limit (DC ≤ 0.01%) (f = 100 Hz, DC = 0.5)	4.5	mJ
T_J	Junction Temperature	150	°C
T_A	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
P_D	Total Power Dissipation (Note 1) Derating Above 25°C	225 1.8	mW mW/°C
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (Note 1)	556	°C/W
ESD	Human Body Model (HBM) According to EIA/JESD22/A114	2000	V

1. Mounted onto minimum pad board.

TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
V_{BRDSS}	Drain to Source Sustaining Voltage (Internally Clamped) (I_D = 10 mA)	14	16	17	V
B_{VGSO}	I_g = 1.0 mA	-	-	16	V
I_{DSS}	Drain to Source Leakage Current (V_{DS} = 12 V , V_{GS} = 0 V, T_A = 25°C) (V_{DS} = 12 V, V_{GS} = 0 V, T_A = 85°C)	 - -	 - -	 20 40	μA
I_{GSS}	Gate Body Leakage Current (V_{GS} = 3.0 V, V_{DS} = 0 V) (V_{GS} = 5.0 V, V_{DS} = 0 V)	 - -	 - -	 19 50	μA
ON CHARACTERISTICS					
$V_{GS(th)}$	Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1.0 mA) (V_{GS} = V_{DS}, I_D = 1.0 mA, T_A = 85°C)	 0.8 0.8	 1.2 -	 1.4 1.4	V
$R_{DS(on)}$	Drain to Source On-Resistance (I_D = 250 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 5.0 V) (I_D = 500 mA, V_{GS} = 3.0 V, T_A=85°C) (I_D = 500 mA, V_{GS} = 5.0 V, T_A=85°C)	 - - - - -	 - - - - -	 1.2 1.3 0.9 1.3 0.9	Ω
$I_{DS(on)}$	Output Continuous Current (V_{DS} = 0.25 V, V_{GS} = 3.0 V) (V_{DS} = 0.25 V, V_{GS} = 3.0 V, T_A = 85°C)	 300 200	 400 -	 - -	mA
g_{FS}	Forward Transconductance (V_{OUT} = 12.0 V, I_{OUT} = 0.25 A)	350	490	-	mmhos

TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 1.0 MHz)	-	23	-	pF
C_{oss}	Output Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 1.0 MHz)	-	30	-	pF
C_{rss}	Transfer Capacitance (V_{DS} = 12.0 V, V_{GS} = 0 V, f = 1.0 MHz)	-	7	-	pF
SWITCHING CHARACTERISTICS					

Symbol	Characteristic	Min	Typ	Max	Units
	Propagation Delay Times:				nS
t_{PHL}	High to Low Propagation Delay; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	-	21	-	
t_{PLH}	Low to High Propagation Delay; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	-	91	-	
	Transition Times:				nS
t_f	Fall Time; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	-	36	-	
t_r	Rise Time; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	-	61	-	

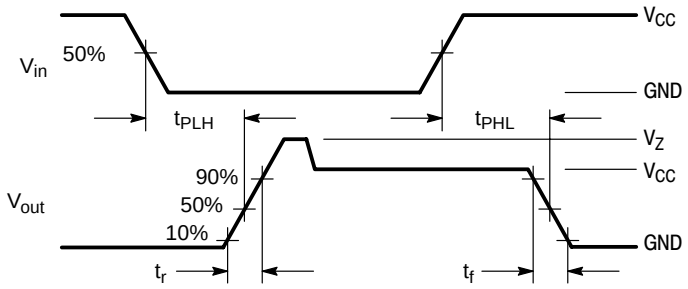


Figure 1. Switching Waveforms

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise specified)

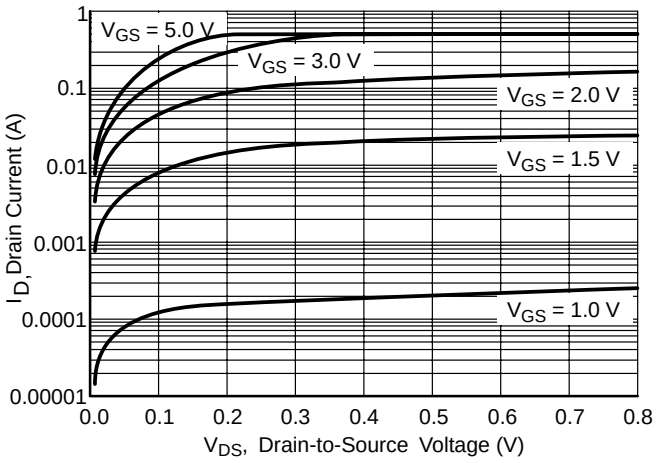


Figure 2. Output Characteristics

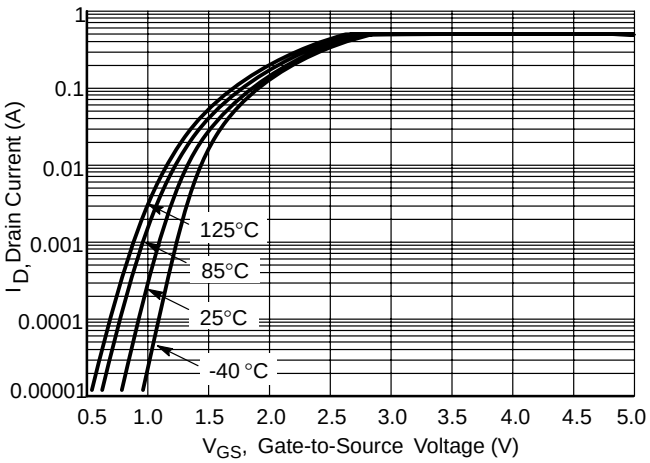


Figure 3. Transfer Function

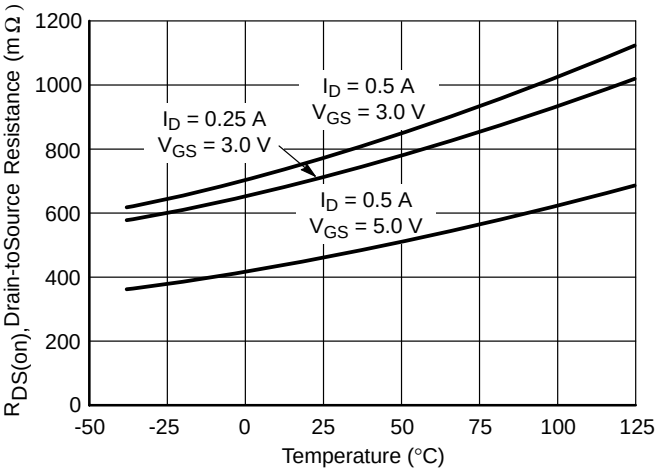


Figure 4. On-Resistance Variation vs. Temperature

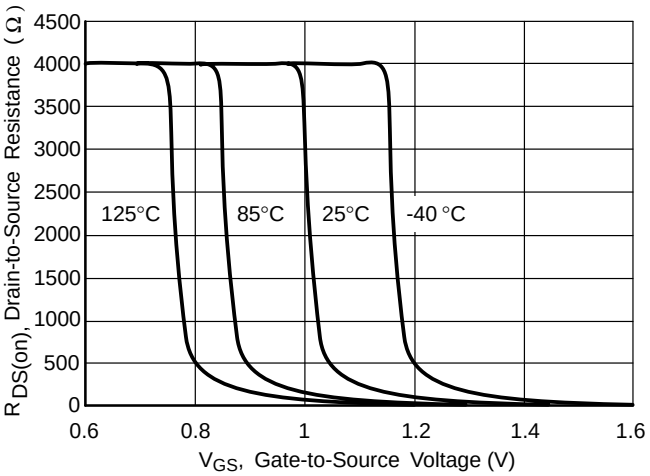


Figure 5. $R_{DS(ON)}$ Variation vs. Gate-to-Source Voltage

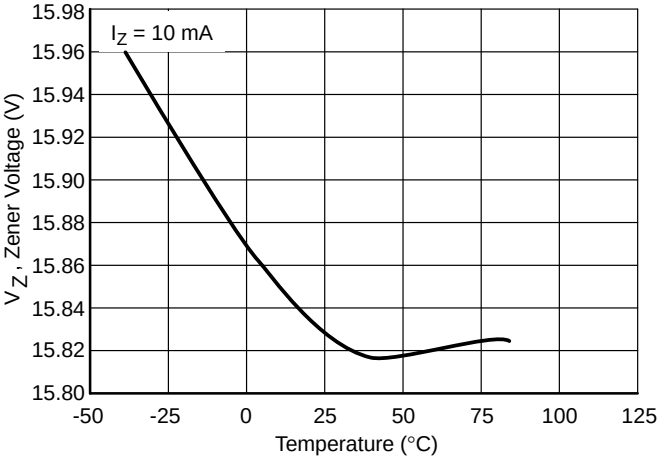


Figure 6. Zener Voltage vs. Temperature

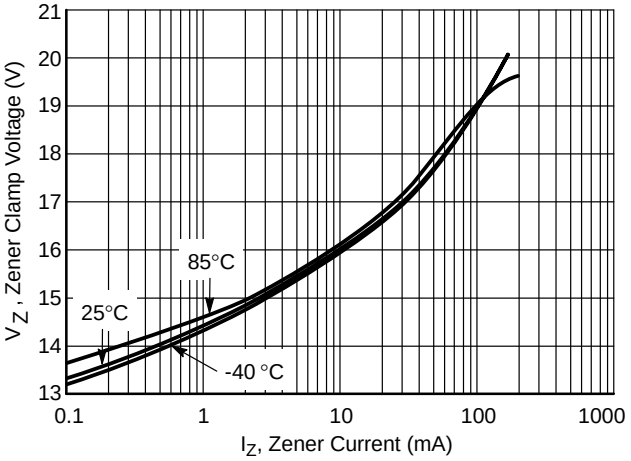


Figure 7. Zener Clamp Voltage vs. Zener Current

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise specified)

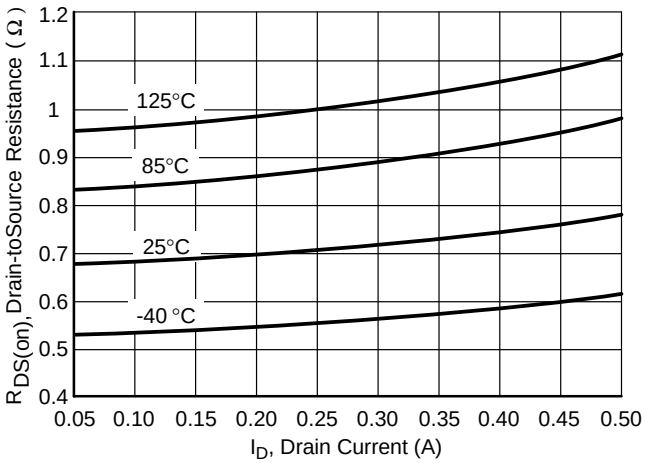


Figure 8. On-Resistance vs. Drain Current and Temperature

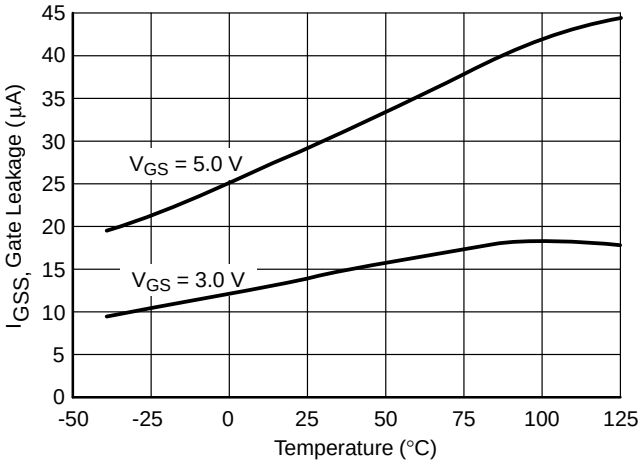


Figure 9. Gate Leakage vs. Temperature

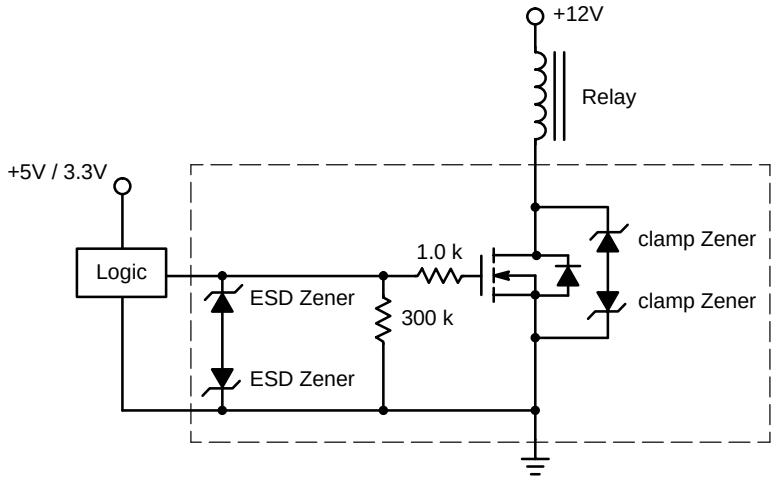
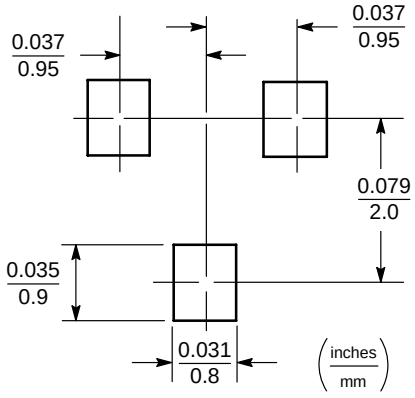


Figure 10. Typical Application Circuit

INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23

SOT-23 POWER DISSIPATION

The power dissipation of the SOT-23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT-23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT-23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

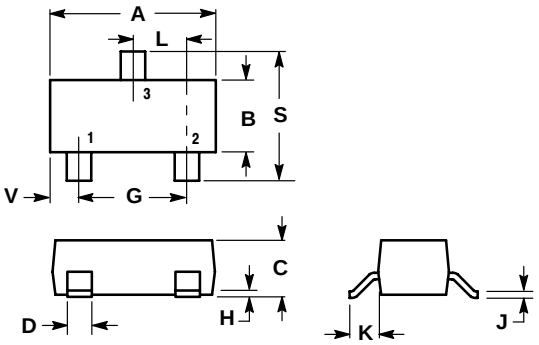
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−03 AND −07 OBSOLETE, NEW STANDARD 318−08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

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