NX25F640C

NEXFLASH® Technologies, Inc.

64M-BIT SERIAL FLASH MEMORY WITH 4-PIN SPI INTERFACE

ADVANCED
JANUARY 2001

FEATURES

- **Flash Storage for Resource-Limited Systems**
  - Ideal for portable/mobile and microcontroller-based applications that store data, audio, and images
- **Nonvolatile Memory Technology**
  - Single transistor EEPROM memory
  - Erase/Write time of 10 ms/sector (typical)
  - Small DOS compatible sectors 512+16 (528) bytes for erase and write
  - AutoVerify function ensures that a sector is written accurately.
  - Optional 32KB block and sector erase for programming
  - 10K (Sector), 100K (Block) erase/write cycles
  - Ten years data retention
- **4-pin SPI Serial Interface**
  - Easily interfaces to popular microcontrollers
  - Clock operation as fast as 13 MHz (standard) 16MHz (Special Clock Mode)
- **Ultra-low Power for Battery-Operation**
  - Single 2.7-3.6V supply for Read, Erase/Write
  - Less than 1 μA standby, 5 mA active (typical)
- **Special Features for Media-Storage Applications**
  - On-board 528 Byte SRAM Buffer
  - Byte-level addressing
  - Auto-increment sector read
  - Transfer and Compare sector to SRAM
  - Configurable software write-protection
  - In-system electronic serial number.
  - Serial Flash Development Kit
- **Package Options**
  - 32 Pin TSOP Surface Mount
  - Removable Cards and Modules

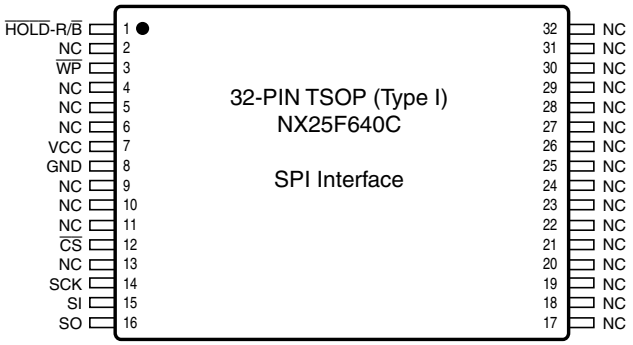
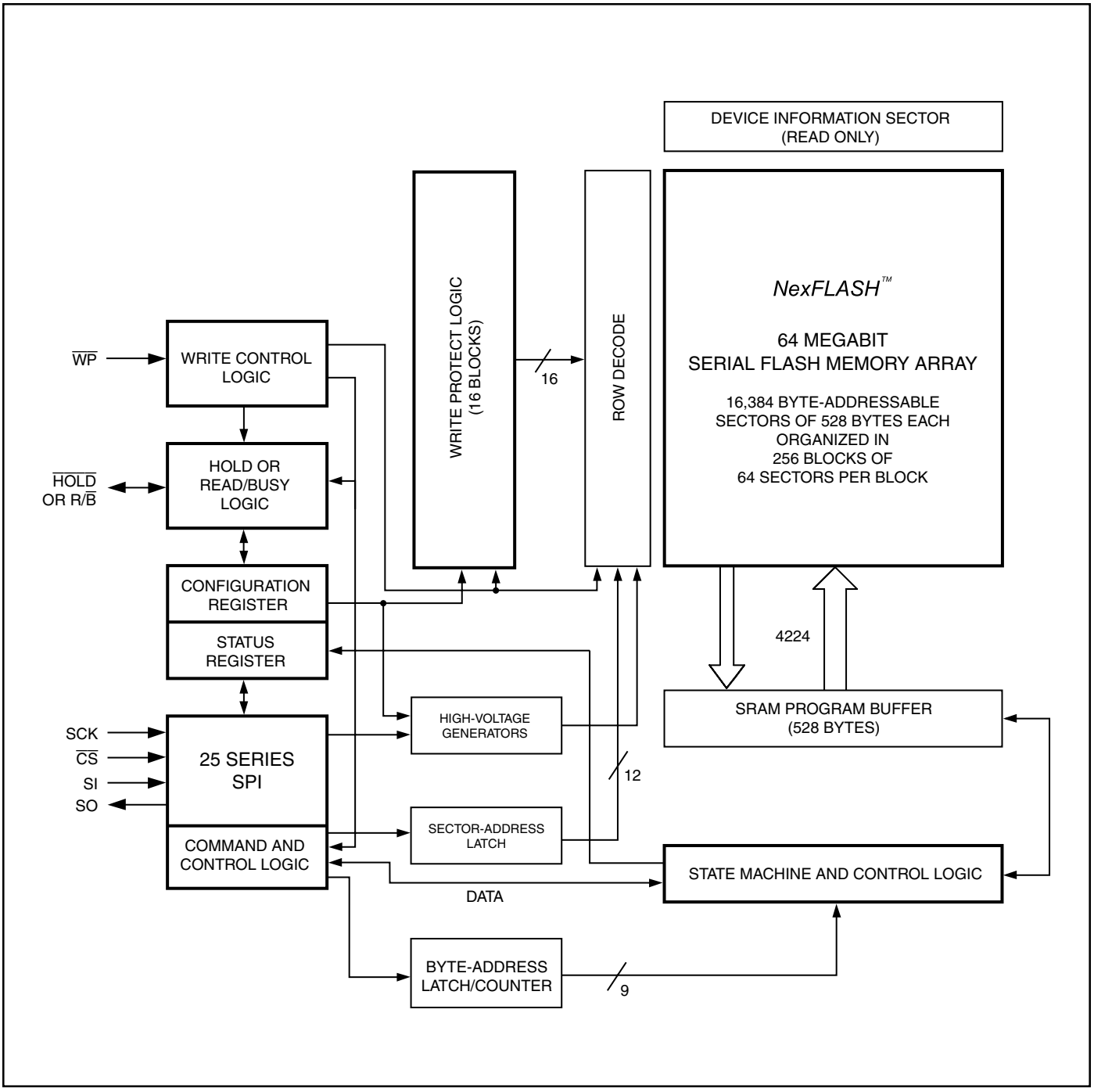


Table 1. Pin Descriptions for the 25F640

SI	Serial Data Input
SO	Serial Data Output
SCK	Serial Clock Input
$\overline{CS}$	Chip Select Input
$\overline{WP}$	Write Protect Input
$\overline{Hold}$, R/$\overline{B}$	Hold Input Ready-Busy Output or No Connect
VCC	Power Supply
GND	Ground



NX25F640C Architectural Block Diagram

Pin Descriptions

Serial Data Input (SI)
The SI pin receives data into the device with the SCK pin. All data transmitted to the device is clocked relative to the rising edge of SCK.

Serial Data Output (SO)
The SO pin transmits data from the device with the SCK pin. All data transmitted from the device is clocked relative to the edge defined with the SPI-RCE bit defined in the configuration register. The default will be to output data on the falling edge of the SCK pin, which is compatible with standard systems that support SPI. With the SPI-RCE bit set, the clock rate can be up to 16Mhz. With the SPI_RCE bit reset, the clock rate can be up to 13Mhz.

Serial Clock Input (SCK)
All commands and data written to the SI pin/SO pin are clocked relative to the falling or rising edge of SCK. The clock rate may be up to 16Mhz.

Chip Select ($\overline{CS}$)
The chip select input is required to start and finish an SPI command. SCK must be low when chip select is asserted low. Upon power-up, an initial low-high transition of chip select is required before any command will be acknowledged. Once the device is de-selected, the SO pin will enter a high impedance state and power consumption will be reduced to standby levels unless a transfer, compare, or sector programming are in progress. If a transfer, compare, or sector programming is in progress, the command will complete and then device will enter standby mode.

Write Protect Input ($\overline{WP}$)
The write protect input (WP) works in conjunction with the configuration register bits WR3..WR0, WD, and the status register bit WE. When WP is asserted low, the entire flash memory array is write protected. When the WP pin is high and the status register WE bit set, the device addresses corresponding to the write protect range and direction are write protected. When the status register bit WE is reset, the entire array is write protected. See the section on the configuration register for more details.

HOLD or Ready/Busy ($\overline{HOLD}$ or R/$\overline{B}$)
This multifunction pin can serve either as a Hold input (HOLD) or as a Ready/Busy output (Ready-/Busy). The pin function is user programmable through the configuration register bits SPI-HR0, SPI-HR1. The device comes from the factory with this pin programmed as a No Connect (NC). The pin can be re-configured by the user by writing to the configuration register.

Power Supply Pins (Vcc and Gnd)
The NX25F640 supports a single power supply between 2.7V and 3.6V connected to the Vcc and Gnd pins.

Configuration Register

The Configuration register stores the current configuration of the HOLD-Read/Busy pin, SPI Read Clock Edge, Write protect range and direction, and NXS treset time.

All Reserved bits (Reserved) should be set to 0 while programming.

Write Protect Range and Direction (WR3-WR0,WD)
The WR3-WR0 bits define the write-protect range. The WD bit defines the write-protect direction.

The $\overline{WP}$ pin and the WE bit in the status register control the write protect function. If the $\overline{WP}$ pin is active (low) or the WE bit in the status register is reset, then the entire array is write-protected. If the $\overline{WP}$ pin is in-active (high) and the WE bit in the status register is set, then the write protect range and direction are active. This allows a portion of the array to be write-protected all of the time. Note each bit represents 64 sectors in the write-protect range.

Read Clock Edge (RCE)
The Read Clock Edge bit selects which edge of the clock (SCK) is used while reading data out of the device. Although the SPI protocol specifies that data is written to the device on the rising edge of SCK and read on the falling edge of SCK, this bit allows the data to be read on the rising edge of SCK. This is necessary for SCK frequencies above 13Mhz.

RCE=0 Read data is ouput on the falling edge of SCK.
RCE=1 Read data is output on the rising edge of SCK.

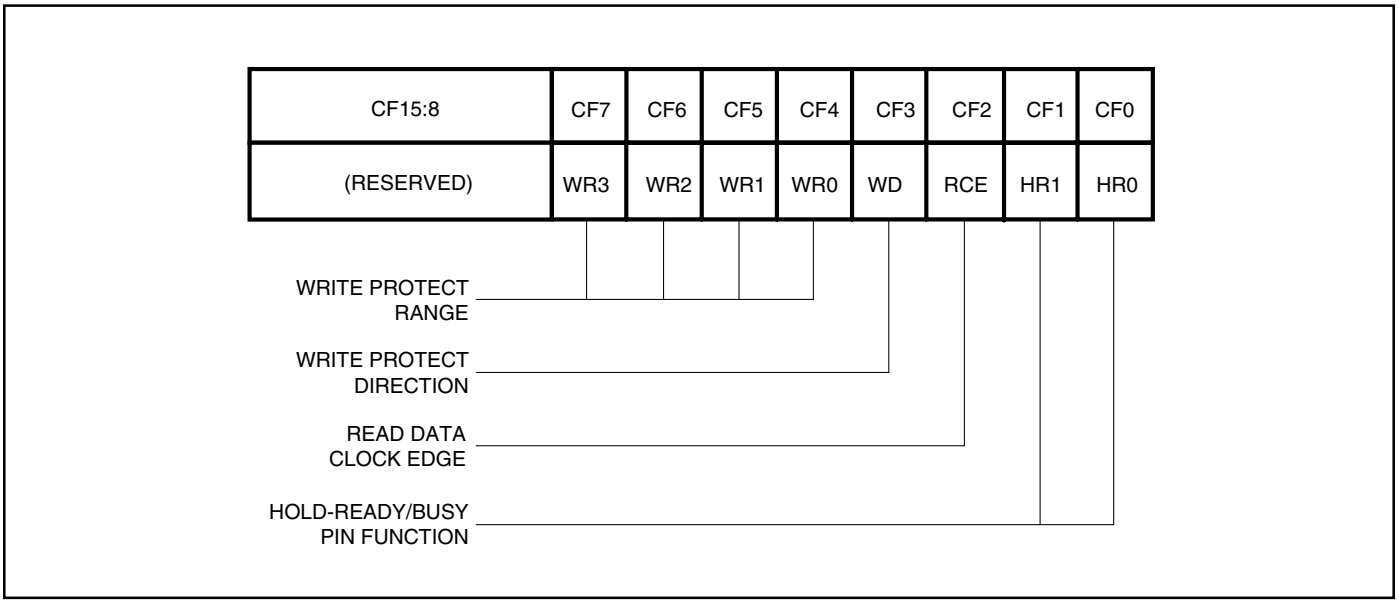


Figure 7. Configuration Register Bit Locations

Table 2. Write Protect Range Sector Selection (Hex)

Write Protect Range Config. Bits				Write Protected Sectors	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	0000-003F	3FC0-3FFF
0	0	1	0	0000-007F	3F80-3FFF
0	0	1	1	0000-00BF	3F40-3FFF
0	1	0	0	0000-00FF	3F00-3FFF
0	1	0	1	0000-013F	3EC0-3FFF
0	1	1	0	0000-017F	3E80-3FFF
0	1	1	1	0000-01BF	3E40-3FFF
1	0	0	0	0000-01FF	3E00-3FFF
1	0	0	1	0000-023F	3DC0-3FFF
1	0	1	0	0000-027F	3D80-3FFF
1	0	1	1	0000-02BF	3D40-3FFF
1	1	0	0	0000-02FF	3D00-3FFF
1	1	0	1	0000-033F	3CC0-3FFF
1	1	1	0	0000-037F	3C80-3FFF
1	1	1	1	ALL	ALL

$\overline{\text{HOLD}}$-R/$\overline{\text{B}}$, HR[1:0]
The Hold-Ready/Busy bits SPI-HR1 and SPI-HR0 select one of four possible functions for the Ready/Busy pin on the device.

HR1	HR0	***Pin Configuration***
0	0	HOLD input
0	1	No Connect
1	0	Ready/Busy output (Open Drain)
1	1	Ready/Busy output

Status Register Bit Descriptions

The status register contains the status for all operations of the device. The following table defines the bit definition of the status register.

Ready/Busy status (Busy)
The busy status bit reflects the ready/busy status of the chip. If the busy status bit is set, then a SRAM transfer, SRAM compare, array program, or array erase operation is in progress. No operations on the flash array may be performed while the Busy bit is set. If an SRAM only operation needs to be performed, the chip can be busy, but the TR0 bit must be clear. If a non-array and non-SRAM oriented command needs to be performed, it can be performed at any time.

SRAM buffer 0 Transfer (TR0)
The TR0 bit indicates that a transfer operation involving SRAM buffer 0 is in operation. The Busy bit will also be set when TR0 is set. When this bit is set, a command which uses SRAM buffer 0 cannot be executed.

Write Enable (WE)
This bit indicates whether the main flash array and the configuration register can be written to. The Write Enable and Write Disable command control this bit. Upon power-up, the WE bit is reset, and the main flash array write protected.

Compare Not Equal (CNE)
This bit provides the result of a Compare Sector with SRAM command. The CNE bit is clear at power-up. At the completion of a Compare Sector with SRAM command, this bit is set if the compare failed, and clear if the compare succeeded.

Error Erase (EE)
This bit provides status for the last erase operation on the main flash array. If this bit is set, then the last erase operation failed, and some bits did not program to the erased state (“1”). If this bit is clear, then the last erase operation succeeded. This bit could be used in conjunction with an ECC algorithm and/or a sector relocation algorithm.

Error Write (EW)
This bit provides status for the last AutoVerify write operation on the main flash array. If this bit is set, then the last verify operation failed, and some bits did not program to the non-erased state (“0”). If this bit is clear, then the last AutoVerify write operation succeeded. This bit could be used in conjunction with an ECC algorithm and/or a sector relocation algorithm.

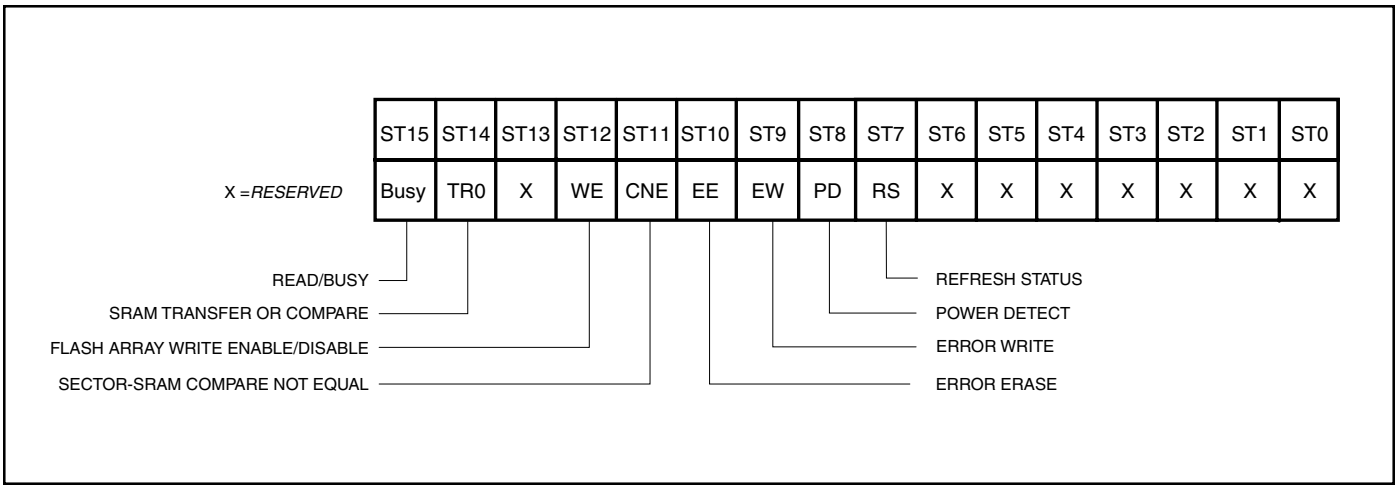


Figure 8. Status Register Bit Locations

Power Detect (PD)
This bit provides allows the detection of whether power has been removed from the device. It works in conjunction with the Set Power Detection Bit and Reset Power Detection Bit commands. When the device powers up this bit is cleared. Application firmware can use this bit to detect when a Serial Flash Module has been removed, by setting this bit, and polling the bit during status reads. If the bit is clear, then power has been removed, and the module changed.)

Refresh Status (RS)
This bit provides the user with an indication that the flash sectors in the current block may need to be refreshed. When this bit is clear no refresh is required. When this bit is set, the block that the last sector resides in needs to be refreshed.

Command Set

The following are rules used for all commands in SPI mode:

- All data is shifted into the device MSB first.
- All data is shifted out of the device MSB first.
- Chip reset is defined as a low to high transition of $\overline{CS}$. Thus, to reset the chip at power on, a high to low to high transition is required.
- A command may start after a high to low transition of $\overline{CS}$. When a command is started, $\overline{CS}$ needs to stay low for the duration of the command and data.

Command Block Bit Definition
The commands for the SPI mode must assert $\overline{CS}$, send a command from the NexFlash Common Command Set, and de-assert $\overline{CS}$.

Refer to the NexFlash Common Commands section for the structure of the supported commands.

Command Set for the NX25F640C Serial Flash Memory

Command Name	Byte 0	Byte 1-2[4]	Byte 3-4[4]	n- bytes *(Italics indicate devise output)*		
Sector Commands						
Read From Sector	52H	Sector	Byte	0000h	*Ready/Busy*	*Read Data*
Read From Sector w/AutoInc	50H	Sector		0000h	*Ready/Busy*	*Read Data*
Write Enable [1]	06H					
Write Disable [1]	04H					
Write to Sector (through SRAM) [2]	F3H	Sector	Byte	Write Data	00h	
Re-Write Sector through SRAM [2]	58H	Sector	Byte	Write Data		
Serial SRAM Commands						
Write to SRAM [2]	72H	Byte	Write data	00h		
Read from SRAM [1]	71H	Byte	00h	Read Data		
Transfer all of SRAM to Sector [2]	F3H	Sector	0000h			
Transfer all of Sector to SRAM [2]	53H	Sector	0000h			
Compare all of Sector to SRAM [2]	8DH	Sector	0000h	0000h		
Configuration and Status Commands						
Read Configuration [1]	8CH	Config				
Write Non-Volatile Configuration Register [1]	8AH	Config	0000h			
Read Status Register [1]	84H	Status				
Set Power Detection Bit [1]	03H					
Reset Power Detection Bit [1]	09H					
Read Device Information Sector	15H	0000h	0000h	0000h	*Ready/Busy*	*DIS Data*
Special Sector Commands						
Erase Sector [3]	F1H	Sector	0000h			
Erase Block [3]	F4H	Block	0000h			
Write-Only to Sector thru SRAM [3]	F2H	Sector	Byte	Write Data	00h	

Notes:
1. Command may be used when device is busy
2. Command may not be used when device is busy and TR bit=0
3. Warning: Read description of these commands before using to ensure reliable operation.
4. Sector, Block and Byte are address references.

Read From Sector with Auto Increment

The Busy bit in the status register must be clear to use this command. The Ready Busy Word, or the status register busy bit may be used to poll for the ready condition. If the Ready Busy word is 9999h, then each consecutive data clock reads a bit in the selected sector starting at Sector Address SA15..0. At the end of the sector, the data continues at Byte 0 on the next Sector Address. On the last Sector Address in the device, the device will wrap to Sector 0 and continue reading. If the Ready Busy word is 6666h, then the chip is busy and should be reset to restart a command.

Read From Sector

The Busy bit in the status register must be clear to use this command. The Ready Busy Word, or the status register busy bit may be used to poll for the ready condition. If the Ready Busy word is 9999h each consecutive data clock reads a bit in the addressed sector SA15..0 starting at the Byte Address BA15..0. At the end of the sector, the data wraps to Byte 0 and continues reading. If the Ready Busy word is 6666h, then the chip is busy and should be reset to restart a command.

Write to Sector Through SRAM

The Busy bit and the TR0 bit in the status register must be clear to use this command. Each consecutive data clock writes a bit to SRAM 0 starting at Byte address BA15..0. At the end of the sector, the data will wrap and write to Byte 0. When the chip resets, if the Write Enable bit in the status register is set, the addressed sector SA15..0 will be erased and the data from SRAM 0 will be written. During this time the Busy bit will be set in the status register. The TR0 bit in the status register will be set while the SRAM SRAM is in use. The SRAM SRAM will become available while the busy bit in the status register is set. If there is an error during erase, the Error Erase bit will be set in the status register, else it will be cleared. If there is an error during write, the Error Write bit will be set in the status register, else it will be cleared.

The SRAM SRAM will be busy for the duration of $t_{EO} + t_{XS}$ to allow the sector to erase and be transferred to the sector latch before programming.

Read From SRAM

The TR0 bit in the status register must be clear to use this command. Each consecutive data clock reads a bit from SRAM 0 starting at Byte address BA15..0. At the end of the sector, the data will wrap and read from Byte 0.

Write to SRAM

The TR0 bit in the status register must be clear to use this command. Each consecutive data clock writes a bit to SRAM 0 starting at Byte address BA15..0. At the end of the sector, the data will wrap and write to Byte 0.

Compare all of Sector to SRAM

The Busy bit and the TR0 bit in the status register must be clear to use this command. After the command block has been sent, the chip will comSAre SRAM 0 to the sector address specified by SA15..0. During this time the Busy bit and TR0 bit will be set in the status register. After the chip becomes ready, the ComSAre Not Equal bit in the status register will be set if the comSAre did not SAss, else the bit will be clear.

Transfer all of Sector to SRAM

The Busy bit and the TR0 bit in the status register must be clear to use this command. After the command block has been sent, the chip will transfer the sector addressed by SA15..0 to SRAM 0. During this time the Busy bit and TR0 bit will be set in the status register.

Reset Power Detection

The Clear Power Down Bit command can be sent at any time. When this command is sent, the Power Down bit in the status register is cleared.

Set Power Detection

The Set Power Down Bit command can be sent at any time. When this command is sent, the Power Down bit in the status register is set.

Write Disable

time. When this command is sent, the Write Enable bit in the status register is cleared. If this command is sent during an array write operation, it will become effective after the current write is completed.

Write Enable

The Write Enable Main Array command can be sent at any time. When this command is sent, the Write Enable bit in the status register is set. The Main Sector Array powers up with the Write Enable bit disabled in the status register. This command must be used to Write Enable the Main Sector Array.

Read Device Information Sector

The Busy bit in the status register must be clear to use this command. The Ready Busy Word, or the status register busy bit may be used to poll for the ready condition. If the Ready Busy word is 9999h, then each consecutive data clock reads a bit in the Device Information Sector starting at the Byte Address BA15..0. At the end of the sector, the data wraps to Byte 0 and continues reading. If the Ready Busy word is 6666h, then the chip is busy and should be reset to restart a command.

Read Status Register

Each consecutive data clock will read the corresponding bit from the status register. Continuously reading bits will re-read the status register so that quick ready/busy polling can be accomplished. Holding the clock high after the 1st data bit is clocked (Ready/Busy bit) will allow real-time sampling of the SIO line as the Ready/Busy line.

Read Configuration Register

This command can be sent at any time. Each consecutive data clock will read the corresponding bit from the configuration register.

Write Configuration Register

The Busy bit in the status register must be clear to use this command. Each consecutive data clock will write the bit into the non-volatile memory of the configuration register.

Erase Sector

The Busy bit in the status register must be clear to use this command. After the command block has been sent, the chip will erase the sector addressed by SA15..0 if the Write Enable bit in the status register is set. During this time the Busy bit will be set in the status register. If the sector does not erase, the Error Erase bit in the status register will be set, else it will be clear.

Erase Block

The Busy bit in the status register must be clear to use this command. After the command block has been sent, the chip will erase the block addressed by SA15..0 if the Write Enable bit in the status register is set. During this time the Busy bit will be set in the status register. If the block does not erase, the Error Erase bit in the status register will be set, else it will be clear.

Write-Only to Sector Through SRAM

The Busy bit and TR0 bit in the status register must be clear to use this command. Each consecutive data clock writes a bit into SRAM 0 starting at Byte address BA15..0. At the end of the sector, the data will wrap and write to Byte 0. When the chip resets, if the Write Enable bit in the status register is set, the addressed sector SA15..0 will be written with the data from SRAM 0. During this time the Busy bit will be set in the status register. If the data does not verify, the Error Write bit in the status register will be set, else it will be cleared. The SRAM will be busy for the transfer time of t_{XS}.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		0 to +4.0	V
V_{IN}, V_{OUT}	Voltage Applied to Any Pin	Relative to Ground	–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to +150	°C
T_{LEAD}	Lead Temperature	Soldering 10 Seconds	+300	°C

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.

OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	3.0V	2.7	3.6	V
T_A	Ambient Temperature, Operating	Commercial	0	70	°C
		Industrial	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (PRELIMINARILY)

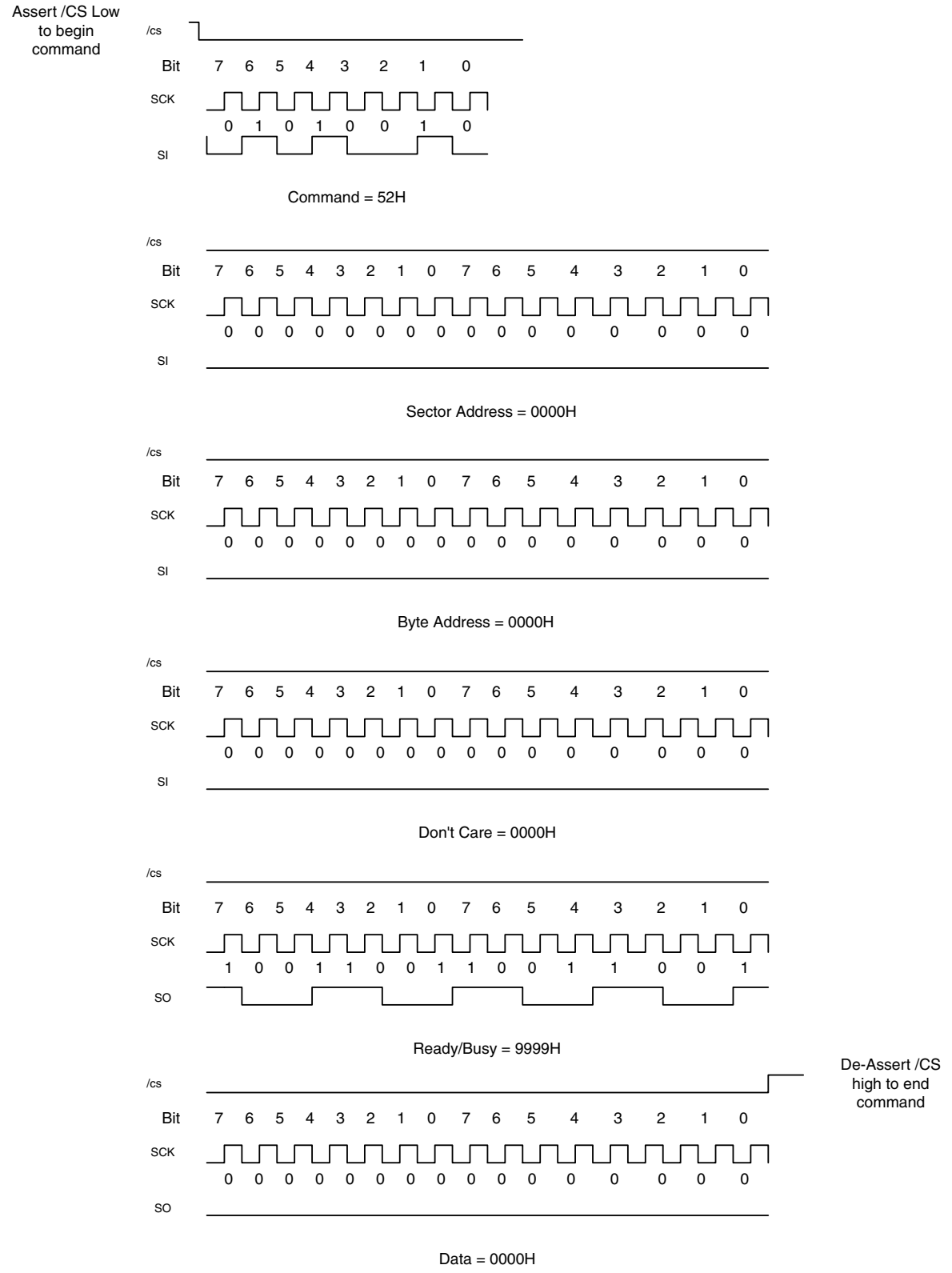
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.4	—	Vcc 0.2	V
V_{IH}	Input High Voltage		Vcc 0.7	—	Vcc +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 2.7V	—	—	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = 2.7V	Vcc 0.85	—	—	V
V_{OLC}	Output Low Voltage CMOS	V_{CC} = 2.7V, I_{OL} = 10 µA	—	—	0.15	V
V_{OHC}	Output High Voltage CMOS	V_{CC} = 2.7V, I_{OH} = –10 µA	V_{CC}–0.3	—	—	V
I_{IL}	Input Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{OL}	I/O Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Erase/Write	—	2.5	5	mA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Read	—	5	10	mA
I_{CCSB} (standby)	Standby Vcc Supply Current	CS = V_{CC}, V_{IN} = Vcc or 0 Standby	—	<3	10	µA
I_{CCSL}	Sleep Vcc Supply Current	CS = V_{CC}, V_{IN} = Vcc or 0 Sleep	—	<1	10	µA
C_{IN}	Input Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF
C_{OUT}	Output Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF

Note:
1. Tested on a sample basis or specified through design or characterization data.

AC ELECTRICAL CHARACTERISTICS (Preliminary)

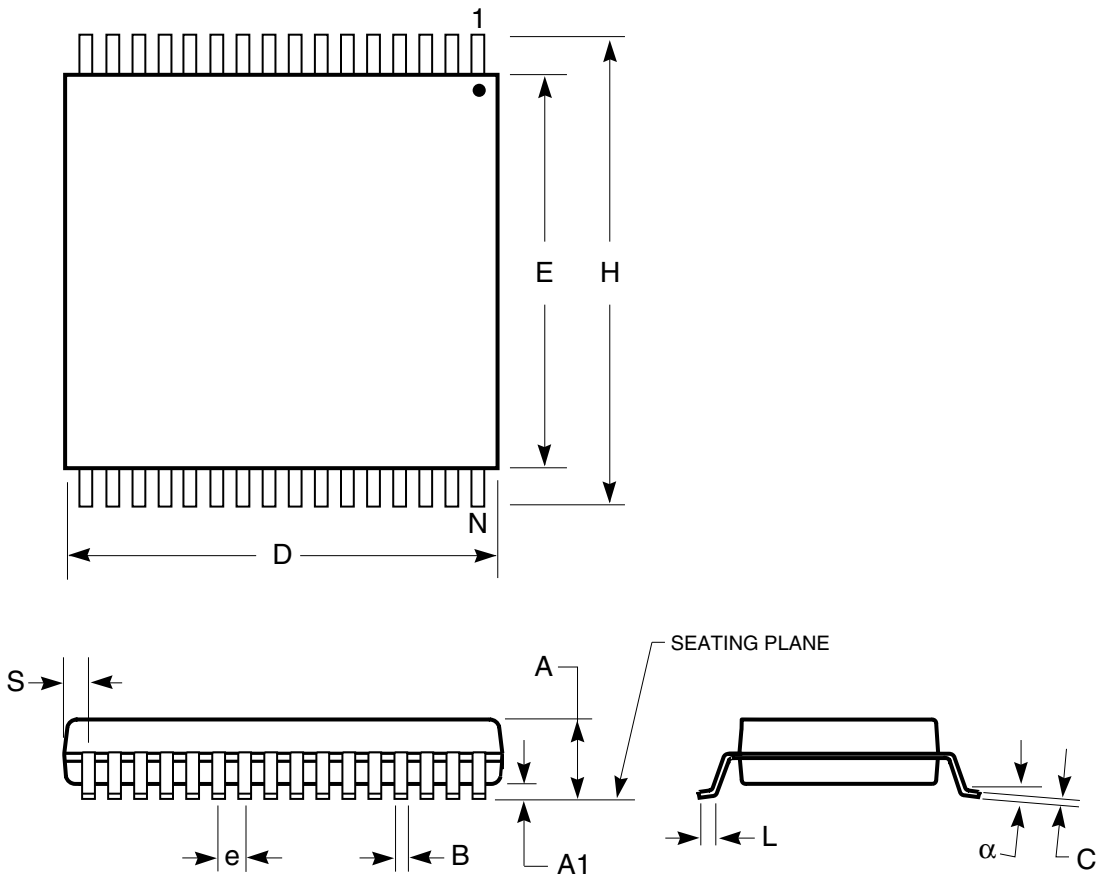
		16 MHz			
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_{CYC}	SCK Serial Clock Period With RCE=1	62	—	—	ns
	SCK Serial Clock Period With RCE=0 (1)	77	—	—	ns
t_{WH}	SCK Serial Clock High or Low Time	$t_{CYC}/2$	—	—	ns
t_{WL}					
t_{RI}	SCK Serial Clock Rise or Fall Time (2)	—	—	5	ns
t_{FI}					
t_{SU}	Data Input Setup Time to SCLK	20	—	—	ns
t_{IH}	Data Input Hold Time from SCLK	0	—	—	ns
t_V	Data Output Valid after SCLK (1,3)	—	—	25	ns
t_{LEAD}	$\overline{CS}$ Setup Time to Command	100	—	—	ns
t_{LAG}	$\overline{CS}$ Delay Time after Command	100	—	—	ns
t_{WP}	Erase/Write Program Time (4)	—	10	15	ms
	(see Write to Sector Command)				
t_{EO}	Erase Only Time	—	3	5	ms
	(see Erase Sector/Block Commands)				
t_{WO}	Write Only Time	—	7	10	ms
	(see Write Only to Sector Command)				
t_{XS}	Transfer Sector	—	—	100	µs
	(see Transfer All Command)				
t_{HD}	SCK Setup Time to $\overline{HOLD}$	10	—	—	ns
t_{CD}	SCK Hold Time from $\overline{HOLD}$	30	—	—	ns
t_{CS}	$\overline{CS}$ Deselect Time	160	—	—	ns
t_{RB}	READY / BUSY Valid Time	160	—	—	ns
t_{DIS}	Data Output Disable Time	—	—	160	ns
t_{OH}	Data Output Hold Time After SCK	0	—	—	ns

Notes:
1. To achieve maximum clock performance, the read clock edge will need to be set for rising edge operation in the configuration register (RCE=1).
2. Test points are 10% and 90% points for rise/fall times. All others timings are measured at 50% point.
3. With 30 pF (16 MHz) load SO to GND.
4. Maximum program time for 99% of sectors, <1% may require 4x this value.



SPI Clock Diagram for Read Command

Plastic TSOP - 32-pins
Package Code: T (Type I)



Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.005
B	0.17	0.27	0.007	0.009
C	0.10	0.21	0.004	0.008
D	7.90	8.10	0.308	0.316
E	18.30	18.50	0.714	0.722
H	19.80	20.20	0.772	0.788
e	0.50 BSC		0.020 BSC	
L	0.50	0.70	0.016	0.024
a	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PRELIMINARY DESIGNATION

The “Preliminary” designation on an *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

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(a) the risk of injury or damage has been minimized;

(b) the user assumes all such risks; and

(c) potential liability of *NexFlash* is adequately protected under the circumstances.

2711 North First Street • San Jose, CA 95134
Ph: 408-907-3600 • Fx: 408-907-3601 • sales@nexflash.com
www.nexflash.com