NROM4EE

SAIFUN PROPRIETARY

4Mbit (512K x 8) PARALLEL EEPROM

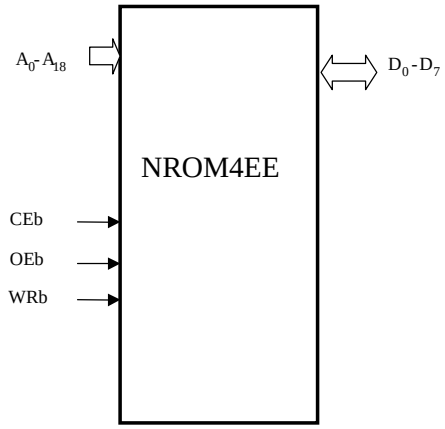
2.7 Volt Low Power EEPROM With Basic Flash Functionality

GENERAL DESCRIPTION

The NROM4EE is a 4Mbits high performance, low power parallel EEPROM device that supports also basic Flash functionality. The device is typically accessed like SRAM for both read and write operations without the need for external components. It is organized as 512K words of 8bits (Byte). The device has on chip latch for data and address and thus it frees the system for other operation while writing a byte. The device contains also a 128-byte page register to allow writing of up to 128 bytes simultaneously to support page write.

Sector Erase, provides the basic Flash functionality. This maximizes user's flexibility by enabling user decision on which sector will serve EEPROM functionality and which Flash.

LOGIC DIAGRAM



FEATURES

- Saifun NROM™ Flash cell
- 4 Mbit parallel EEPROM
  - 512K bytes (X8)
- Fast Read Access Time - 90nSec
- Byte (real) and Page Write Operation
  - Up to 128 bytes of data
  - Scattered operation
- Fast Write Cycle Time
  - Byte operation < 3mSec (typical)
  - Page operation < 10mSec (typical)
- Single Voltage operation
  - 2.7-3.6V
  - VPP test pad for fast sort testing
- Low Power Dissipation
  - Active current (R /W) - 7/20mA (typ.)
  - Active power - 65mW (typ.)
- Automatic sleep mode
  - Standby Current - 20µA
- Sector Erase Architecture
- Hardware data protection
- Software data protection (SDP)
- DATA polling for end of write detection
  - DATA#
  - Toggle bit
- User extra 256 Bytes, protected from sector and chip erase.
- Manufacturer 256 extra Bytes, with protected access.
- Endurance: 100,000 cycles per Byte
- Data Retention: 10 years
- Compatible to JEDEC
  - Standard commands as E^2PROM

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DEVICE OPERATION

READ

The NROM4EE is accessed like static RAM. Read is performed when CE# and OE# are activated. The data stored at the memory location determined by the address pins is put also on the Data pins. The data bus is at high-Z when either CE# or OE# are inactive.

WRITE

The NROM4EE is accessed like static RAM. Write is performed when CE# and WE# are activated and OE# is inactive. The accessed address is latch at the falling edge of CE# or WE#, whichever last activated and the data is latch at the rising edge of either CE# or WE#, whichever come first. Both the address and data are stored internally and enable the system to continue its operation. Once the write operation started, a read operation will effectively be a polling operation and address is ignored.

PAGE WRITE

The page write feature allows 1 to 128 bytes of data to be consecutively written to the memory before starting of internal programming cycle. Page write is useful during DMA operation where data is fetched from another device into the memory as continues burst. The page write operation is initiated in the same manner as a byte write. The first byte defines the start address inside a page (A6-A0) followed by 1 to 127 additional bytes, each successive byte must be written within 100µS (Tblc). Last byte written defines the Page address (A18-A7). If Tblc limit is exceeded, the NROM4EE will cease accepting data and start the internal page programming. All bytes during a page operation must reside on the same page as defined in A18-A7 address pins. A6-A0 inputs specify which bytes within the page are to be written.

The bytes may be loaded in scattered order but within the same page address. Any change of page address within burst of byte writes will cause abortion of page command and ERROR flag will be turned on.

DATA POLLING

While the NROM4EE is processing write operation, D7 outputs the complement data of the written byte. The first read with the true data indicates the write operation completion.

TOGGLE BIT

In addition to data polling, while the NROM4EE is processing write operation, D6 is toggled from read to read operation. A first read with non-complementary data indicates the write operation completion.

DATA PROTECTION

The NROM4EE provides extra protection against false write operation. It includes both hardware and software features to cover all inadvertent write.

Hardware Data Protection

Power up/down detection: VCC sense does not allow write operation to occur if level is fail below 2.2V for more then 100uS.

Power on delay: at power on the NROM4EE has an internal timer that prevents write operation 5mS after power exceeds the right level.

Noise protection: A WE# pulse of less than 10nS will be ignored.

Software Data Protection (SDP)

When the device is protected by SDP it means that 1 cycle writes will be ignored and only specific command pattern will be accepted. The SDP feature may be enabled or disabled by the user. SDP is enabled when the host issues a series of three write commands. Once set, any write cycle must be preceded by a write enable command sequence consisting of 3 bytes. The protection (SDP) is disabled only after a 6 bytes protection disable command sequence is provided. SDP disable requires Tblc before enabling new write command. SDP state is stored in VL flag thus will return to its default value after power down transitions.

USER EXTRA SPACE

A space of 256 bytes is available to the user for device identification. Accessing the user space is done through super address only.

SECTOR ERASE

A sector erase command can be issued to the NROM4EE. This command will erase the sector associated with the 6 most significant address bits.

CHIP ERASE

A full chip erase command can be issued to the NROM4EE. This command will erase the entire array but the user extra space. The command is built from a sequence of 6 writes.

ERROR STATE

When the device is entered to ERROR state the user will be notified by flags status. Only the user can command the chip to exit ERROR state and go back to read mode. When the host wants to exit ERROR State, it will produce a Read/Reset command sequence and the device will return to read.

BLOCK DIAGRAM

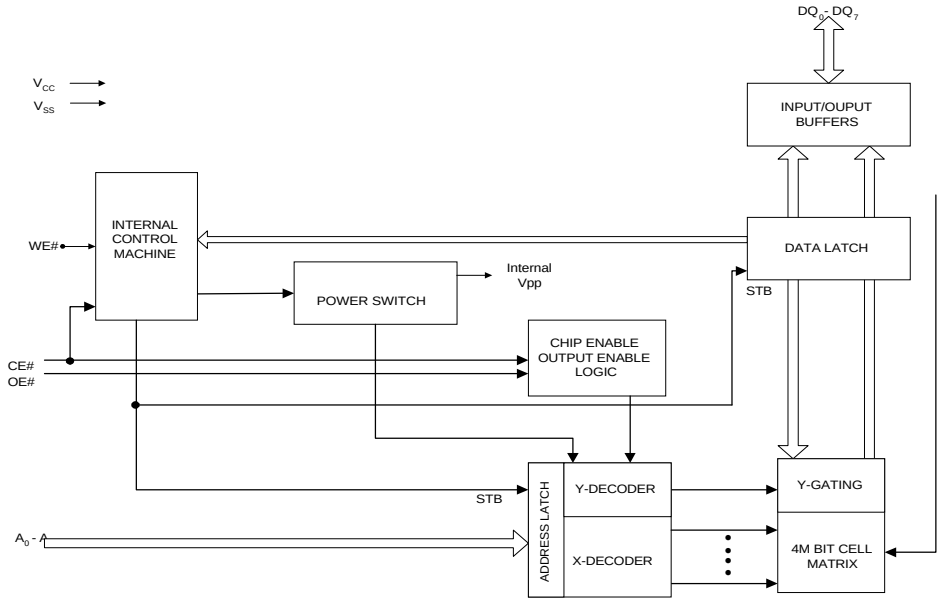


Figure 1 - NROM4EE Block Diagram

OPERATING RANGE

Range	Temperature	Vcc Tolerance
Commercial	0°C to + 70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
All Input Voltages Except A9 with Respect to Ground (Note 2)	-0.5V to V_{CC} +0.5V
V_{CC} Supply Voltage with Respect to Ground (Note 2)	-0.5V to 4.0V
ESD Protection	>4000V
All Output Voltages With Respect to Ground (Note 2)	V_{CC} + 0.5V to GND -0.5V
A_9 Input Voltage	-0.5V to +13.5V

Note 1:
Stresses above theses listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0 V for periods less than 20ns.

CONNECTION DIAGRAM

32 PLCC package type (conform to JEDEC Standard)

PIN NAMES

V_{CC}	Power Supply for Device Operation
A0 - A18	Address Inputs
CE#	Chip Enable (Active low)
OE#	Output Enable (Active low)
WE#	Write Enable (Active low)
D0-D7	Inputs/Outputs

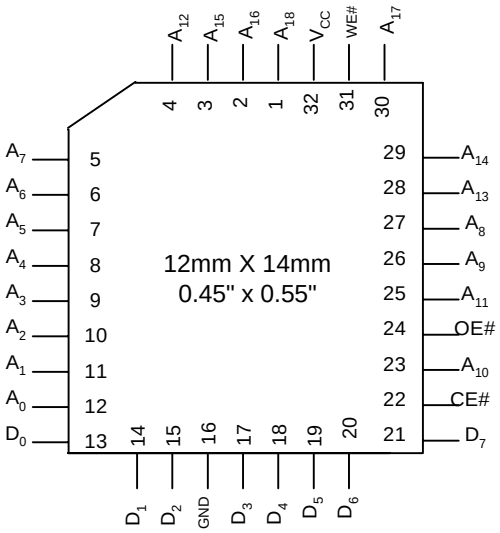


Figure 2 - PLCC Pin Configuration – Top View

DC CHARACTERISTICS COMMERCIAL TEMPERATURE

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
V_{IL}	Input Low Level		-0.5		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA, V_{CC}=$V_{CC\ MIN}$			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA, V_{CC}=$V_{CC\ MIN}$	V_{CC} - 0.4			V
V_{ID}	A_9 Super Address Voltage		11.50		12.50	V
I_{ID}	A_9 Super Address Current	A_9 = V_{ID}			200	µA
I_{SB1}	V_{CC} Standby Current (CMOS)	CE# = V_{CC} ± 0.3V (all other pins = Hi) V_{CC} = $V_{CC\ MAX}$			20	µA
I_{CC1}	V_{CC} Active Current (Read)	CE# = V_{IL} WE# = OE# = V_{IH} F = 5Mhz V_{CC} = $V_{CC\ MAX}$		7	10	mA
I_{CC2}	V_{CC} Active Current (Write)	CE# = V_{IL} WE# = OE# = V_{IH} F = 330Hz (3mS write time) V_{CC} = $V_{CC\ MAX}$		15	25	mA
I_{CC3}	V_{CC} Program only Current (no erase phase)	CE# = V_{IL} WE# = OE# = $V_{IH}$$V_{CC}$ = $V_{CC\ MAX}$		15	25	mA
I_{L1}	Input Leakage Current	V_{IN} = V_{CC} or GND, V_{CC} = V_{CC} max			±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND, V_{CC} = V_{CC} max			+1	µA
I_{L1T}	A_9 Input Leakage Current of super address inputs	V_{IN} = V_{ID}, V_{CC} = V_{CC} max			35	µA

CAPACITANCE: T_A = +25°C, F = 1 MHz

Symbol	Parameter	Typ.	Max	Units	Conditions
C_{IN}	Input Capacitance	6	15	pF	V_{IN}=0v
C_{OUT}	I/0 Capacitance	10	15	pF	V_{OUT}=0v

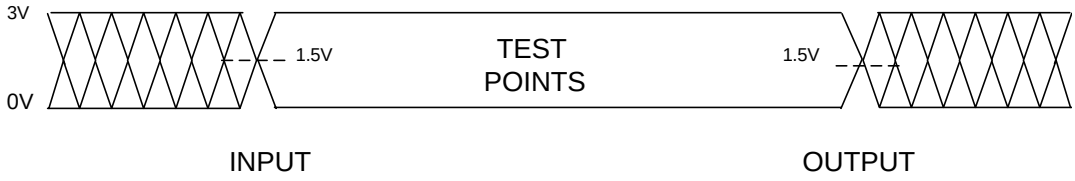
AC TEST CONDITIONS

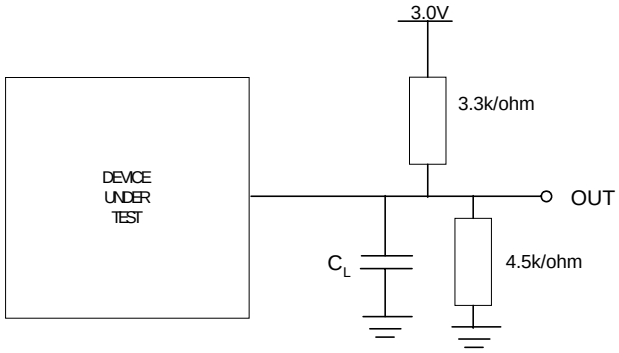
Test Condition		Unit
Output Load	1 TTL Gate (4mA load)	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Time (10% - 90%)	5	ns
Input Pulse Levels	0 – 3V	V
Input Timing Measurement Reference Levels	1.5V	V
Output Timing Measurement Reference Levels	1.5V	V

AC MEASUREMENT CONDITIONS

For 90 ns (1) VCC = 3V

Input Rise and Fall Times = 5ns
Input Pulse Voltage: 0v to 3v
Input and Output Timing Ref. Voltage: 1.5v





C_L=30

Figure 3: Device Under Test

NOTE: The floating Voltage is tuned to 1.5v

AC READ CHARACTERISTICS OVER OPERATING RANGE

Symbol		Parameter	Time (3)		Units
JEDEC	SID		Min	Max	
t_{AVAV}	T_{RC}	Read Cycle Time	90		ns
t_{ELQV}	T_{CE}	CE# Access Time		90	
t_{AVQV}	T_{ACC}	Address Access Time		90	
t_{GLQV}	T_{OE}	OE# Access Time		30	
t_{ELQX}	T_{LZ}	CE# to Active Output	0		
t_{EHQZ}	T_{DF}	Chip Disable to Output in High Z (Note 4)		20	
t_{GLQX}	T_{OLZ}	OE# to Active Output	0		
t_{GHQZ}	T_{ODF}	Output Disable to Output in High Z (Note 4)		20	
t_{AXQX}	T_{OH}	Output Hold from Addresses, CE# or OE#, change (Note 4)	0		
t_{WHGL}	T_{WO}	WE# Disable to OE# assertion	15		
t_{VCS}	T_{VCS}	V_{cc} Setup Time to Valid Read (Note 4)		100	µs

Note 3: 30pF load
Note 4: Guaranteed by design, not tested.

AC WAVEFORMS FOR READ OPERATIONS

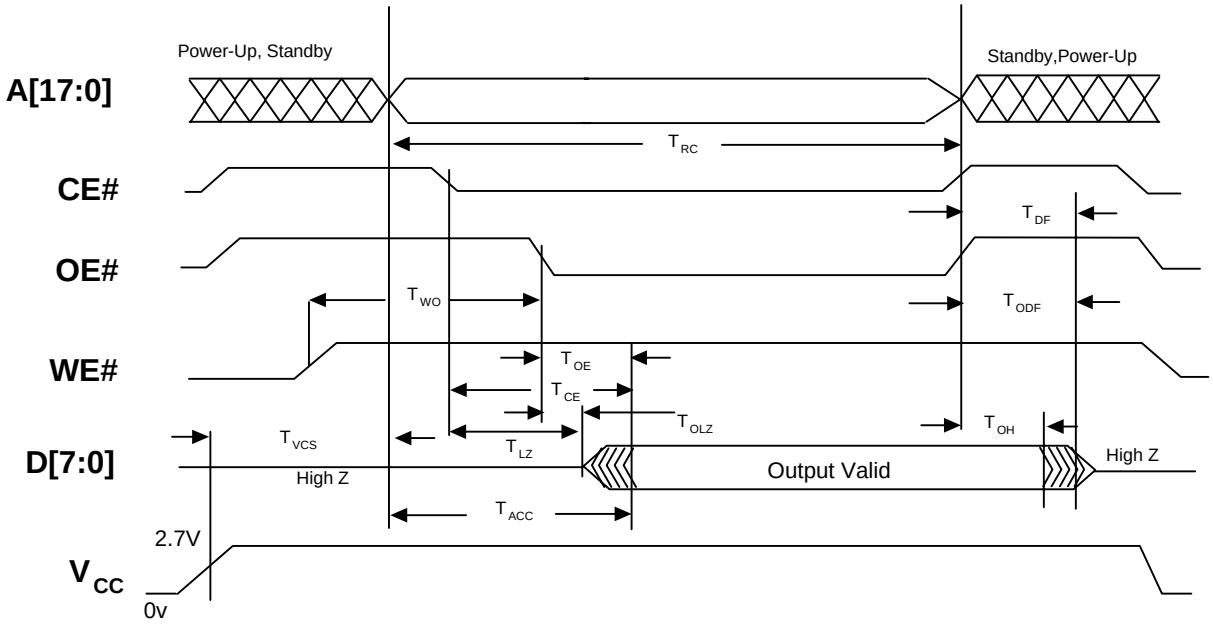


Figure 4: AC Waveform for Read Operation

AC WAVEFORMS FOR WRITE/COMMAND OPERATIONS

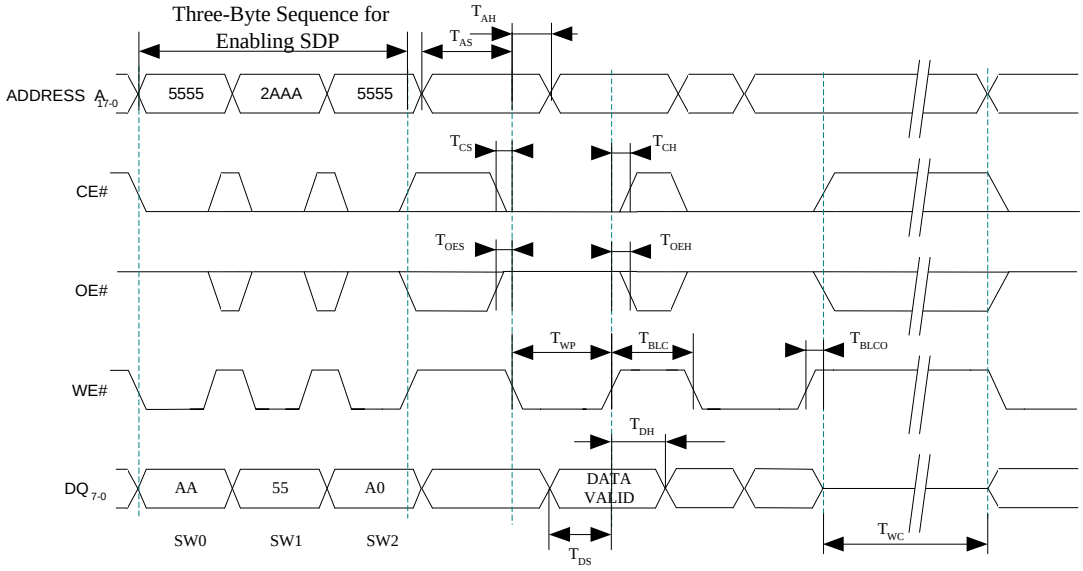
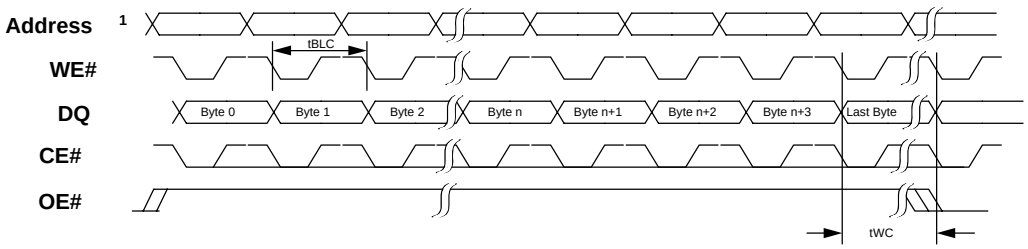


Figure 5: AC Waveforms for Write Operations

AC CHARACTERISTICS - WRITE OPERATIONS

Symbol		Parameter	Time			Units
JEDEC	SID		Min	Typ	Max	
T_{BLC}	T_{BLC}	Byte Load Time	0.05		100	µs
T_{BLCO}	T_{BLCO}	Last Byte Command Load to Start of Operation	150			µs
t_{AVWL}	T_{AS}	Address Setup Time	0			ns
t_{WLAX}	T_{AH}	Address Hold Time	35			ns
t_{DVWH}	T_{DS}	Data Setup Time	25			ns
T_{WHDX}	T_{DH}	Data Hold Time	0			ns
	T_{OES}	OE# to WE# setup time	0			ns
	T_{OEH}	OE# to WE # Hold Time	0			ns
t_{ELWL}	t_{CS}	WE# to CE# Setup Time	0			ns
t_{WHEH}	t_{CH}	WE# to CE# Hold Time	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width	45			ns
t_{WHWH1}		Duration of BYTE Programming Operation		3	10	ms
	t_{WC}	Duration of by the Page Programming Operation		10	15	ms
	T_{VCSW}	V_{cc} Setup Time to Valid Write			5	ms

AC WAVEFORMS FOR PAGE WRITE OPERATION



1. Addresses A[18:7] within the page write operation should be the same, otherwise unknown operation might occur

Figure 6: AC Waveforms for Page Write Operation

OPERATION MODES

The NROM4EE memory operates in 2 basic modes: the Bus operation that used as in-system operation by external host and Hardware operation which basically used in common programmers or testers.

BUS OPERATION

Mode	CE#	OE#	WE#	D	Address	Power
Read	Vil	Vil	Vih	Dout	Ain	Active
Write / Command	Vil	Vih	Vil	Din	Ain	Active
Standby/Write Inhibit	Vih	X	X	High Z	X	Standby
Write Inhibit	Vil	Vil	Vil	High Z / Dout (1)	X	Active
Write Inhibit	Vil	Vih	Vih	High Z	X	Active

(1) During this mode OE# is masking WE# and data is driven out, but if OE# is negated before WE#. A write cycle will be generated with unexpected behavior

X = Don't care.

HARDWARE OPERATION

Mode	CE#	OE#	WE#	D	Address
Product ID read (1)	Vil	Vil	Vih	Manufacturer ID Device ID	A=00000,H A9=Vid A=00001H, A9=Vid
User Extra Memory read	Vil	Vil	Vih	Dout	A=7FF(1xxx,xxxx) H A9=Vid (1)
User Extra Memory write	Vil	Vih	Vil	Din	A=7FF(1xxx,xxxx)H A9=Vid (1)

(1) Vid = 12V

X = Don't Care

COMMAND SEQUENCES AND WRITE CYCLES

Command sequence is a series of write accesses with a period time of less then Tblc (100uS) between successive writes, once Tblc limit is exceeded the command is locked and internal operation is started. Any write access during internal operation execution will be ignored, any read access will results with flags value rather then array data.

Any command sequence that is not aligning to the above rules will be declared as illegal command and will be ignored. Only Tblc period time can close a command sequence and start a new one, i.e. a series of illegal writes can ended when Tblc will expire and the device will start a new command sequence.

COMMAND CYCLES EXAMPLES

The following will describe some command execution examples in details:

Write cycles in SDP disable

- Tblc followed by Write followed by Tblc ; write access is performed
- Write followed by new Write in the same page (not part of legal command); access is performed
- Stream of writes followed by Tblc (same page); access is performed

Write cycles in SDP enable

- Write followed by Tblc; access is ignored
- Stream of writes followed by Tblc ; access is ignored

The following tables will describe the available commands the user can write into the device. The following table will describe the array commands while the next one will take care for EM space commands. EM accesses are differing from regular accesses by using a super address on last write of the command to protect it from write cycles during normal operation, that's why SDP flag is not necessary and is ignored in this case.

ARRAY COMMANDS' SEQUENSES

Command Sequence (4)		# of Cycles	1'st Bus Cycle		2'nd Bus Cycle		3'rd Bus Cycle		4'th Bus Cycle		5'th Bus Cycle		6'th Bus Cycle		Comments
			Add(1)	Data	Add(1)	Data	Add(1)	Data	Add(1)	Data	Add(1)	Data	Add(1)	Data	
Read		1	Add	Dout											
Write (3,8)		1	Add	Din											Need 150uSec Idle between 2 writes
Read /Reset		3	5555H	AAH	2AAAH	55H	5555H	F0H							
Read /Reset		1	xxxH	F0H											Will be active only when SDP is enabled Usually clear ERROR flag
Chip erase (8)		6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H	
S/W Data Protect SDP (8)	SDP Enable (10)	3	5555H	AAH	2AAAH	55H	5555H	A0H							
	Write Enable (6)	4	5555H	AAH	2AAAH	55H	5555H	A0H	Add	Din					
	SDP Disable (10)	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H	
Sector erase (8)		6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA(2)	30H	
Auto select mode (8)	ManID	4	5555H	AAH	2AAAH	55H	5555H	90H	00H(7)	ManufID (9)					4'th cycle is read cycle need Read/Reset command to exit
	DeviceID	4	5555H	AAH	2AAAH	55H	5555H	90H	02H(7)	DevID					4'th cycle is read cycle need Read/Reset command to exit

NOTES

(1) A_{14-0} are Hex Format. A_{18-15} are don't care

(2) SA is the sector address placed on pins A_{18-14} for array sectors as described in "Sector address map" table.

(3) Valid only if S/W data protection is disabled.

(4) Command sequence is not sustained if the product is powered off.

(5) Not Used

(6) Used as write command when SDP is enabled. If SDP is disabled, it will be re-activated after write completion.

(7) A_{18-8} are don't care.

(8) t_{BLC} is defined as the write inactive time between 2 consecutive writes. To assure multi write command execution, write inactive should not exceed 100uSec. This implies that any single byte write must be followed with 150ns time out to differentiate between byte write and command sequence.

(9) Not Used

(10) SDP will be enabled T_{BLC} after end of "SDP enable" command. SDP is latched after Power up, changes in SDP value are valid till power down

EXTRA MEMORY COMMANDS' SEQUENCES

Command Sequence (4)		# of Cycles	1'st Bus Cycle		2'nd Bus Cycle		3'rd Bus Cycle		4'th Bus Cycle		5'th Bus Cycle		6'th Bus Cycle		Comments
Read	A9=Vid	1	Add A9=Vid	Dout											See table 8 for EM address map
Write (3,8)	A9=Vid	1	Add A9=Vid	Din											User mode
S/W Data Protect SDP (5,8) Write Enable (6)	A9=Vid	4	5555H	AAH	2AAAH	55H	5555H	A0H	Add A9=Vid	Din					User mode

NOTES

(1) A_{14-0} are Hex Format. A_{18-15} are don't care

(2) Not Used.

(3) In EM access SDP is not required and will be ignored, so write will be always valid.

(4) Command sequence is not sustained if the product is powered off.

(5) SDP protection is bypassed during EM access so SDP command sequence is not really needed but nevertheless it will be accepted if written to the device.

(6) Used as write command when SDP is enabled. If SDP is disabled, it will be re-activated after write completion.

(7) Not Used

(8) t_{BLC} is defined as the write inactive time between 2 consecutive writes .To assure multi write command execution; write inactive should not exceed 100uSec.

DATA BUS POLLING DURING EMBEDDED OPERATION (FLAGS)

DATA POLLING - DQ7

While the NROM4EE executes embedded command. An attempt to read the device (address = don't care) will produce the compliment data of D[7] on DQ7. Once completed, an attempt to read the device (with original address) will produce the valid expected data on DQ7. The data-polling feature is valid after the negation of WE# of the last write access of the command sequence.

TOGGLE BIT - DQ6

While the NROM4EE executes embedded command. Each attempt to read the device (address = don't care) will result in DQ6 toggling between the logic levels "1" and "0". Once completed, DQ6 will stop toggling and an attempt to read the device (with any address) will produce valid data on DQ6. The toggle bit feature is valid after the negation of WE# of the last write access of the command sequence.

FAIL TO WRITE - DQ5

DQ5 will indicate if the program or erase failed the operation (according to design specified limits). Under this condition, DQ5 will provide "1". The part will be locked in this state until Read/Reaset command will be issued.

INTERNAL PHASE FAILURE - DQ4

DQ4 will indicate in which phase (program OR erase) the algorithm failed, "0" in DQ4 indicate that the programming failed while "1" is indicating a failure in erase.

SECTOR ERASE TIMER - DQ3

The NROM4EE is not supporting a pipeline operation of sector erase, therefore this flag will be extracted as "1" during sector erase command.

FLAGS VALUES

Embedded cycle	Internal operation	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2-0
In progress	Erase part in Write cycle	DQ7#	Toggle	0	1	1	0 - RFU
	Program part in Write cycle	DQ7#	Toggle	0	0	1	0 - RFU
	Refresh part in Write cycle	DQ7#	Toggle	0	0	1	0 - RFU
	Sec/chip erase	0	Toggle	0	1	1	0 - RFU
Finish	Write cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ1-0
	Sec/Chip erase	1	1	1	1	1	11
Write failure	Erase part in Write cycle	DQ7#	Toggle	1	1	1	0 - RFU
	Program part in Write cycle	DQ7#	Toggle	1	0	1	0 - RFU
	Refresh part in Write cycle	DQ7#	Toggle	1	0	1	0 - RFU
	Sec/chip erase	0	Toggle	1	1	1	0 - RFU

* RFU - Reserved for Future Use.

ADDRESS MAPPING

SECTOR ADDRESS MAP

Sector #	Address (A_{18-14})
0	00000B
1	00001B
2	00010B
3	00011B
4	00100B
5	00101B
6	00110B
7	00111B
8	01000B
9	01001B
10	01010B
11	01011B
12	01100B
13	01101B
14	01110B
15	01111B
16	10000B
17	10001B
18	10010B
19	10011B
20	10100B
21	10101B
22	10110B
23	10111B
24	11000B
25	11001B
26	11010B
27	11011B
28	11100B
28	11101B
30	11110B
31	11111B
EM sectors	**Address (A9=Vid)**

*** SECTOR SIZE = 16KBYTES**

MEMORY ADDRESS MAP

Access		Address
Memory access		XXX-XXXX-XXXX-XXXX-XXXX[1]
Extra memory access (UEM+ID)		XXX-XXXX-XXH1-XXXX-XXXX[2]
	Manufacturer ID	000-0000-00H0-0000-0000[2]
	Device ID	000-0000-00H0-0000-0001[2]
	User Extra Memory (UEM)	111-1111-11H1-XXXX-XXXX[2]

[1] X = low voltages only (Vil, Vih)

[2] H=VID; A9 driven with VID (12V) will identify EM space