NCP4561

Ultra Low–Noise Low Dropout Voltage Regulator with 1.0 V ON/OFF Control

The NCP4561 is a Low DropOut (LDO) regulator featuring excellent noise performances. Thanks to its innovative concept, the circuit reaches an incredible 40 μVRMS noise level ***without*** an external bypass capacitor. Housed in a small SOT–23 5 leads–like package, it represents the ideal designer's choice when space and noise are at premium.

The absence of external bandgap capacitor unleashes the response time to a wake–up signal and makes it stay within 40 μs (in repetitive mode), pushing the NCP4561 as a natural candidate in portable applications.

The NCP4561 also hosts a novel architecture which prevents excessive undershoots when the regulator is the seat of fast transient bursts, as in any bursting systems.

Finally, with a static line regulation better than –75 dB, it naturally shields the downstream electronics against choppy lines.

Features

- Ultra Low–Noise: 150 nV/√Hz @ 100 Hz, 40 μVRMS 100 Hz – 100 kHz Typical, Iout = 60 mA, C_o = 1.0 μF
- Fast Response Time from OFF to ON: 40 μs Typical at a 200 Hz Repetition Rate
- Ready for 1.0 V Platforms: ON with a 900 mV High Level
- Nominal Output Current of 80 mA with a 100 mA Peak Capability
- Typical Dropout of 90 mV @ 30 mA, 160 mV @ 80 mA
- Ripple Rejection: 70 dB @ 1.0 kHz
- 1.5% Output Precision @ 25°C
- Thermal Shutdown

Applications

- Noise Sensitive Circuits: VCOs RF Stages, etc.
- Bursting Systems (TDMA Phones)
- All Battery Operated Devices

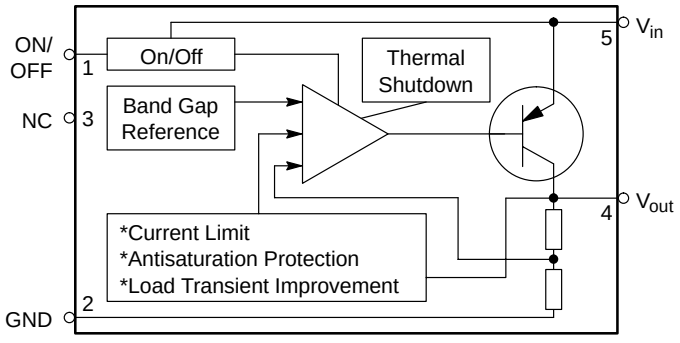

Figure 1. Simplified Block Diagram

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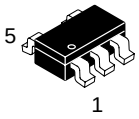
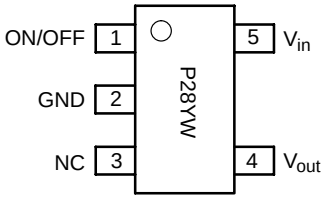


TSOP–5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



(Top View)

P28 = Device Code
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Voltge Output*	Shipping
NCP4561SNT1–28	2.8 V	3000/Tape & Reel

* Contact your ON Semiconductor sales representative for other output voltage values.

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PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Function	Description
1	ON/OFF	Shuts or wakes–up the IC	A 900 mV level on this pin is sufficient to start the IC. A 150 mV shuts it down.
2	GND	The IC's ground	
3	NC	None	It makes no arm to connect the pin to a known potential, like in a pin–to–pin replacement case.
4	V_{out}	Delivers the output voltage	This pin requires a 1.0 μF output capacitor to be stable.
5	V_{in}	Powers the IC	A positive voltage up to 12 V can be applied upon this pin.

MAXIMUM RATINGS

Rating	Pin #	Symbol	Value Min	Value Max	Unit
Power Supply Voltage	5	V_{in}	–	12	V
ESD Capability, HBM Model	All Pins		–	1.0	kV
ESD Capability, Machine Model	All Pins		–	200	V
Maximum Power Dissipation NW Suffix, Plastic Package Thermal Resistance Junction–to–Air		P_D $R_{\theta J-A}$	– –	Internally Limited 210	W °C/W
Operating Ambient Temperature Maximum Junction Temperature (Note 1.) Maximum Operating Junction Temperature (Note 2.)		T_A T_{Jmax} T_J	– – –	–40 to +85 150 125	°C
Storage Temperature Range		T_{stg}	–	–60 to +150	°C

ELECTRICAL CHARACTERISTICS

(For Typical Values T_A = 25°C, for Min/Max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Logic Control Specifications						
Input Voltage Range	1	$V_{ON/\overline{OFF}}$	0	–	V_{in}	V
ON/$\overline{OFF}$ Input Resistance	1	$R_{ON/\overline{OFF}}$	–	250	–	kΩ
ON/OFF Control Voltages (Note 3.) Logic Zero, OFF State, I_O = 50 mA Logic One, ON State, I_O = 50 mA	1	$V_{ON/\overline{OFF}}$	 – 900	 – –	 150 –	mV
Currents Parameters						
Current Consumption in OFF State OFF Mode Current: $V_{in} = V_{out}$ + 1.0 V, I_O = 0, V_{OFF} = 150 mV		IQ_{OFF}	–	0.1	2.0	μA
Current Consumption in ON State ON Mode Current: $V_{in} = V_{out}$ + 1.0 V, I_O = 0, V_{ON} = 3.5 V		IQ_{ON}	–	180	–	μA
Current Consumption in ON State, ON Mode Saturation Current: $V_{in} = V_{out}$ – 0.5 V, No Output Load		IQ_{SAT}	–	800	–	μA
Current Limit $V_{in} = Vout_{nom}$ + 1.0 V, Output is brought to $Vout_{nom}$ – 0.3 V		I_{MAX}	100	180	–	mA

1. Internally Limited by Shutdown.
2. Specifications are guaranteed below this value.
3. Voltage Slope should be Greater than 2.0 mV/μs.

ELECTRICAL CHARACTERISTICS (continued)
(For Typical Values T_A = 25°C, for Min/Max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Output Voltages						
V_{out} + 1.0 V < V_{in} < 6.0 V, T_A = 25°C, 1.0 mA < I_{out} < 80 mA	4	V_{out}	2.758	2.8	2.842	V
V_{out} + 1.0 V < V_{in} < 6.0 V, T_A = –40°C to +85°C, 1.0 mA < I_{out} < 80 mA	4	V_{out}	2.716	2.8	2.884	V
Line and Load Regulation, Dropout Voltages						
Line Regulation V_{out} + 1.0 V < V_{in} < 12 V, I_{out} = 80 mA	4/5	Reg_{line}	–	–	20	mV
Load Regulation V_{in} = V_{out} + 1.0 V, C_{out} = 1.0 μF, I_{out} = 1.0 to 80 mA	4	Reg_{load}	–	–	40	mV
Dropout Voltage (Note 4.) I_{out} = 30 mA I_{out} = 60 mA I_{out} = 80 mA	 4 4 4	 V_{in}–V_{out} V_{in}–V_{out} V_{in}–V_{out}	 – – –	 90 140 160	 150 200 250	mV
Dynamic Parameters						
Ripple Rejection V_{in} = V_{out} + 1.0 V + 1.0 kHz 100 mVpp Sinusoidal Signal	4/5	Ripple	–	–70	–	dB
Output Noise Density @ 1.0 kHz	4		–	150	–	nV/√Hz
RMS Output Noise Voltage C_{out} = 1.0 μF, I_{out} = 50 mA, F = 100 Hz to 1.0 MHz	4	Noise	–	35	–	μV
Output Rise Time C_{out} = 1.0 μF, I_{out} = 50 mA, 10% of Rising ON Signal to 90% of Nominal V_{out}	4	t_{rise}	–	40	–	μs
Thermal Shutdown						
Thermal Shutdown			–	–	125	°C

4. V_{out} is brought to V_{out} – 100 mV.

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant chip temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential value). The dropout level is affected by the chip temperature, load current and minimum input supply requirements.

Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output current are kept constant during the measurement. Results are expressed in μVRMS.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specs.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected. One usually distinguishes *static line regulation* or *DC line regulation* (a DC step in the input voltage generates a corresponding step in the output voltage) from *ripple rejection* or *audio susceptibility* where the input is combined with a frequency generator to sweep from a few hertz up to a defined boundary while the output amplitude is monitored.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 125°C, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package power dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient temperature, it is possible to calculate the maximum power dissipation and thus the maximum available output current.

TYPICAL CHARACTERISTICS

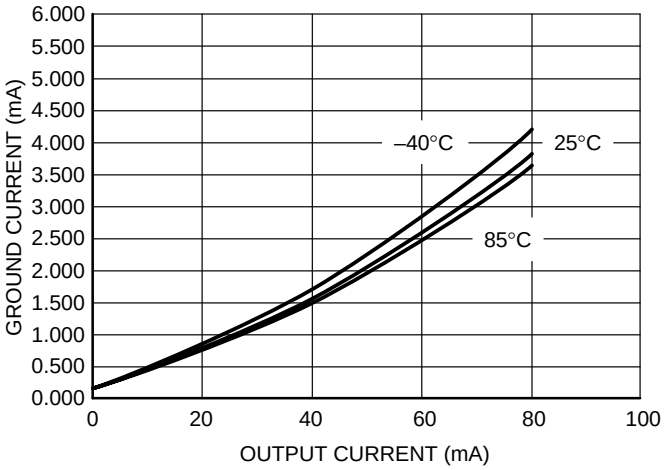


Figure 2. Ground Current vs. Output Current

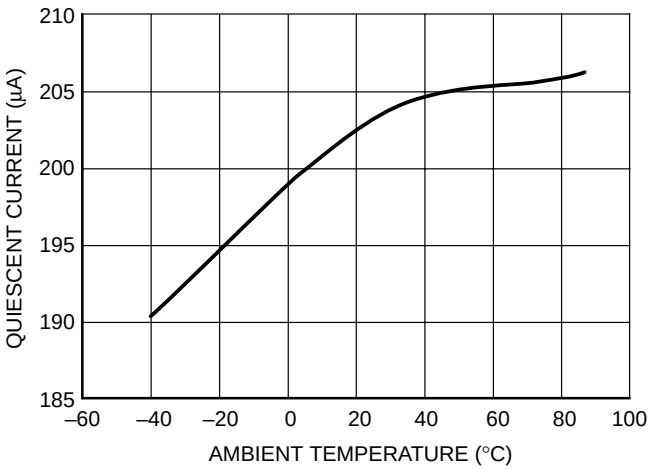


Figure 3. Quiescent Current vs. Temperature

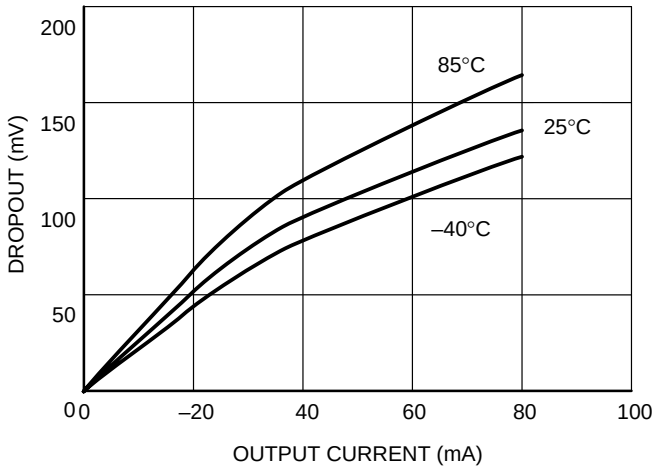


Figure 4. Dropout vs. Output Current

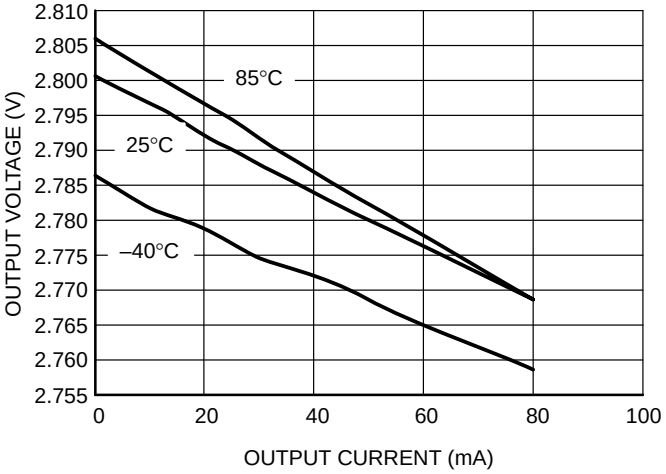


Figure 5. Output Voltage vs. Output Current

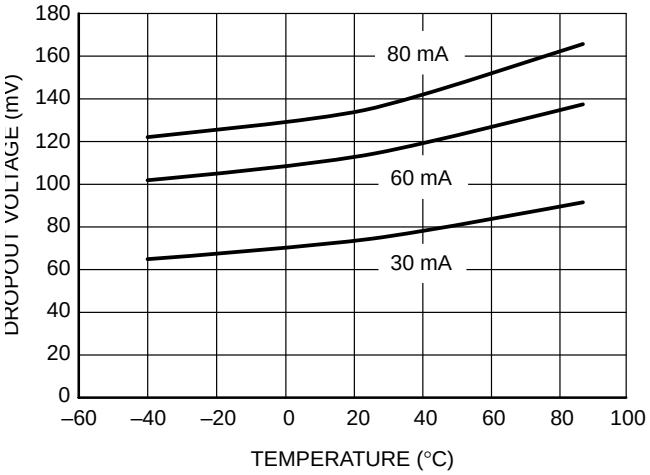


Figure 6. Dropout Voltage vs. Temperature

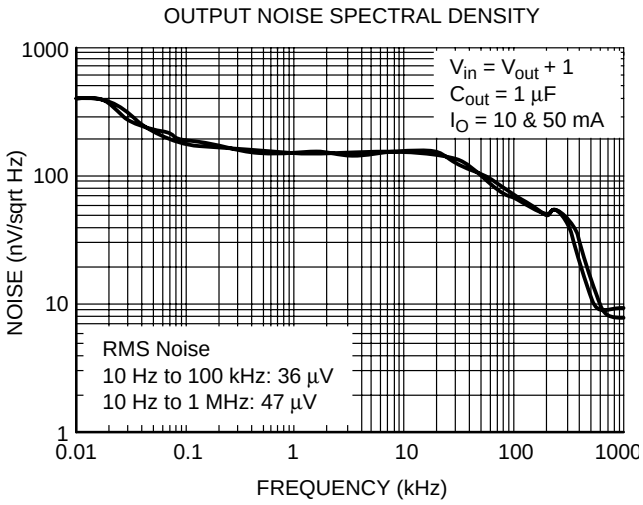


Figure 7. Typical Noise Density Performance

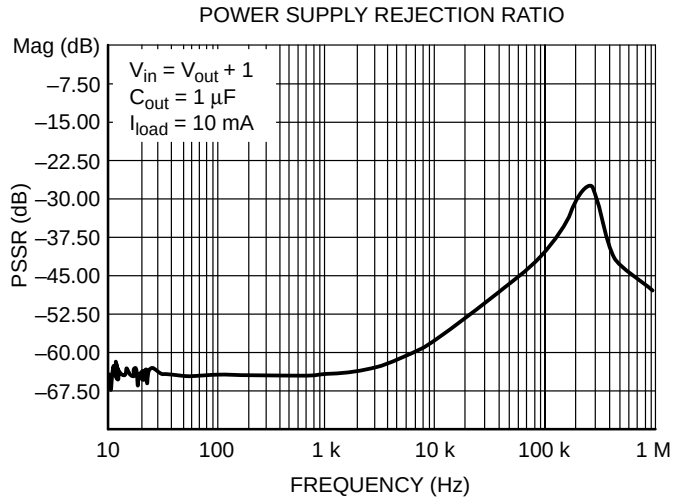


Figure 8. Typical Ripple Rejection Performance (I_{load} = 10 mA)

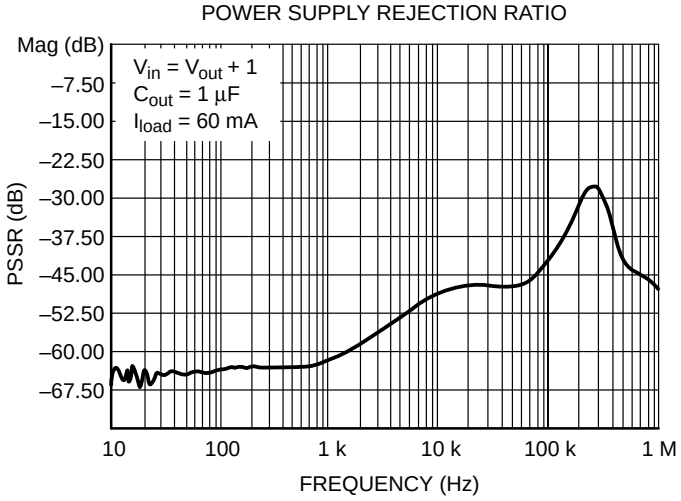


Figure 9. Typical Ripple Rejection Performance (I_{load} = 60 mA)

APPLICATION HINTS

Input Decoupling

As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP4561 package. Higher values will correspondingly improve the overall line transient response.

Output Decoupling

Thanks to a novel concept, the NCP4561 is a stable component and does not require any specific Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

Noise Decoupling

Unlike other LDOs, the NCP4561 is a true low–noise regulator. Without the need of an external bypass capacitor, it typically reaches the incredible level of 40 μVRMS overall noise between 100 Hz and 100 kHz. To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics. The classical bypass capacitor impacts the start–up phase of standard LDOs. However, thanks to its low–noise architecture, the NCP4561 operates without a bypass element and thus offers a typical 40 μs start–up phase.

Protections

The NCP4561 hosts several protections, giving natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a maximum value of 180 mA *typical* while temperature shutdown occurs if the die heats up beyond 125°C. These values let you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$P_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

If T_{Jmax} is limited to 125°C, then the NCP4561 can dissipate up to 470 mW @ 25°C. The power dissipated by the NCP4561 can be calculated from the following formula:

$$Ptot = \left(V_{in} \times I_{gnd}(I_{out})\right) + \left(V_{in} - V_{out}\right) \times I_{out}$$

or

$$Vin_{max} = \frac{Ptot + V_{out} \times I_{out}}{I_{gnd} + I_{out}}$$

If a 80 mA output current is needed, the ground current is extracted from the data–sheet curves: 4.0 mA @ 80 mA. For a NCP4561SNT1–28 (2.8 V) delivering 80 mA and operating at 25°C, the maximum input voltage will then be 8.3 V.

Typical Applications

The following figure portrays the typical application of the NCP4561.

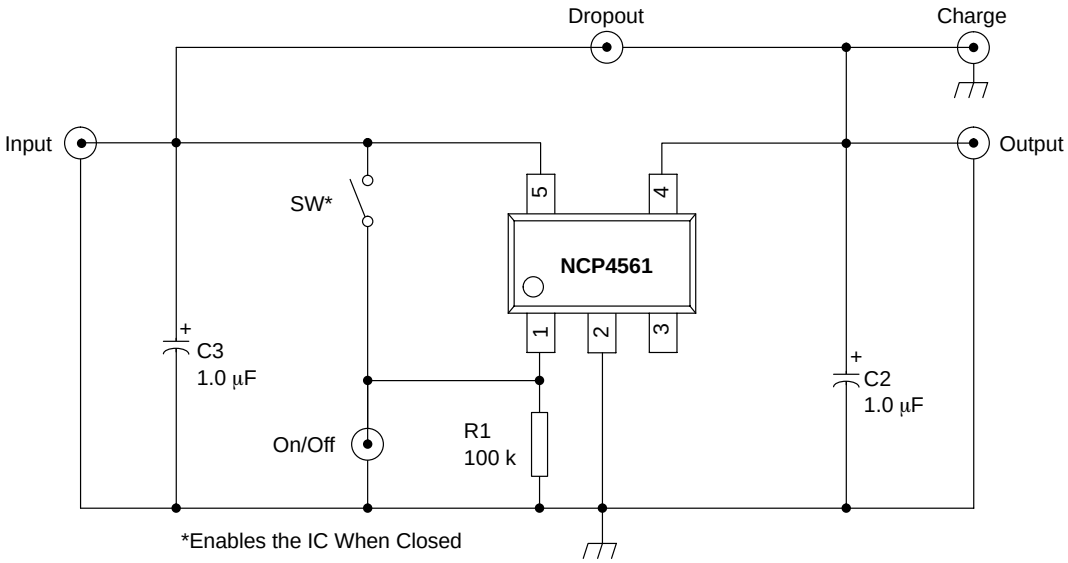


Figure 10. A Typical Application Schematic

PCB Layout Considerations

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. The figure below gives an example of a layout where stray inductances/capacitances are minimized. This layout is the basis for the NCP4561 performance evaluation board. The BNC connectors give the user an easy and quick evaluation mean.

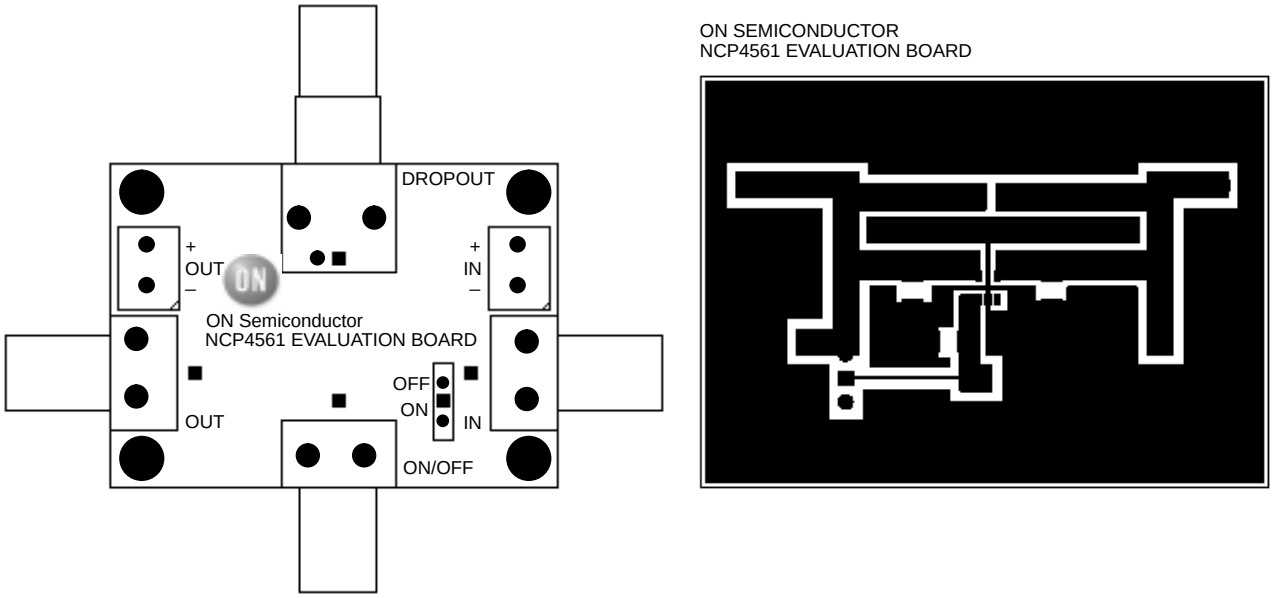


Figure 11. PCB Layout

Understanding the Load Transient Improvement

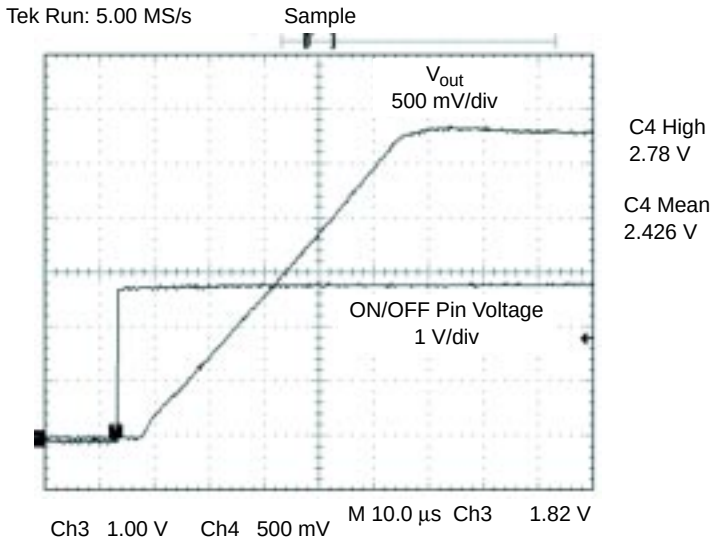
The NCP4561 features a novel architecture which allows the user to easily implement the regulator in burst systems where the time between two current shots is kept very small.

The quality of the transient response time is related to many parameters, among which the closed–loop bandwidth with the corresponding phase margin plays an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open–loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place with a positive overshoot. The problem appears when this overshoot decays down to the LDO steady–state value. During this decreasing phase, the LDO stops the PNP bias and one can consider the LDO asleep. If by misfortune a current shot appears, the reaction time is incredibly lengthened and a strong undershoot takes place. This reaction is clearly not acceptable for line sensitive devices, such as VCOs or other Radio–Frequency parts. This problem is dramatically exacerbated when the output current drops to zero rather than a few mA. In this later case, the internal feedback network is the only discharge path, accordingly lengthening the output voltage decay period.

The NCP4561 cures this problem by implementing a clever design where the LDO detects the presence of the overshoot and forces the system to go back to steady–state as soon as possible, ready for the next shot, which positively improves the response time and decreases the negative peak voltage.

NCP4561 has a fast start–up phase

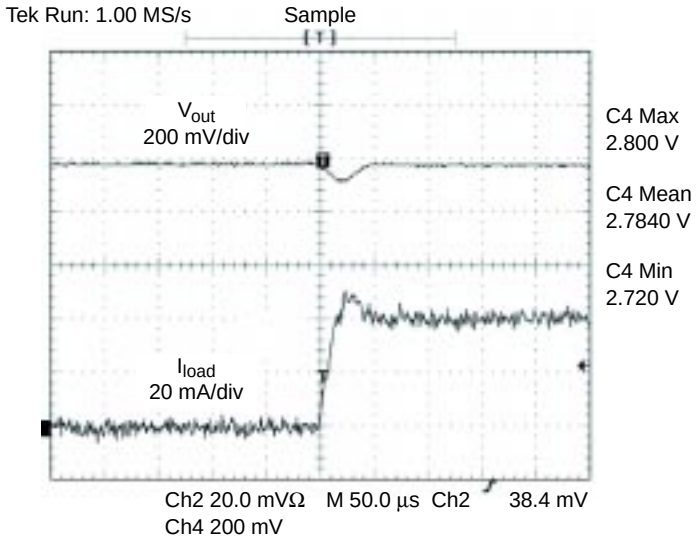
Thanks to the lack of bypass capacitor the NCP4561 is able to supply its downstream circuitry as soon as the OFF to ON signal appears. In a standard LDO, the charging time of the external bypass capacitor hampers the response time. A simple solution consists in suppressing this bypass element but, unfortunately, the noise rises to an unacceptable level. NCP4561 offers the best of both worlds since it no longer includes a bypass capacitor and starts in less than 40 μs typically (Repetitive at 200 Hz). It also ensures a low–noise level of 40 μVRMS 100 Hz–100 kHz. The following picture details the typical NCP4561 startup phase.



(Conditions: V_{in} = 3.8 V, I_{load} = 10 mA, C_{out} = 1 μF)

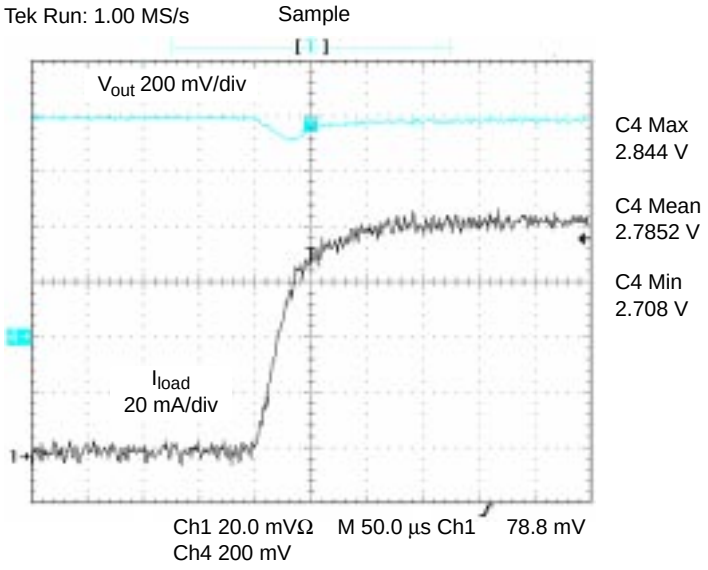
Figure 12. Start–Up Waveform

TYPICAL TRANSIENT RESPONSES



(Conditions: V_{in} = 3.8 V, $\mathbf{C_{out}}$ **= 1** µ**F**)

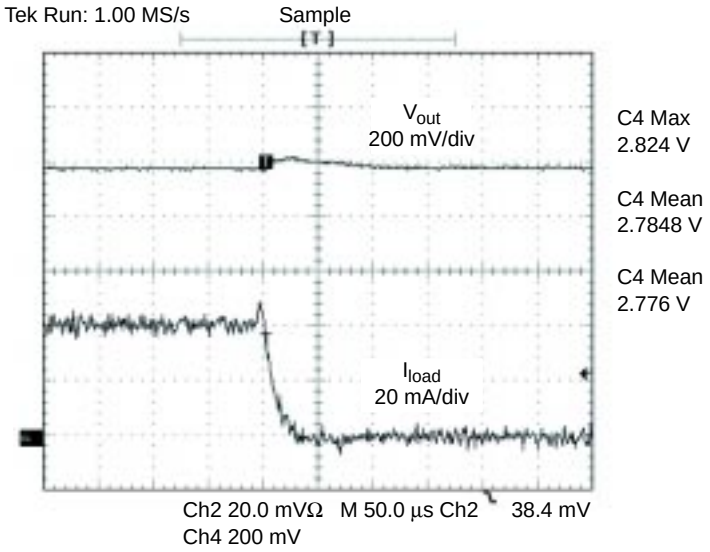
Figure 13. Load Current is Pulsed from 0 to 40 mA



(Conditions: V_{in} = 3.8 V, $\mathbf{C_{out}}$ **= 1** µ**F**)

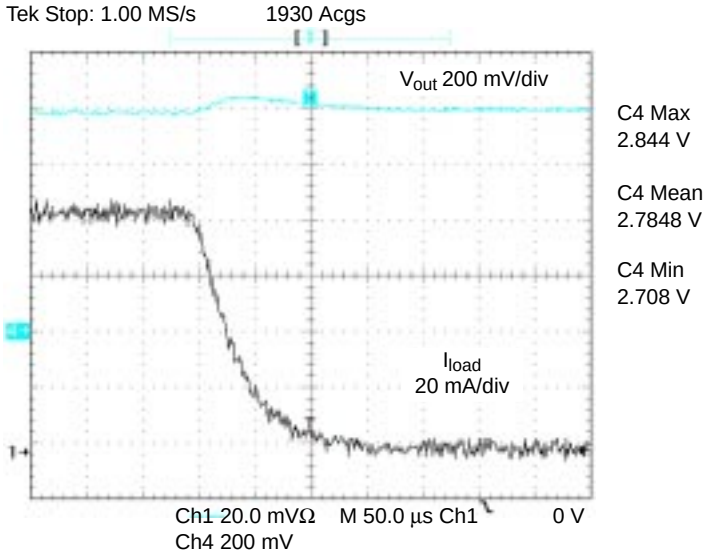
Figure 14. Load Current is Pulsed from 0 to 80 mA

TYPICAL TRANSIENT RESPONSES



(Conditions: V_{in} = 3.8 V, **C_{out} = 1 µF**)

Figure 15. Load Current is Switched from 40 to 0 mA

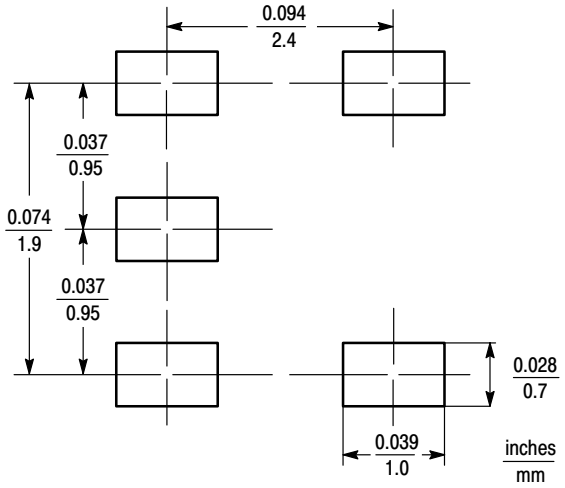


(Conditions: V_{in} = 3.8 V, **C_{out} = 1 µF**)

Figure 16. Load Current is Switched from 80 to 0 mA

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



TSOP–5

(TSOP–5 is footprint compatible with SOT23–5)

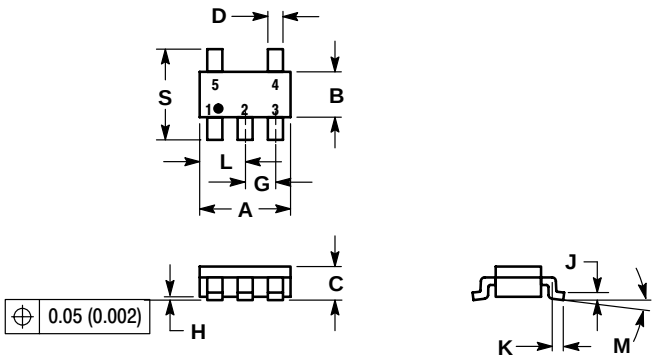
ORDERING INFORMATION

Device	Voltage Output*	Package	Shipping
NCP4561SNT1–28	2.8 V	TSOP–5	3000 Units /Tape & Reel

*Contact your ON Semiconductor sales representative for other output voltage values.

PACKAGE DIMENSIONS

TSOP–5
SN SUFFIX
PLASTIC PACKAGE
CASE 483–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

Notes

Notes

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