PRELIMINARY

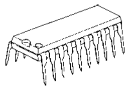
4-BIT SINGLE CHIP MICRO CONTROLLER

■ GENERAL DESCRIPTION

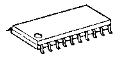
The **NJU3501** is the C-MOS 4-bit Single Chip Micro Controller consisting of the 4-bit CPU Core, Input / Output Selectable I/O ports, Program ROM, Data RAM, Timer, 8-bit Serial Interface, and Oscillator Circuit (CR or Ceramic or X'tal). It realizes the control for home appliances or toys by only few external components.

The **NJU3501** is suitable for battery operated appliances because of low operating current, wide operating voltage range, and STANDBY function(HALT mode).

■ PACKAGE OUTLINE



NJU3501D

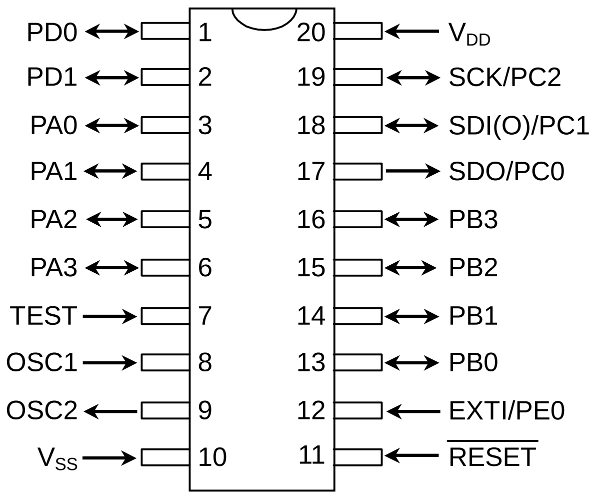


NJU3501G

■ FEATURES

- Internal Program ROM 512 X 8 bits
- Internal Data RAM 64 X 4 bits
- Input / Output Port 14 lines(MAX)
  - 6 lines Input / Output direction of each bit is selected by the mask option.
  - 4 lines Input / Output direction of 4-bit lines group can be changed by the program.
  - Additional functions by the mask option.
    - External Interrupt Terminal : EXTI/PE0
    - Serial Interface Terminals :SDO/PC0, SDI(O)/PC1, SCK/PC2
- High Output-Current terminal (4 lines)
  - N-Channel FET Open Drain Type (I_{OL}) 15mA at V_{DD}=5V
- Instruction Set 59 instructions
- Subroutine Nesting 8 levels
- Pulse Edge Detector
  - The rising or falling edge of a pulse is selected by the mask option.
- Instruction Executing Time 6/f_{OSC} sec
- Operating Frequency Range 30kHz–4MHz
- Internal Oscillator
  - CR, or Ceramic, or X'tal oscillation and External clock input
- STANDBY function (HALT mode)
- Wide operating voltage range 2.4V–5.5V
- 8-bit Serial Input / Output port
- Timer (8-bit re-load type timer)
- Interrupt factor 3(external, timer, serial Input / Output)
- C-MOS technology
- Package outline DIP / SOP20

■ PIN CONFIGURATION



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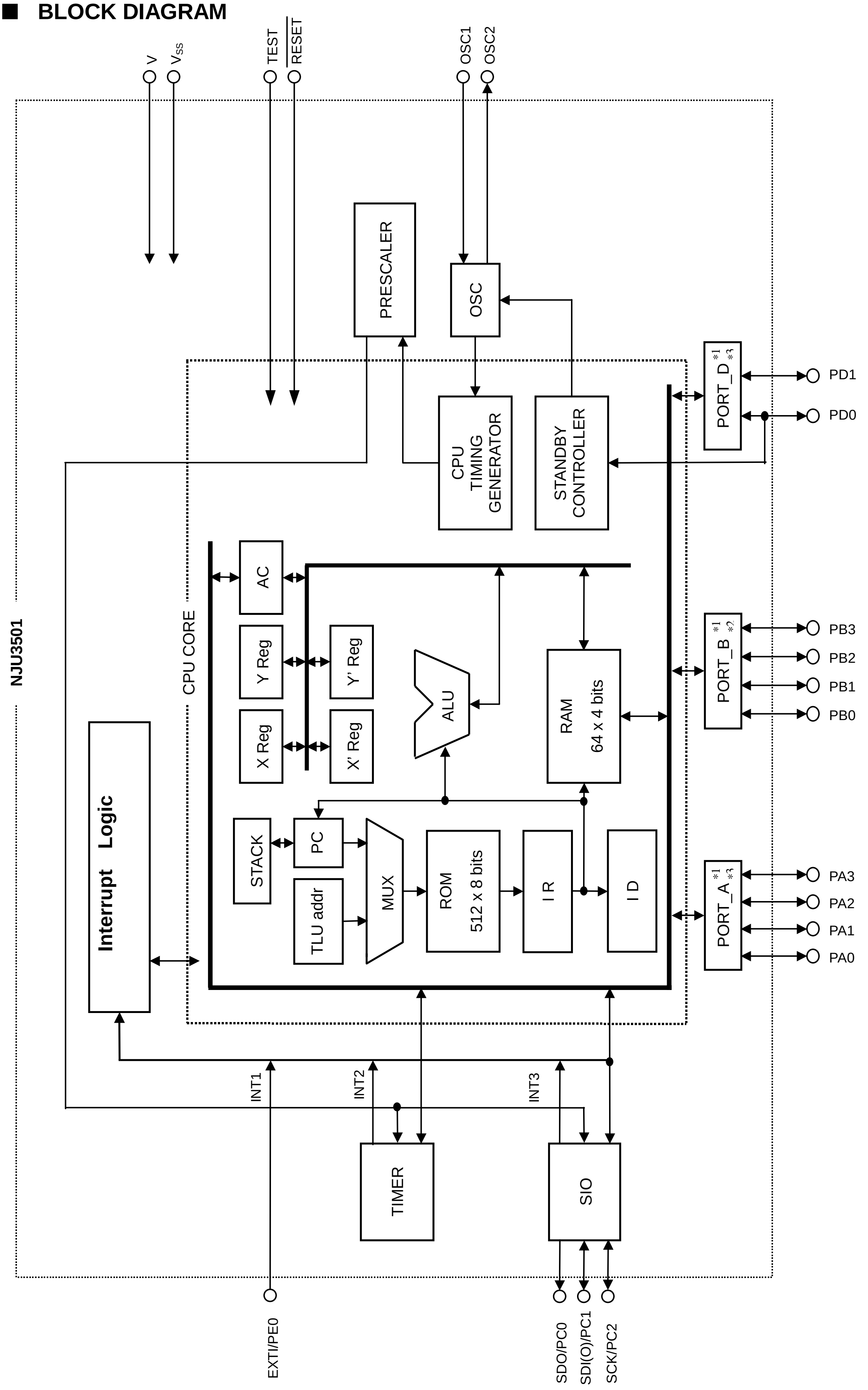
■ BLOCK DIAGRAM


V
VSS
TEST
RESET
OSC1
OSC2
NJU3501
CPU CORE
PRESCALER
OSC
CPU TIMING GENERATOR
STANDBY CONTROLLER
PORT_D *1 *3
PD1
PD0
AC
Y Reg
Y' Reg
X Reg
X' Reg
ALU
RAM
64 x 4 bits
PORT_B *1 *2
PB3
PB2
PB1
PB0
Interrupt Logic
STACK
PC
TLU addr
MUX
ROM
512 x 8 bits
I R
I D
PORT_A *1 *3
PA3
PA2
PA1
PA0
INT1
INT2
INT3
TIMER
SIO
EXTI/PE0
SDO/PC0
SDI(O)/PC1
SCK/PC2

*1 Refer ■ INPUT/OUTPUT TERMINAL TYPE

*2 Input / Output direction of 4-bit group is changed by the program.

*3 Input / Output direction of each bit is selected by mask option.

TERMINAL DESCRIPTION 1

No.	SYMBOL	INPUT/OUTPUT	FUNCTION
1 2	PD0 PD1	INPUT/OUTPUT INPUT/OUTPUT	2-bit Input / Output PORTD. Selects a terminal circuit for each port from follows by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance(IB) •C-MOS Schmitt Trigger Input terminal(ID) •C-MOS Output Terminal(OB) When the ports are selected as the input terminal, PD0 operates also as RESTART signal input terminal to return from STANDBY mode, and PD1 operates also as the Edge Detector Terminal.
3 4 5 6	PA0 PA1 PA2 PA3	INPUT/OUTPUT INPUT/OUTPUT INPUT/OUTPUT INPUT/OUTPUT	4-bit Input / Output PORTA. Selects a terminal circuit for each port from follows by the mask option. •C-MOS Input Terminal with Pull-up Resistance(IA) •C-MOS Input Terminal(IC) •C-MOS Output Terminal(OB)
7	TEST	INPUT	Maker Testing Terminal with Pull-down Resistance The terminal is recommended to connect to GND.
8 9	OSC1 OSC2	INPUT OUTPUT	Internal Oscillator Terminals. Connects a device selected from the ceramic or the crystal resonator, or the resistor, to these terminals for the internal oscillator. In the external clock operation, OSC1 is the external clock input terminal and OSC2 is normally open terminal.
10	V_{SS}	–	Power Source (0V)
11	$\overline{\text{RESET}}$	INPUT	RESET Terminal. When the low level input-signal, the system is initialized.
12	EXTI / PE0	INPUT	1-bit Input PORTE. Selects a function of either 1) or 2) for PORTE by the mask option. 1) External Interrupt Input Terminal with Pull-up Resistance. :EXTI 2) 1-bit Input Terminals as PORTE. Selects a terminal circuit for each port from follows by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance(IB) •C-MOS Schmitt Trigger Input Terminal(ID)
13 14 15 16	PB0 PB1 PB2 PB3	INOUT INOUT INOUT INOUT	4-bit Programmable Input / Output PORTB These 4-bit terminals' direction can be changed by the program as 4-Input or 4-Output. Use of Pull-up resistance is in accordance with the mask option. •as Input : C-MOS Input Terminals •as Output : Nch-FET Open-Drain Output Terminals

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
INOUT : Input or Output is changed by the program.

■ TERMINAL DESCRIPTION 2

No.	SYMBOL	INPUT/OUTPUT	FUNCTION
17 18 19	SDO / PC0 SDI(O) / PC1 SCK / PC2	SDO :OUTPUT SDI(O) :INOUT SCK :INOUT PC0–PC2 : INPUT/OUTPUT	3-bit Input / Output PORTC. Selects a function of either 1) or 2) for PORTC by the mask option. 1) Serial Interface Function. Serial Data Output Terminal : SDO Serial Data Input-Output Terminal with Pull-up Resistance : SDI(O) Serial Clock Input or Output Terminal with Pull-up Resistance : SCK 2) 3-bit Input / Output Terminal PORTC. Selects a terminal circuit for each port from follows by the mask option. •C-MOS Input Terminal with Pull-up Resistance(IA) •C-MOS Input Terminal(IC) •C-MOS Output Terminal(OB)
20	V_{DD}	–	Power Source (2.4V–5.5V)

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
INOUT : Input or Output is changed by the program.

■ INTERNAL SYSTEM DESCRIPTION

The **NJU3501** is a C-MOS 4-Bit Single Chip Micro Controller consisted of Original CPU Core, Selectable Input-Output(I/O) Ports(MAX. 14 lines), Program ROM(512 bytes), Data RAM(64 nibbles), 8-bit Serial Interface, 8-Bit Timer, Interrupt Control Circuit and Oscillator Circuit.

The CPU block in the **NJU3501** is consisted of ALU(Arithmetic Logic Unit) executing the binary adding, subtracting or logical calculating, AC(Accumulator), four Registers, STACK allowing the 8-level subroutine-nesting or Interrupt operation, PC(Program Counter) indicating 512 addresses sequentially, and Timing generator.

The **NJU3501** can be applied to the various markets because of the rich and efficient instruction set(59 instructions), wide operating voltage range(2.4V to 5.5V), low operating current, and STANDBY function reducing the power supply current.

(1) INTERNAL REGISTER

- Accumulator(AC)

  Accumulator(AC) is structured by the 4-bit register. It holds a data or a result of calculation, and executes the shift-operation(ROTATE) or the data transference between the other registers and Data Memory(RAM).

  Accumulator(AC) condition is unknown on the “RESET” operation.

- X-register(X-reg)

  X-register(X-reg) operates as the 4-bit register. Bit0 and bit1 of X-reg operate also as the RAM address pointer with Y-register.

  The X-reg condition is unknown on the “RESET” operation.

- Y-register(Y-reg)

  Y-register(Y-reg) operates as the 4-bit register or the RAM address pointer with bit1 and bit2 of X-reg.

  The Y-reg condition is unknown on the “RESET” operation.

- X'-register(X'-reg)

  X'-register(X'-reg) operates as the 4-bit register or a part of Program Memory(ROM) address pointer for looking data in the ROM(TRM instruction) up function.

  The X’-reg condition is unknown on the “RESET” operation.

- Y'-register(Y'-reg)

  Y'-register(Y'-reg) operates as the 4-bit register or the peripheral register number(PHYn) pointer.

  The Y’-reg condition is unknown on the “RESET” operation.

(2) INTERNAL FLAG

- RPC flag(RPC)

  RPC flag(RPC) changes the instruction table. Several instructions perform either of the dual tasks in accordance with the RPC flag condition. The RPC flag condition selects either of two couples of registers which are X- and Y- reg, or X’- and Y'-reg. X- or Y- reg is selected when the RPC flag condition is "0"(RPC=0). X'- or Y'- reg is selected when the RPC flag condition is "1"(RPC=1). The RPC flag condition is set to "1"(RPC=1) by SRPC instruction, and is set to “0”(RPC=0) by RRPC instruction.

  The RPC flag condition is set to “0” on the “RESET” operation.

- CARRY flag(CY)

  When the carry occurs after the adding calculation, the CARRY flag(CY) condition is set to "1"(CY=1), and when no carry, the CY flag condition is set to "0"(CY=0). When the borrow occurs after the subtracting calculation, the CY flag condition is set to "0"(CY=0), and when no borrow, the CY flag condition is set to "1"(CY=1). The bit-operation instruction executes the bit data rotation on the CY flag combined with the Accumulator or the other register.

  The CY flag condition is set to "1"(CY=1) by SEC instruction and is set to "0"(CY=0) by CLC instruction. The CY flag condition is kept until the end of the next instruction operates cycle. The CY flag condition is unknown on the “RESET” operation.

- STATUS flag(ST)

  STATUS flag(ST) is the conditional flag in accordance with the result of the instruction execution. Its condition is in accordance with follows:

  1) to be same as CY flag condition.
  2) to be set the condition to "0"(ST=0) when the result of the logical calculation(AND, OR, XOR, YNEA) is zero.
  3) to be set the condition to "0"(ST=0) when the result of the comparison(CMP) is zero.

  However, ST flag condition is always set to "1"(ST=1) except above three.

  ST flag controls the branch operation. Branch instruction does not branch when ST flag condition is "0", and branches when ST flag condition is "1". ST flag condition is kept until the end of the next instruction executing cycle.

  The ST flag condition is unknown on the “RESET” operation.

(3) FUNCTIONAL BLOCK

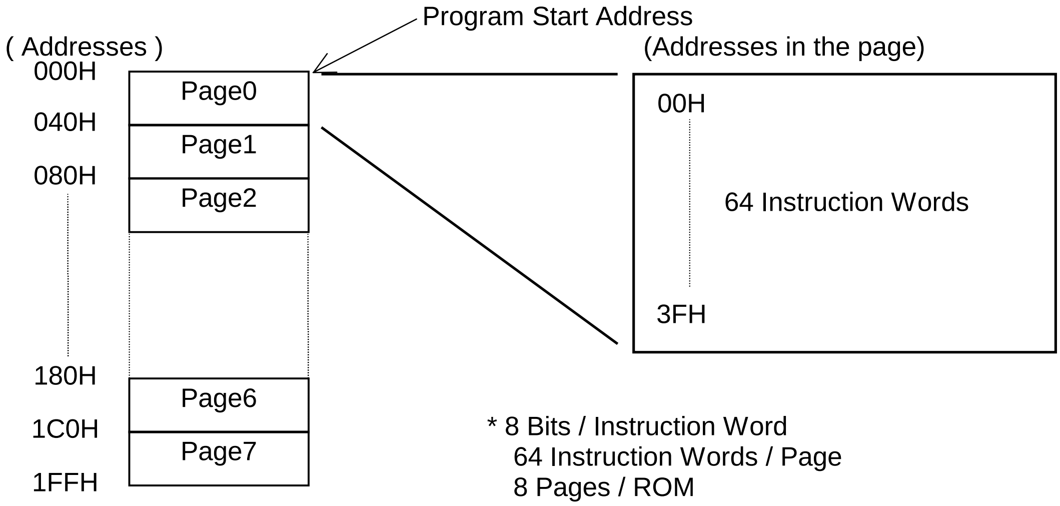
- ARITHMETIC LOGIC UNIT(ALU)

  ARITHMETIC LOGIC UNIT(ALU) is a 4-bit binary paralleled calculation circuit operating binary addition, binary subtraction, comparison, logical AND, logical OR, exclusive OR, and SHIFT(Rotation). And it also can detect CARRY, BORROW or ZERO in accordance with the result of each calculation.

- PROGRAM MEMORY(ROM)

  PROGRAM MEMORY(ROM) consists of 8 pages, and a page consists of 64 bytes memory capacity. Therefore the **NJU3501** prepares the 512-byte ROM for the application program. The ROM address is indicated by the Program Counter(PC).

[PROGRAM MEMORY AREA]

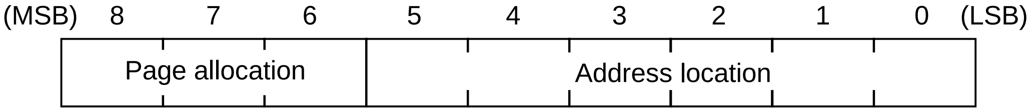


* 8 Bits / Instruction Word
64 Instruction Words / Page
8 Pages / ROM

- PROGRAM COUNTER(PC)

PROGRAM COUNTER(PC) consisted of the 9-bit binary counter stores the address for the next operating instruction in ROM. Data figures limited from b0 to b5 on the PC indicate the address in a page, and data figures limited from b6 to b8 on the PC indicate the page in ROM. Although the ROM address can be indicated 512 addresses continuously, the target address of JMP instruction is restricted by Paging structure in ROM.

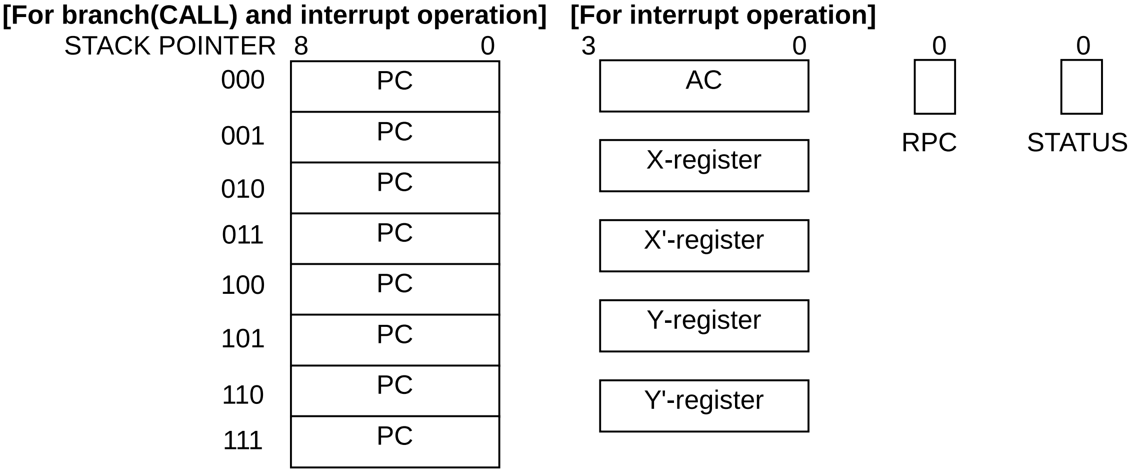
The PC condition is set to “0” on the “RESET” operation.



JMP instruction can branch to the optional address in the page. The target address is indicated by the data figures limited from b0 to b5(6 bits) on PC as shown in above. The paging structure can reduce the program size in ROM and the JMP instruction execution time against JPL instruction because JMP instruction is consisted of one byte(8 bits) length. JPL and CALL instructions can branch to the optional address without considering the paging structure, because they consist of two bytes(16 bits) length including the full bits(9 bits) of PC.

- STACK

STACK consists of three types of registers which are the 8 by 9 bits, the 5 by 4 bits, and the 2 by 1 bit registers. The registers of STACK hold the data of PC automatically when the interrupt routine or the subroutine is called. The 5 by 4 bits registers of STACK hold the data of the internal registers automatically when the interrupt operation is executed. The 2 by 1 bit registers of STACK hold the data of the internal flag automatically when the interrupt operation is executed. In the return (RET or RETI) operation, PC, the internal registers, and the internal flags registers get the held data from STACK automatically.



- STACK POINTER(SP)

STACK POINTER(SP) consists of the 3 bits binary counter. SP indicates the number of next operating position in the STACK. It counts one up(increment) after the subroutine call(CALL) or the interrupt operation, and it counts one down(decrement) after the return(RET or RETI) operation.

Data storing operation to STACK after that SP overflowed(over than 7) or under flowed(under than 0), breaks the former held data in STACK. Therefore the subroutine nesting level must be cautioned in the application program.

SP condition is set to "0" on “RESET” operation.

- DATA MEMORY(RAM)

  DATA MEMORY(RAM) is formed with the 4-bit length a word. The **NJU3501** prepares 64 words(256 bits) RAM. The data formed with the 4-bit length a word can be read/written from/to RAM, and the data formed with the 1-bit length in a word can be set, reset, or tested by the bit-operation instruction.

  The RAM address is indicated indirectly by X- and Y-reg. The lower 2 bits(b0, b1) in X-reg are used as the RAM address pointer and the higher 2 bits(b2, b3) are not used.

[RAM ADDRESS MAP]

Y-reg →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	[HEX]
0																	
1																	
2																	
3																	

[HEX] ↑

X-reg

- PERIPHERAL REGISTERs(PH)

PERIPHERAL REGISTERs(PH) controlling I/O Ports or the ROM address are selected by the data in Y'-reg.

The Peripheral Register assigned for each I/O Port can get the signal data from the external application by reading operation, or can output the signal data to the external application by writing operation in accordance with the type of input or output selected by the mask option. Although the data can be read from the Peripheral Register assigned as the Output, it sometimes takes the incorrect data of the Output Port.

[PERIPHERAL REGISTER TABLE]

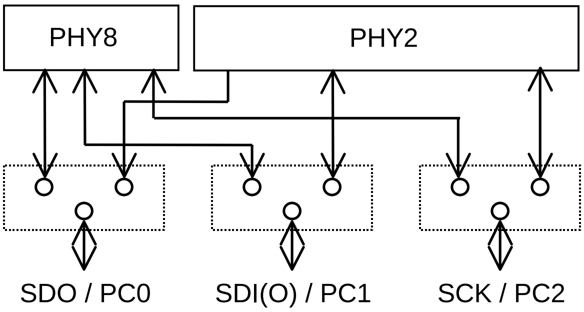
Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read ∗1	Data in Reset
0H	PHY0 (00H)				0
1H	PHY1 (01H)	Serial Input/Output Control Register	–	WR	0 ∗2
2H	PHY2 (02H)	Serial Input/Output Shift Register	–	WR	0 ∗2
3H	PHY3 (03H)	Timer/Prescaler Control Register	–	WR	0
4H	PHY4 (04H)	Initial Value Register / Timer Counter	–	WR	0
5H	PHY5 (05H)	Interrupt Control Register	–	WR	0
6H	PHY6 (06H)	PORTA Output or PORTA Input	4	W or R	0
7H	PHY7 (07H)	PORTB Output or PORTB Input	4	WR	0
8H	PHY8 (08H)	PORTC Output or PORTC Input	3	W or R	0 ∗2
9H	PHY9 (09H)	PORTD Output or PORTD Input	2	W or R	0
AH	PHY10(0AH)	PORTE Input	1	R	0 ∗3
BH	PHY11(0BH)	PORTB Input/Output Control Register	1	WR	0
CH	PHY12(0CH)				
DH	PHY13(0DH)	ROM Addressing Register	4	WR	unknown
EH	PHY14(0EH)				
FH	PHY15(0FH)				

∗1

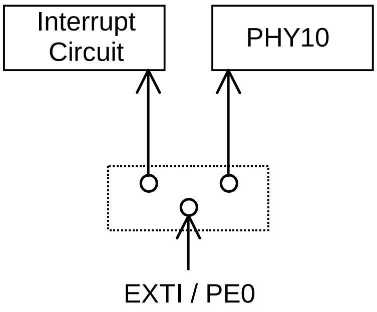
W	: Write only
R	: Read only
WR	: Read and Write
W or R	: Fixed as Read or Write by the mask option

∗2 Wiring of terminals

The mask option selects a terminal type from SDO/PC0, SDI(O)/PC1 or SCK/PC2 as shown in right.



∗3 Wiring of terminals
The mask option selects a terminal type from EXTI/PE0 as shown in right.



- ROM ADDRESSING REGISTER(PHY13)

  ROM ADDRESSING REGISTER(PHY13) indicates the address of ROM with Accumulator and X'-reg for the data transference operation(TRM) from ROM to RAM. The effective bit on PHY13 is b0, and the other three bits, b1, b2, and, b3, are not related.

  The PHY13 condition is unknown on “RESET” operation.

[ROM ADDRESSING]

no used			A8	A7	A6	A5	A4	A3	A2	A1	A0
b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0
PHY13				X’				AC			

■ INPUT OUTPUT PORT

The **NJU3501** prepares 10 Input-Output lines and 4 dual-function lines for the interface to an external application circuit. All lines are assigned to each Peripheral Register.

Data reading operation from the peripheral register can input the actual signals through the input terminal. Data writing operation to the peripheral register can output the actual signals through the output terminal.

[FUNCTION OF EACH PORT TABLE]

PORT NAME	FUNCTION	INPUT/OUTPUT
PORTB	Input / Output Port	Programmable Input / Output PORT (4-bit).
PORTA PORTD	Input / Output Port	Input / Output selectable ports by the mask option.
PORTE	Input Port or EXTI	Input
PORTC(PC0)	Input / Output Port or SDO	Input / Output selectable ports by the mask option.
PORTC(PC1)	Input / Output Port or SDI(O)	Input / Output selectable ports by the mask option.
PORTC(PC2)	Input / Output Port or SCK	Input / Output selectable ports by the mask option.

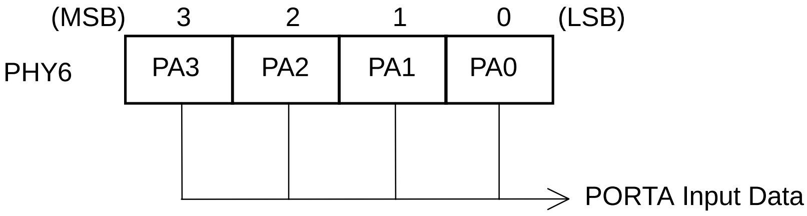
Note) Pull-up resistance is selected by the mask option. (refer ■ INPUT OUTPUT TERMINAL TYPE)

(1) INPUT OUTPUT PORT

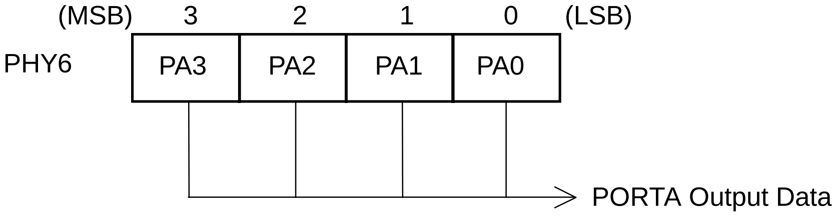
- PORTA(PA0–PA3)

  PORTA is a 4-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTA register(PHY6). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY6.

[READING PORTA INPUT DATA (PHY6)]



[WRITING PORTA OUTPUT DATA (PHY6)]



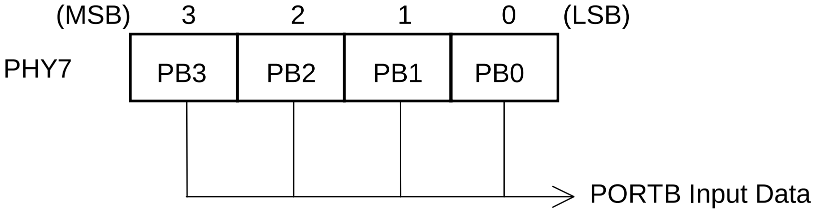
- PORTB(PB0–PB3)

PORTB is a 4-bit programmable input-output PORT. It is set as the output when LSB of the programmable input/output control register(PHY11) is set to “1”, and is set as the input when LSB of PHY11 is set to “0”. When the PORT is set as the output, the 4-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTB(PHY7). PHY7 as the output register should be written the output data before the PORTB is set as the output by PHY11, because the conditions of the output terminals are unknown while the output data is not written in PHY7. When this PORT is set as the input, the 4-bit external signals are gotten directly through the input terminals by reading data from PHY7. PHY7 can be written or read independent of the state of PHY11 as the input or output.

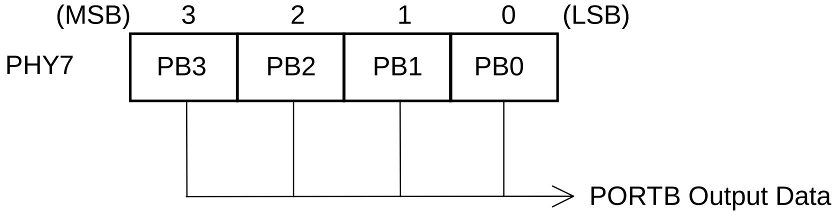
Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between V_{DD} and V_{SS} is input to this terminal.

PORTB is set as the input in accordance with the state of PHY11 set to “0” on the “RESET” operation.

[READING PORTB INPUT DATA (PHY7)]



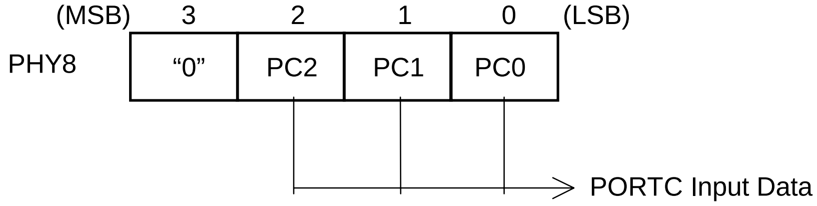
[WRITING PORTB OUTPUT DATA (PHY7)]



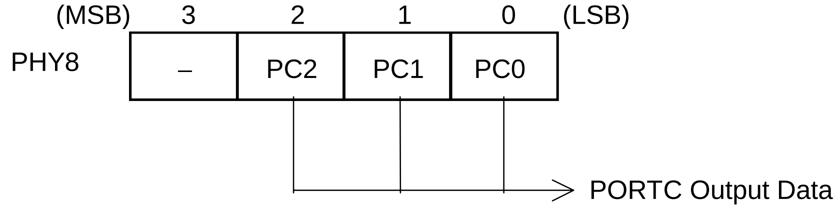
- PORTC(PC0–PC2)

PORTC is a 3-bit input-output PORT. It operates also as SDO, SDI(O) and SCK terminals for the 8-bit serial interface by the mask option. When the PORTC is selected as the input-output PORT, PC0 to PC2 can be selected as the input or the output by the mask option. When the PORTC is selected as the output, the three signals are output through the output terminals to the external circuit by writing data to the PORTC register(PHY8). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY8.

[READING PORTC INPUT DATA (PHY8)]



[WRITING PORTC OUTPUT DATA (PHY8)]



- PORTD(PD0, PD1)

PORTD is a 2-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTD register(PHY9). When the port is set as the input, the external signal is gotten directly though the input terminal by reading data from PHY9. When this PORTD is set as the input, these two ports perform the extra functions as follows:

a) PD0 TERMINAL

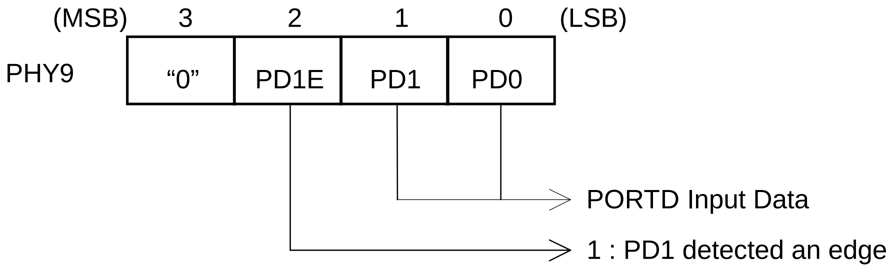
PD0 terminal performs the extra function as the restart signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PD0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program. (refer ■ STANDBY FUNCTION)

b) PD1 TERMINAL

PD1 terminal performs the extra function as the edge detector terminal. When the PD1 terminal detects the edge of the signal from the external circuit, the third bit(b2) condition of PHY9 is set to "1". The “b2” of PHY9 is set to "1" even when the edge is input during the “STANDBY” mode. The condition of “b2” is kept until the writing operation to PHY9.

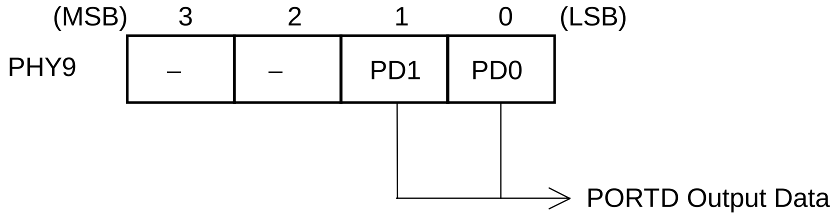
The polarity as low to high or high to low of the input signal edge can be selected by the mask option.

[READING PORTD INPUT DATA (PHY9)]



	(MSB) 3	2	1	0 (LSB)
PHY9	“0”	PD1E	PD1	PD0

[WRITING PORTD OUTPUT DATA (PHY9)]

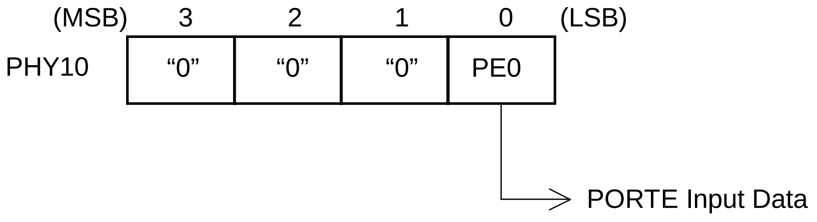


	(MSB) 3	2	1	0 (LSB)
PHY9	–	–	PD1	PD0

- PORTE(PE0)

PORTE is a 1-bit input PORT. It operates also as EXTI terminal for external interrupt input by the mask option. When the PORTK is set as the input PORT, the external signal is gotten directly through the input terminal by reading data from PHY10.

[READING PORTE INPUT DATA (PHY10)]



	(MSB) 3	2	1	0 (LSB)
PHY10	“0”	“0”	“0”	PE0

- PROGRAMMABLE INPUT/OUTPUT PORT CONTROL REGISTER(PHY11)

  Programmable Input / Output Port Control Register(PHY11) is a peripheral register to set the programmable input/output PORT(PORTB) as either the input or the output. All bits in PORTB are set as the output when LSB(b0) of PHY11 is set to “1”. All bits in PORTB are set as the input when “b1” of PHY11 set to “0”.

  PORTB is set as the input in accordance with the state of PHY11 which is set to “0” on the “RESET” operation.

[READING PORTB Input / Output Port Control Register(PHY11)]

	(MSB) 3	2	1	0 (LSB)
PHY11	“0”	“0”	“0”	“*”

└→ PORTB input/output state
(0:input, 1:output)

[WRITING PORTB Input / Output Port Control Register(PHY11)]

	(MSB) 3	2	1	0 (LSB)
PHY11	–	–	–	“*”

└→ PORTB input/output setting
(0:input, 1:output)

(2) PROGRAMMABLE INPUT/OUTPUT PORT OPERATION

a. The output operation example

PB0 and PB1 of PORTB output “H”, and PB2 and PB3 of PORTB output “L”.

```
                :
        SRPC                ;
        LDI     Y,7         ;PHY7 is pointed
        LDI     A,%0011     ;"0011" is stored into Accumulator
        TAP                 ;Data in Accumulator is transmitted to PHY7
                            ;     (PORTB output register)
        LDI     Y,11        ;PHY11 is pointed                          ⎫ PORTB is
        LDI     A,%0001     ;"0001" is stored into Accumulator         ⎬ set as the output
        TAP                 ;Data in Accumulator is transmitted to PHY11 ⎭
                :
```

b. The input operation example

Accumulator gets the input data from PORTB.

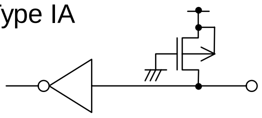
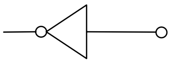
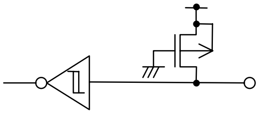
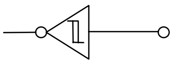
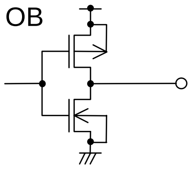
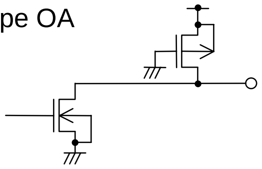
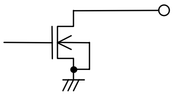
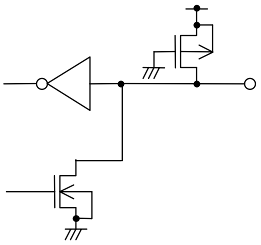
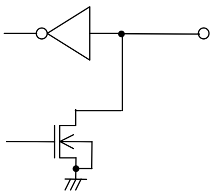
```
                :
        SRPC                ;
        LDI     Y,11        ;PHY11 is pointed                          ⎫ PORTB is
        LDI     A,%0000     ;"0000" is stored into Accumulator         ⎬ set as the input
        TAP                 ;Data in Accumulator is transferred to PHY11 ⎭
        LDI     Y,7         ;PHY7 is pointed
        TPA                 ;The input data from PHY7 is transferred to Accumulator
                :
```

The signal from PB0 terminal is stored into the LSB of Accumulator, the signal from PB1 terminal is stored into the b1 of Accumulator, the signal from PB2 terminal is stored into the b2 of Accumulator, and the signal from PB3 terminal is stored into the b3 of Accumulator.

■ INPUT OUTPUT TERMINAL TYPE

Each terminal of PORTA, B, C, D, and E can select a terminal type from the follows by the mask option which is the same mask of the program coding in ROM and the others. But PORTE selects only the input terminal type.

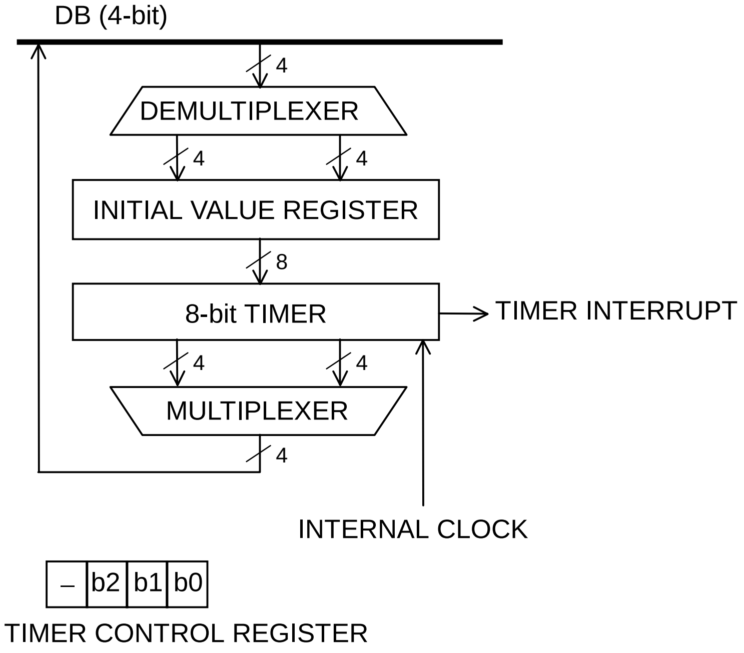
[INPUT OUTPUT TERMINAL TYPES]

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type IA 	Type IC 	PA0–PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2
	SCHMITT TRIGGER	Type IB 	Type ID 	PD0, PD1, EXTI/PE0
OUTPUT TERMINAL	C-MOS		Type OB 	PA0–PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1
	N-channel (Nch) OPEN DRAIN	Type OA 	Type OC 	
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT/ N-channel (Nch) OPEN DRAIN OUTPUT	Type C 	Type D 	PB0–PB3

■ TIMER

The **NJU3501** prepares Programmable Timer consisted of 8-bit binary counter.

[Structure of TIMER]



Timer counts only the internal clock. The initial value of the Timer can be set the optional value by the program which instructs to write the data(a value of the time-interval) into the Initial Value Register. In enabling the Timer interrupt, when the Timer counts from "FF" to "00" (overflow), the Timer interrupt request occurs and the internal interrupt process starts the own operation.

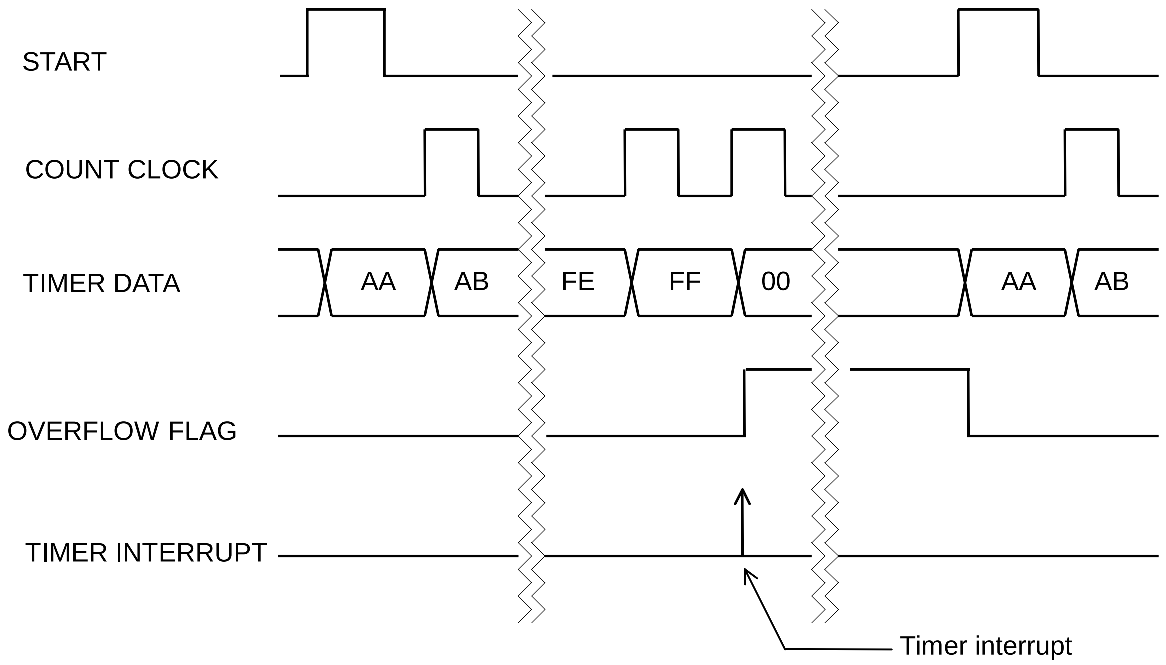
In the repeat mode of the Timer operation, when the Timer overflows, the initial value is loaded into the Timer automatically and the Timer continues the count from the loaded initial value (Auto re-load function: See the repeat mode of the Timer operation timing chart). In the single mode of the Timer operation, when the Timer overflows, the count is stopped(See the single mode of the Timer operation timing chart). For starting the count operation again, the start bit(LSB) of Timer Control Register must be set to "1". The latest initial value is set into the Timer and the Timer starts the count.

In enabling the interrupt operation, when the Timer overflows, the Timer overflow flag is set to "1" and the internal interrupt process starts to the own operation. In disabling the Timer interrupt, the Timer overflow flag is not set. The Timer overflow flag is initialized by the Timer Start or the Reset signal.

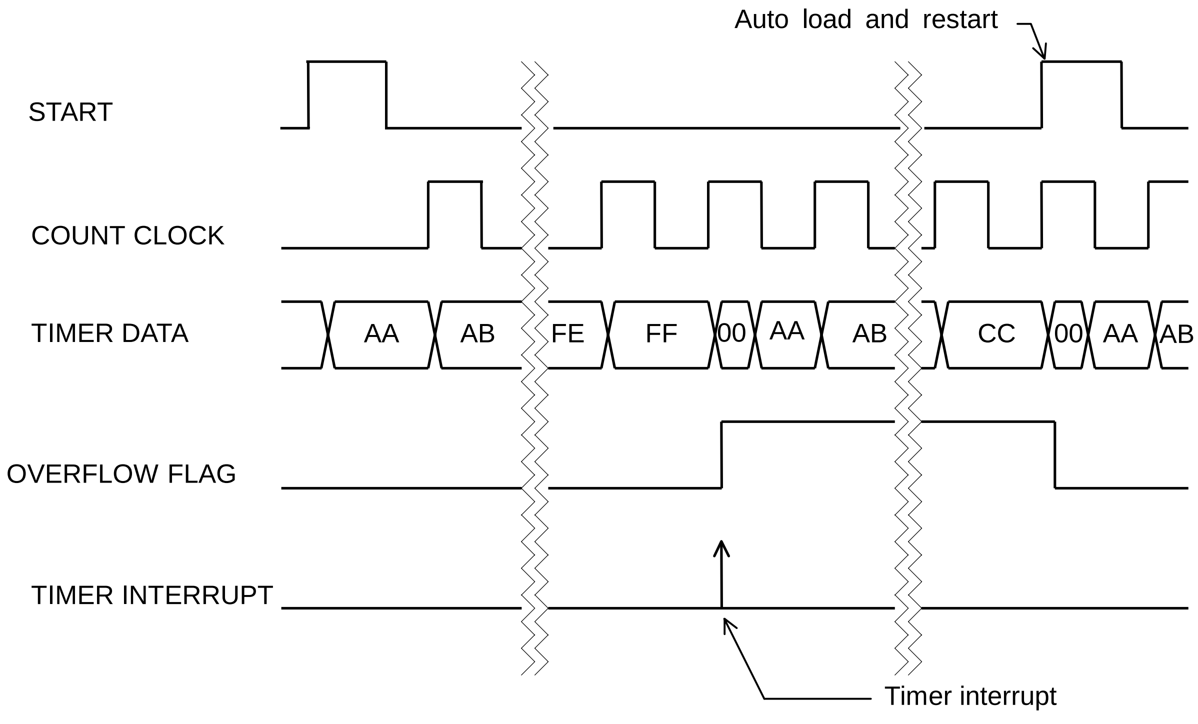
The internal clock into the counter is the divided clock from the internal prescaler. the frequency of the clock can be selected by the mask option from follows which are the dividing numbers based on the inverse of the 1-instruction executing period($1/f_{OSC}$ x 6).

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

[THE SINGLE MODE OF THE TIMER OPERATION TIMING] (The initial value is set to "AAh")

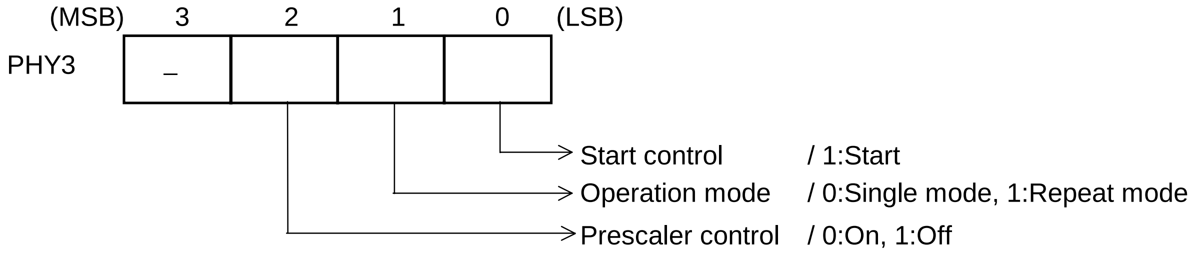

START
COUNT CLOCK
TIMER DATA
AA
AB
FE
FF
00
AA
AB
OVERFLOW FLAG
TIMER INTERRUPT
Timer interrupt

[THE REPEAT MODE OF THE TIMER OPERATION TIMING] (The initial value is set to "AAh")


Auto load and restart
START
COUNT CLOCK
TIMER DATA
AA
AB
FE
FF
00
AA
AB
CC
00
AA
AB
OVERFLOW FLAG
TIMER INTERRUPT
Timer interrupt

- TIMER / PRESCALER CONTROL REGISTER {PHY3 ; (Y'=3)}

[Writing to Timer / Prescaler Control Register]

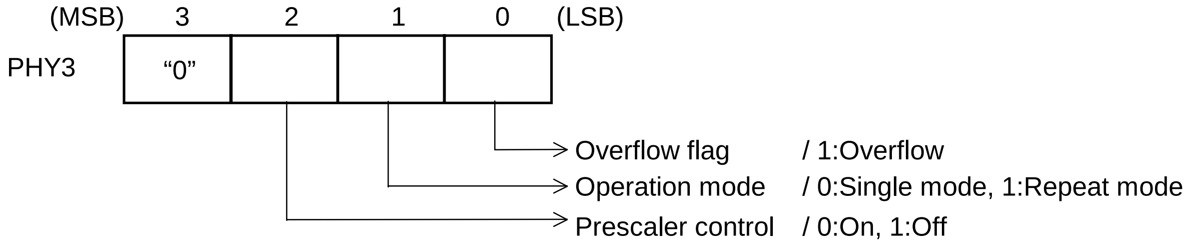

(MSB)
3
2
1
0
(LSB)
PHY3
–
Start control / 1:Start
Operation mode / 0:Single mode, 1:Repeat mode
Prescaler control / 0:On, 1:Off

EX.)An example of the start procedure in the single mode and the internal clock operation.

```
        :
        :
SRPC                    ;
LDI     Y,3             ;PHY3(Timer1/Prescaler Control Register) is pointed.
LDI     A,%0000         ;"0000"(BIN) is stored to accumulator            } Single mode,
TAP                     ;Data is transferred from accumulator to PHY3    } Prescaler is enable
LDI     A,%0001         ;"0001"(BIN) is stored to accumulator            }
TAP                     ;Data is transferred from accumulator to PHY3    } The count is started.
        :
        :
```

Remarks) When the prescaler generating the internal count clock is stopped the operation, Timer is also stopped. But the data in the counter is kept. Therefore Timer can continue to count from the kept condition of the counter when the prescaler is started the operation again. However, the clocks from the prescaler are delivered to Serial I/O, therefore the prescaler requires careful operation, especially stop or start. When the prescaler is started the operation again after it was stopped, it is reset and start to count from “zero”.

[Reading from Timer / Prescaler Control Register]


(MSB)
3
2
1
0
(LSB)
PHY3
“0”
Overflow flag / 1:Overflow
Operation mode / 0:Single mode, 1:Repeat mode
Prescaler control / 0:On, 1:Off

EX.)An example of the overflow in the single mode and the internal clock operation.(The data of the Timer / Prescaler Control Register is "0001"(BIN).)

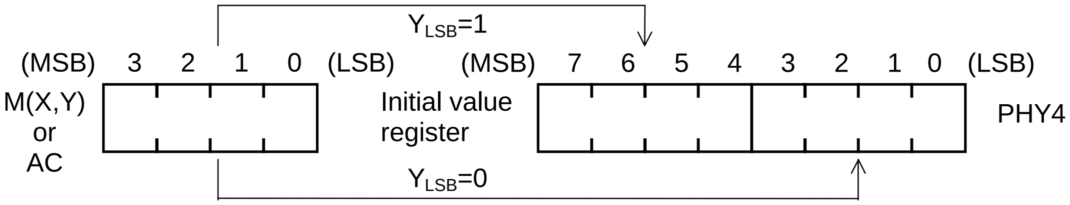
```
        :
        :
SRPC                    ;
LDI     Y,3             ;PHY3(Timer/Prescaler Control Register) is pointed.
TPA                     ;"0001"(BIN) of PHY3 is transferred to accumulator.
        :
        :
```

- INITIAL VALUE REGISTER / TIMER COUNTER {PHY4;(Y'=4)}

The Initial Value Register consisted of a 8-bit register sets the initial value to the Timer, or gets the counted value from the Timer.

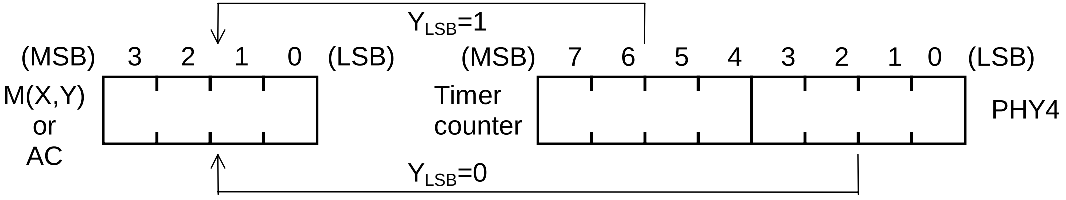
[Writing to Initial Value Register]

When a data in RAM or Accumulator is transferred to the Initial Value Register, the data is loaded into the higher 4-bit(b7 to b4) or lower(b3 to b0) of the Initial Value Register in accordance with the condition of LSB of Y-register.


Y_{LSB}=1
(MSB) 3 2 1 0 (LSB)
(MSB) 7 6 5 4 3 2 1 0 (LSB)
M(X,Y)
or
AC
Initial value
register
PHY4
Y_{LSB}=0

[Reading from Timer Counter]

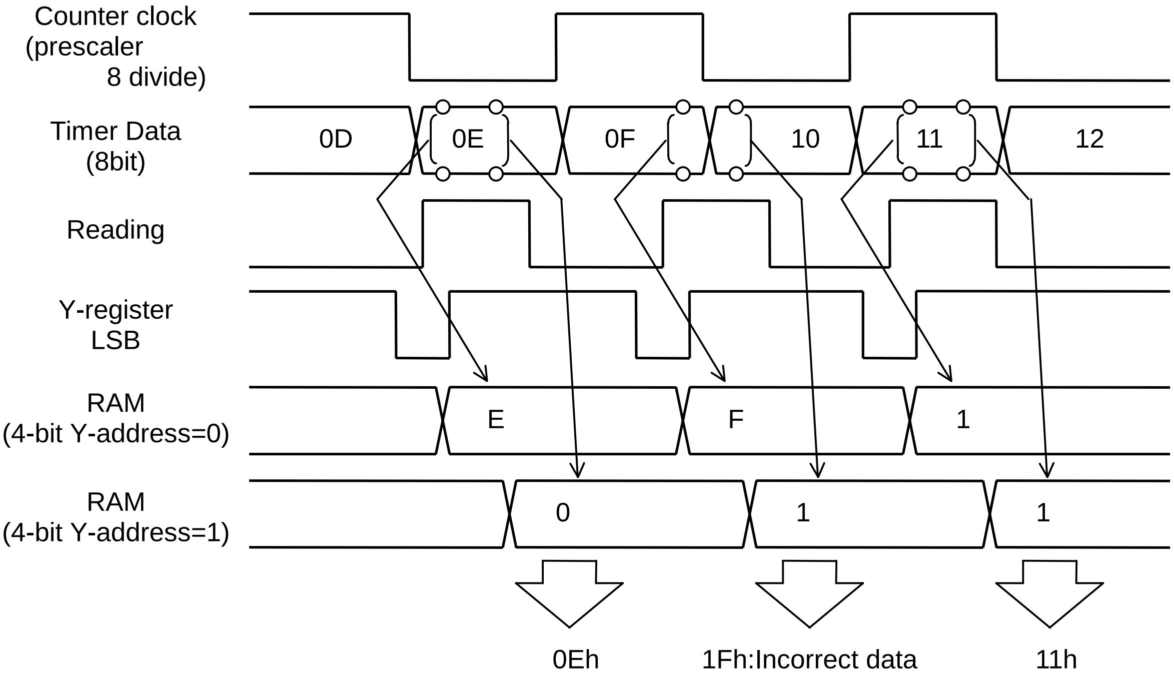
When a current data in the Timer Counter is transferred into RAM or Accumulator, the data is gotten from higher 4-bit(b7 to b4) or lower(b3 to b0) of the Timer Counter in accordance with the condition of LSB of Y-register.


Y_{LSB}=1
(MSB) 3 2 1 0 (LSB)
(MSB) 7 6 5 4 3 2 1 0 (LSB)
M(X,Y)
or
AC
Timer
counter
PHY4
Y_{LSB}=0

Though the data of Timer can be read in the count operation, the read data is sometimes incorrect when the clock inputs to the counter during the reading operation.

When the 8-bit counter data is read in count operation in the shown as following timing chart(An example of data reading from the counter to RAM), Timer often counts up between the first 4-bit data reading and the second. In case of the following chart, though the timer data is "0Fh" when the lower 4-bit data is gotten, it is "10h" when the higher 4-bit data is gotten. Therefore the final data becomes to be "1Fh".

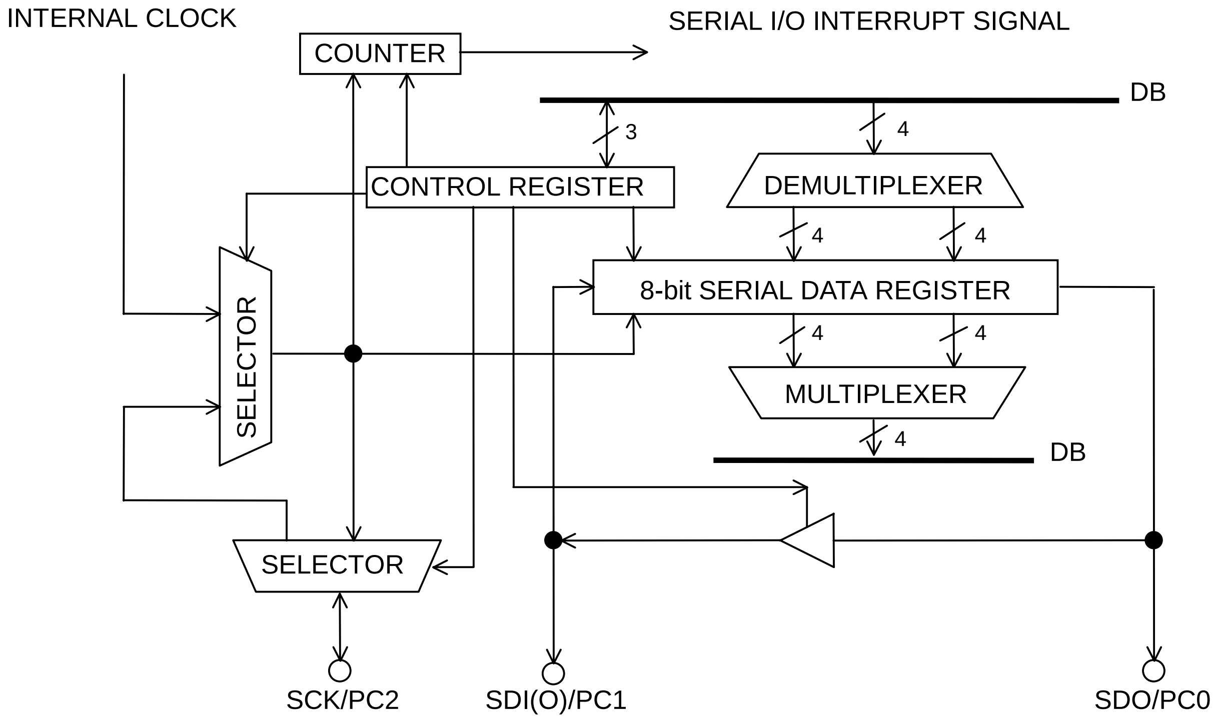
[An example of data reading from the counter to RAM]


Counter clock
(prescaler
8 divide)
Timer Data
(8bit)
0D
0E
0F
10
11
12
Reading
Y-register
LSB
RAM
(4-bit Y-address=0)
E
F
1
RAM
(4-bit Y-address=1)
0
1
1
0Eh
1Fh:Incorrect data
11h

■ SERIAL INPUT OUTPUT

SERIAL INPUT OUTPUT consists of the sift registers to convert from 8-bit parallel data to serial data, the 3-bit serial clock counter, and the 3-bit serial control register. It operates as the 8-bit serial input or output. The external or internal clock is selected as the shift clock in accordance with the Serial Input / Output control register.

[Block diagram of the SERIAL INPUT OUTPUT]


INTERNAL CLOCK
COUNTER
SERIAL I/O INTERRUPT SIGNAL
DB
3
4
CONTROL REGISTER
DEMULTIPLEXER
4
4
SELECTOR
8-bit SERIAL DATA REGISTER
4
4
MULTIPLEXER
4
DB
SELECTOR
SCK/PC2
SDI(O)/PC1
SDO/PC0

The serial input or output operation starts when the LSB of the Serial Input / Output control register(PHY1) is set to "1". In the external clock operation, the serial input or output operation waits to start until the external clock come in.

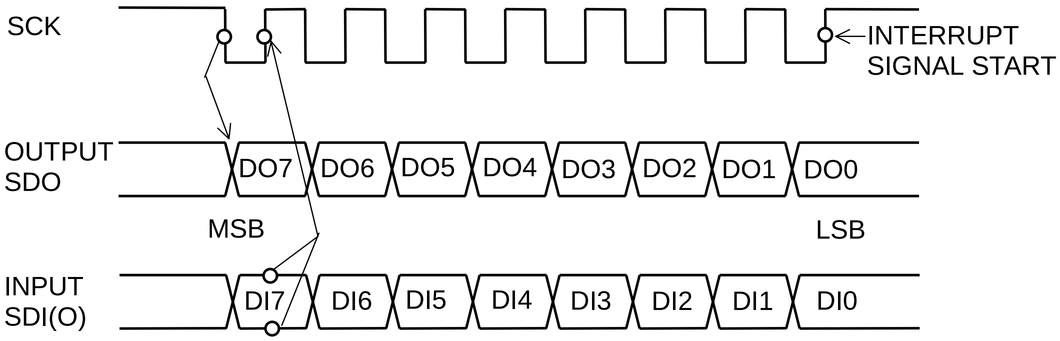
When the serial shift register(PHY2) is set the data in advance, the data is output(transmitted) through the SDO or the SDI(O) terminal. The SDI(O) terminal can be changed as a transmitter or a receiver in accordance with the bit3(b3) of PHY1. The data order, MSB or LSB first, is selected by the mask option.

Serial Input Output operates as the 3-wire method using SDI(O), SCK and SDO terminals, or the 2-wire using SDI(O) and SCK terminals.

<<The 3-wire method>>

The data synchronized with the falling edge of the SCK clock is output(transmitted) through the SDO terminal. The data synchronized with the rising edge of the SCK clock is input(received) through the SDI(O) terminal.

[The 3-wire transmission timing chart (MSB first)]

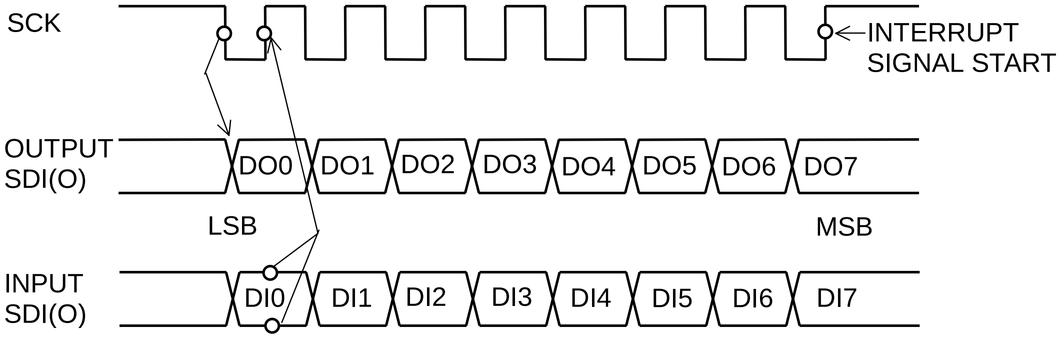

SCK
INTERRUPT
SIGNAL START
OUTPUT
SDO
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
MSB
LSB
INPUT
SDI(O)
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0

<<The 2-wire method>>

The data synchronized with the falling edge of the SCK clock is transmitted through the SDI(O) terminal. The data synchronized with the rising edge of the SCK clock is received through the SDI(O) terminal.

＊ In case of the data transmission through the SDI(O) terminal, the SDI(O) terminal must be set as the output by the condition of the bit3(b3) of the Serial Input / Output control register(PHY1) set to "1". In case of the data reception through the SDI(O) terminal, the SDI(O) terminal must be set as the input by the condition of the b3 of PHY1 set to "0".

[The 2-wire transmission timing chart (LSB first)]


SCK
INTERRUPT
SIGNAL START
OUTPUT
SDI(O)
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
LSB
MSB
INPUT
SDI(O)
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7

In case of the external clock operation, the external clock is input as the SCK clock to the SCK terminal as shown in the serial transmission timing chart. The signal condition into the SCK terminal must be kept as “HIGH” until the external clock come in. In the transmission, when the SCK with the noise or other redundant signals from the outside of **NJU3501** input to the SCK terminal, Serial Input Output operates incorrectly. The maximum frequency of the SCK is 500kHz.

In case of the internal clock operation, the SCK outputs through the SCK terminal as shown in the serial transmission timing chart. The internal interrupt signal occurs when the 3-bit counter has counted the SCK clock up to 8 times that means 1-byte serial data transmission end. The internal clock as the SCK is the divided clock in the internal prescaler, and the frequency of the clock can be selected by the mask option from follows which are dividing numbers based on the inverse of the 1-instruction executing period($1/f_{OSC}$ x 6).

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

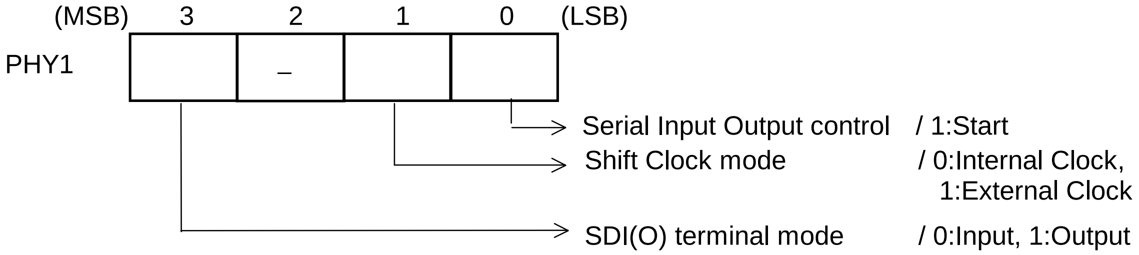
Remarks1) When the bit2(b2) of Timer / Prescaler control register(PHY3) is set to "1", the prescaler generating the internal serial clock is stopped and the internal serial clock is also stopped. Accordingly, Serial Input Output does not operate.

Remarks2) If the writing operation is operated to the Serial Input / Output shift register(PHY2) or the Serial Input / Output control register during the transmission or the reception operation, the 3-bit counter is reset and the serial data transmission or reception is stopped. Therefore the writing operation to the above registers must not be operated during the transmission or reception operation.

- Serial Input/Output control register {PHY1 ; (Y'=1)}

  When the data of bit1(b1) and bit3(b3) of the Serial Input / Output control register are changed, the operation must be performed before starting the serial transmission. (See the following sample program) In changing the condition of b1 or b2 of PHY1 and setting the LSB of PHY1 to start the transmission are operated in the mean time, Serial Input Output operation does not operate correctly.

[Writing to the Serial Input / Output Control Register]

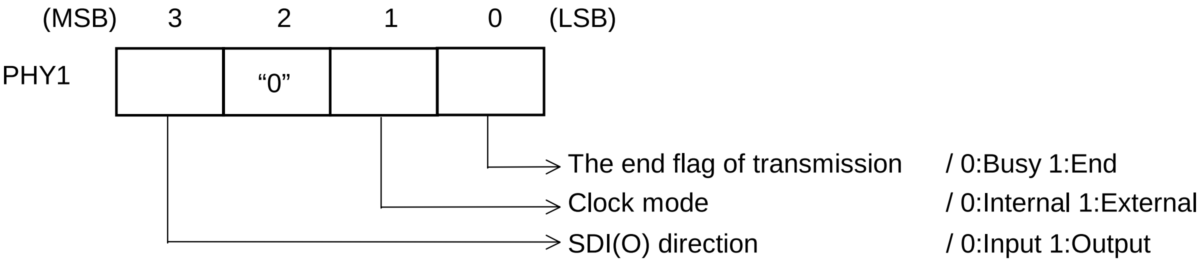

(MSB)
3
2
1
0
(LSB)
PHY1
–
Serial Input Output control / 1:Start
Shift Clock mode / 0:Internal Clock, 1:External Clock
SDI(O) terminal mode / 0:Input, 1:Output

EX.)An example of the start procedure in the 3-wire serial data transmission, the external clock operation and the SDI(O) terminal setting as the input .

```
         :
         :
SRPC                ;
LDI      Y,1        ;PHY1(Serial Input / Output control register) is pointed
LDI      A,%0010    ;"0010"(BIN) is stored to accumulator              ⎫ External clock,
TAP                 ;Data is transferred from accumulator to PHY1      ⎭ Input mode
LDI      A,%0011    ;"0011"(BIN) is stored to accumulator              ⎫ Transmission
TAP                 ;Data is transferred from accumulator to PHY1      ⎭ Starts.
         :
         :
```

Remarks3) In case of the external clock operation at the both of the transmission and reception mode, inputting the external clock must wait while the 2-instruction execution period after that LSB of Serial Input / Output control register is set to "1"(START). (one instruction execution period = 1 / f_{OSC} X 6)
If the external clock is input within the 2-instruction execution period, the Serial Input / Output shift register can not recognize the first SCK. The number of the shift operation is decreased a time, 8 times to 7.

[Reading from the Serial Input / Output Control Register]


(MSB)
3
2
1
0
(LSB)
PHY1
"0"
The end flag of transmission
/ 0:Busy 1:End
Clock mode
/ 0:Internal 1:External
SDI(O) direction
/ 0:Input 1:Output

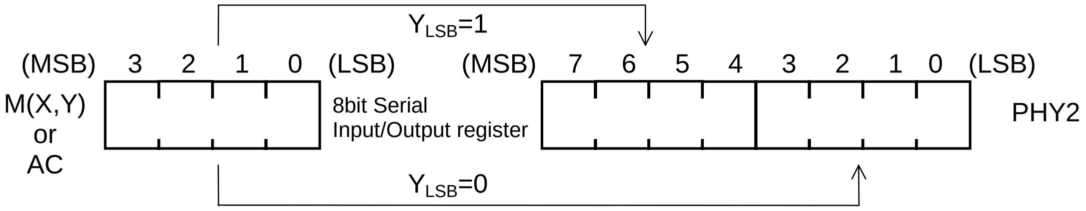
Remarks4) The end flag of transmission is set to "1" when the serial data(8 bits) transmission operation is ended. It is cleared by setting the serial data transmission start signal in the Serial Input /Output control register.

- Serial Input/Output Shift register {PHY2 ; (Y'=2)}

The Serial Input / Output Shift register consisted of a 8-bit register operates to set the transmission data or to get the reception data.

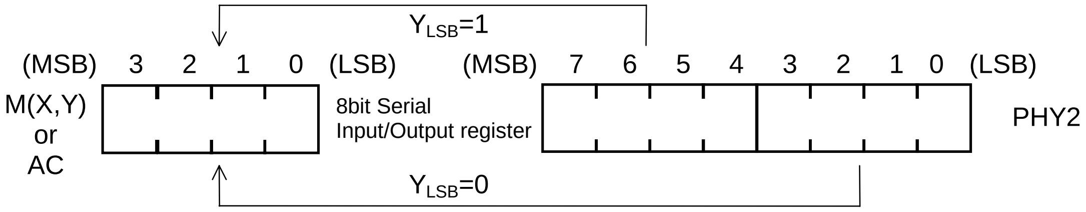
[Writing to the Serial Input / Output Shift Register]

The data in RAM or Accumulator is transferred to the Serial Input / Output Shift register, and it is loaded into lower 4-bit(b0 to b3) or higher(b4 to b7) in PHY2 in accordance with the condition of LSB of Y-register.


YLSB=1
(MSB)
3
2
1
0
(LSB)
(MSB)
7
6
5
4
3
2
1
0
(LSB)
M(X,Y)
or
AC
8bit Serial
Input/Output register
PHY2
YLSB=0

[Reading from the Serial Input / Output Shift Register]

The Serial Input data is transferred to RAM or Accumulator, it is loaded from lower 4-bit(b0 to b3) or higher(b4 to b7) of PHY2 in accordance with the condition of LSB of Y-register.


YLSB=1
(MSB)
3
2
1
0
(LSB)
(MSB)
7
6
5
4
3
2
1
0
(LSB)
M(X,Y)
or
AC
8bit Serial
Input/Output register
PHY2
YLSB=0

An example of the serial data reception program

In the internal clock operation, SDI(O) terminal is set as the input and the serial input data is transferred to RAM.

```
            :
            :
;---- Interrupt process ----
            ORG    $30              ;Interrupt vector address of FULL or EMPTY
SINT        SRPC                    ;
            LDI    Y,1              ;The Serial Input / Output control register is set
            TPA                     ;
            TBA    0                ;The end flag of transmission is tested
            JMP    SIO_OK           ;
            JMP    SINT_E           ;
;
SIO_OK      LDI    Y,2              ;The Serial Input / Output shift register is set
            RRPC                    ;RAM to store the serial input data is pointed
            LDI    X,SIO_DAT.X      ;RAM address, X=0
            LDI    Y,SIO_DAT.Y      ;RAM address, Y=0
            TPMICY                  ;The serial input data is transferred to RAM(lower 4-bit)
                                    ;      and Y-register is incremented
            TPMICY                  ;The serial input data is transferred to RAM(higher 4-bit)
                                    ;      and Y-register is incremented
;
SINT_E      RETI                    ; End of the interrupt process
;
;------ Serial data inputting process ------
SIO_IN      SRPC                        ;
            LDI    Y,1              ;The Serial Input / Output control register is set
            LDI    A,%0000          ;The internal clock operation is set and the SDI(O)
                                    ;      terminal is set as the input
            TAP                     ;
            LDI    A,%0001          ;The serial data reception is started
            TAP
;
            :
            :
            WSEG                    ;The RAM area is set
SIO_DAT     DS     2                ;The area to store the serial input data is secured
```

An example of the serial data transmitting program)

In the internal clock operation, the SDI(O) terminal is set as the output and the data in RAM is transmitted.

```
           :
           :
;---- Interrupt process ----
           ORG    $30             ;Interrupt vector address of FULL or EMPTY
SINT       SRPC                   ;
           LDI    Y,1             ;The Serial Input / Output control register is set
           TPA                    ;
           TBA    0               ;The end flag of transmission is tested
           JMP    SIO_OK          ;
           JMP    SINT_E          ;
;
SIO_OK     RRPC                   ;The end flag of transmission is set
           LDI    X,SIO_FLG.X     ;
           LDI    Y,SIO_FLG.Y     ;
           LDI    A,1             ;
           TAM                    ;
;
SINT_E     RETI                   ; End of the interrupt process
;
;------ Serial data transmitting process ------
SIO_OUT    SRPC   ;
           LDI    Y,2             ;The Serial Input / Output shift register is set
;
           RRPC                   ;RAM to store the serial output data is set
           LDI    X,SIO_DAT.X     ;RAM address, X=0
           LDI    Y,SIO_DAT.Y     ;RAM address, Y=1
           TMPICY                 ;The data in RAM is transferred to the Serial Input /
                                  ;     Output shift register(lower 4-bit)
                                  ;     and Y-register is incremented
           TMPICY                 ;The data in RAM is transferred to the Serial Input /
                                  ;     Output shift register(higher 4-bit)
                                  ;     & Increments Y
;
           SRPC                   ;
           LDI    Y,1             ;The Serial Input / Output control register is set
           LDI    A,%1000         ;The internal clock operation and the transmission
                                  ;    mode are set
           TAP                    ;
           LDI    A,%1001         ;The serial data transmitting operation is started
           TAP                    ;
;
           :
           :
           WSEG                   ;The RAM area
SIO_FLG    DS      1              ;The end flag of transmission
SIO_DAT    DS      2              ;The area to store the serial output data
```

INTERRUPT

The **NJU3501** prepares three kinds of the interrupt. The interrupt "enable" or "disable" is controlled by the program. The interrupt operates as single process and no multiple. However, when new interrupt request occurs during the other interrupt process, the request is kept, and then the new interrupt process starts after the prior interrupt process. The priority order of the interrupt is that the first is (1)External interrupt-1, the second is (2)Internal interrupt-1, and the third is (3)Internal interrupt-2, as shown bellow.

When the interrupt request flag is set by the own factor, the interrupt enabled by the interrupt control register(PHY5) stores the data of Program Counter, Accumulator, X-reg, X'-reg, Y-reg, Y'-reg, RPC, and STATUS into the STACK register, and sets the interrupt vector address into Program Counter, and then the interrupt process is started. The return from the interrupt process by "RETI" instruction resets the corresponded interrupt request flag, and regains the held data from STACK, and then the operation before the interrupt process is started continuously. When the interrupt control register disables the interrupt process, the interrupt request flag is not set.

[THE PRIORITY ORDER OF THREE FACTORS INTERRUPT]

Order	Interrupt factor	Vector Address(H:HEX)
(1)	External interrupt-1	10H
(2)	Internal interrupt-1 Timer Overflow	20H
(3)	Internal interrupt-2 Serial shift register Full/Empty	30H

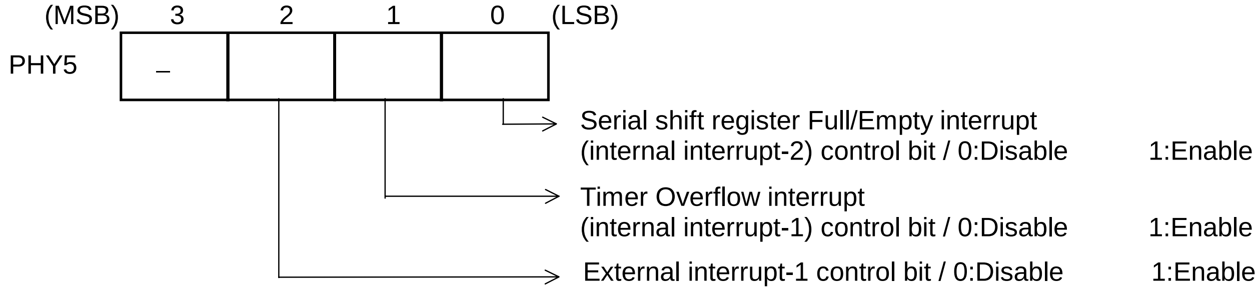
The External interrupt-1 enabled by PHY5 is started the interrupt process when the rising edge of signal pulse is input to the external interrupt signal input terminal(EXTI). The External interrupt-1 request flag is re-set by 'RETI' instruction. When the external interrupt-1 occurs during the standby mode by the HALT instruction, the External interrupt-1 request signal is latched and its interrupt process is started after that the standby mode is released.

The Internal interrupt enabled by PHY5 is started the interrupt process when the internal interrupt request flag is set.

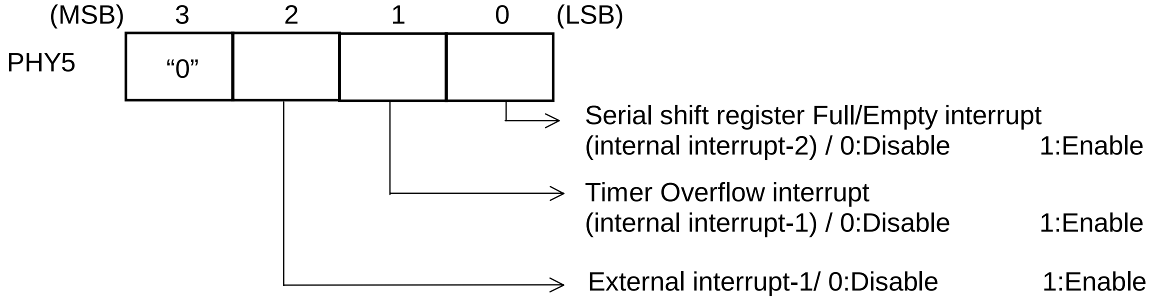
The Timer interrupt request flag is independent of the overflow flag, and it is reset by "RETI" instruction, (TIMER)START signal of the Timer control register, or RESET signal from the external circuit. Serial Input Output interrupt request flag is set synchronizing with the transmission end flag when its interrupt is enabled by PHY5. And the flag is reset by the "RETI" instruction or the RESET signal from the external circuit.

- INTERRUPT CONTROL REGISTER {PHY5 ; (Y'=5)}

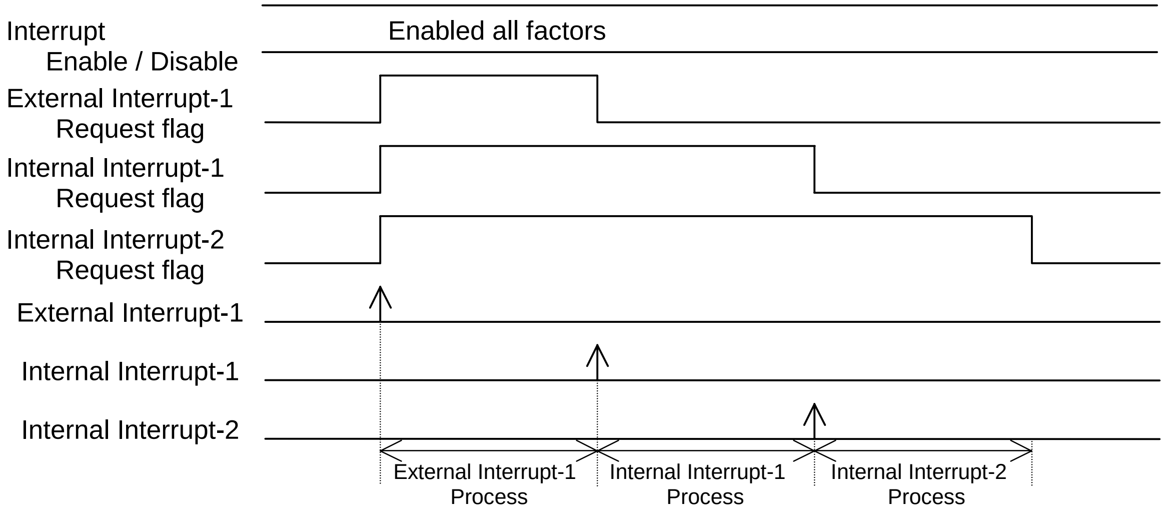
[Writing to the Interrupt Control Register]


(MSB)
3
2
1
0
(LSB)
PHY5
–
Serial shift register Full/Empty interrupt
(internal interrupt-2) control bit / 0:Disable 1:Enable
Timer Overflow interrupt
(internal interrupt-1) control bit / 0:Disable 1:Enable
External interrupt-1 control bit / 0:Disable 1:Enable

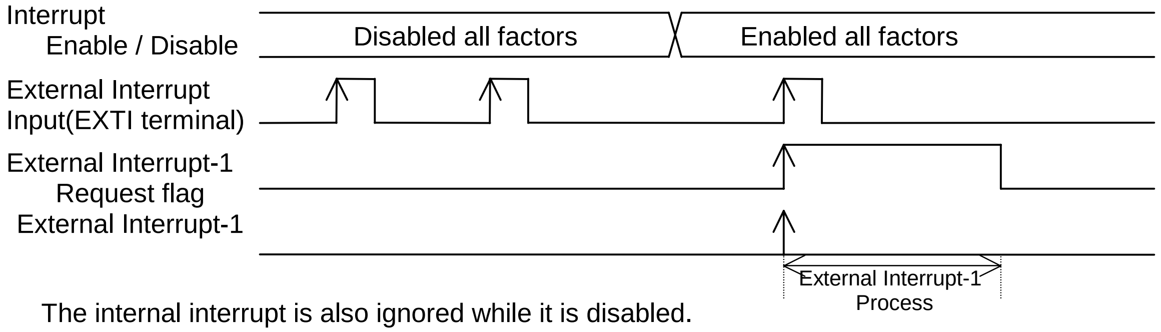
[Reading from the Interrupt Control Register]


(MSB)
3
2
1
0
(LSB)
PHY5
"0"
Serial shift register Full/Empty interrupt
(internal interrupt-2) / 0:Disable 1:Enable
Timer Overflow interrupt
(internal interrupt-1) / 0:Disable 1:Enable
External interrupt-1/ 0:Disable 1:Enable

[Enabled all factors (b0 to b2 of PHY5 were set to "1")]

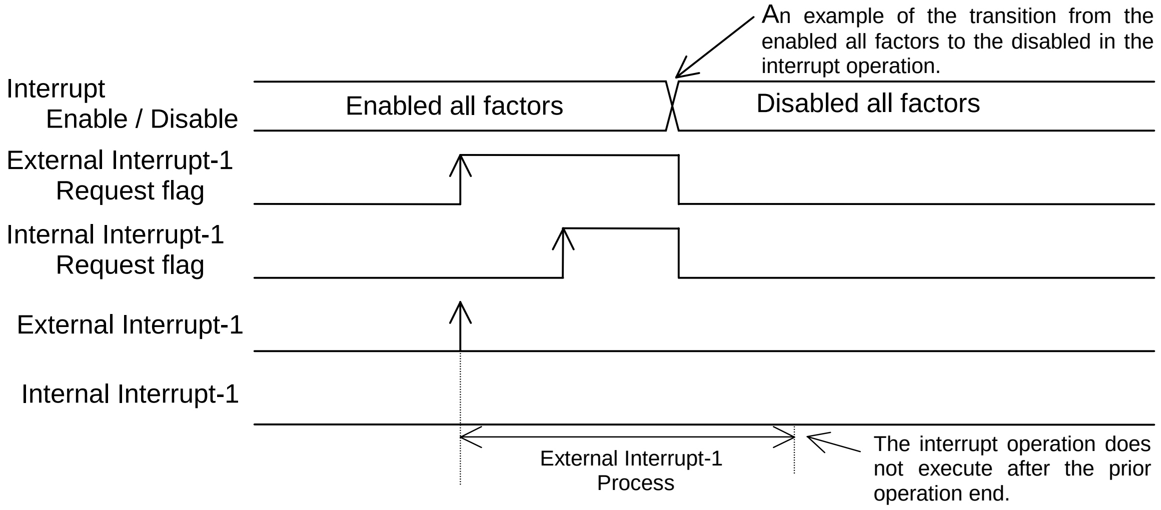

Interrupt
Enable / Disable
Enabled all factors
External Interrupt-1
Request flag
Internal Interrupt-1
Request flag
Internal Interrupt-2
Request flag
External Interrupt-1
Internal Interrupt-1
Internal Interrupt-2
External Interrupt-1
Process
Internal Interrupt-1
Process
Internal Interrupt-2
Process

[From the all factors disabled to the enabled (b0 to b2 of PHY5 are changed from "0" to "1")]


Interrupt
Enable / Disable
Disabled all factors
Enabled all factors
External Interrupt
Input(EXTI terminal)
External Interrupt-1
Request flag
External Interrupt-1
External Interrupt-1
Process

* The internal interrupt is also ignored while it is disabled.

[From the all factors enabled to the disabled (b0 to b2 of PHY5 are changed from "1" to "0")]


Interrupt
Enable / Disable
Enabled all factors
Disabled all factors
External Interrupt-1
Request flag
Internal Interrupt-1
Request flag
External Interrupt-1
Internal Interrupt-1
External Interrupt-1
Process

An example of the transition from the enabled all factors to the disabled in the interrupt operation.

The interrupt operation does not execute after the prior operation end.

* When the interrupt is enabled, the latest interrupt request occurred during the prior other interrupt process starts its interrupt process after the prior interrupt operation. However, when the interrupt is disabled during the prior interrupt process as shown in above timing chart, the latest interrupt request does not start. But the prior interrupt process is completed.

■ STANDBY FUNCTION

STANDBY FUNCTION halts the IC operation and reduces the current consumption.

The STANDBY function starts by the HLT instruction. After the HLT instruction execution cycle, the internal oscillator operation is stopped and all of the operation is halted. In case of the external clock operation, the clock is stopped automatically delivering into the internal system by the internal circuits, and all of the operation is halted as same as the internal oscillator operation. This is STANDBY mode.

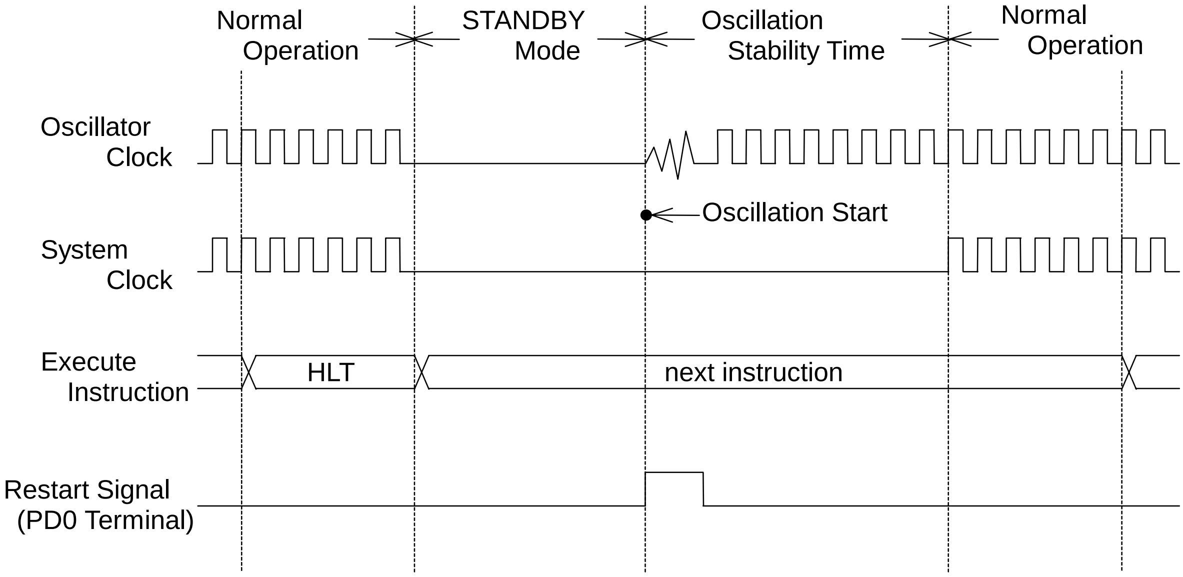
In the STANDBY mode, the operating current can be reduced. Though the clock into the internal system is stopped and all of the operation is halted, all conditions of Program Counter, Registers, and data in RAM are kept certainly.

Two ways to release from the STANDBY mode are prepared. One way is the reset operation that when the reset signal is input to RESET terminal, the operation starts from the initial condition. The other way is the restart operation that when the restart signal is input to PD0 terminal, the operation starts from the kept Program Counter location which is the program address after the final operation. In case of the restart signal operation, if the rising signal, low to high, is input to PD0 terminal, the internal oscillator circuit starts at first. After the stabilized clock from the internal oscillator was counted eight times, the clock is started delivering into the internal system. Then the NJU3501 starts to operate from the kept Program Counter location with all of the kept conditions.(See *1)

In case of the external clock operation, the external clock must be started to supply to the OSC1 terminal before the STANDBY mode is released. The external clock is recommended to stop supplying to the OSC1 terminal for reducing the power consumption during the STANDBY mode.

*1: When the restart signal is input to PD0 terminal to release the STANDBY mode, PORTD must be selected as the input by the mask option.

[STANDBY MODE TIMING CHART]



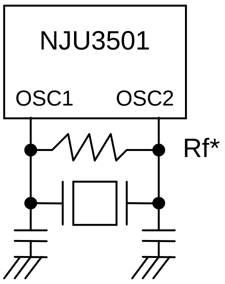
■ CLOCK GENERATION

The system clock is generated in the internal oscillator circuit using an external Crystal or Ceramic resonator, or the resistor connected to OSC1 and OSC2 terminals. Furthermore, the NJU3501 can operate by the external clock to the OSC1 terminal for the system clock. In the external clock operation, the OSC2 terminal must be opened.

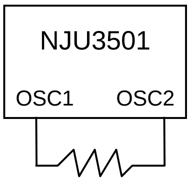
The typical application examples for each oscillator circuit are shown in follows. However a Crystal or a Ceramic operation requires the considered evaluation, because the oscillator operates in accordance with the characteristics of each component.

[OSCILLATOR APPLICATION EXAMPLES]

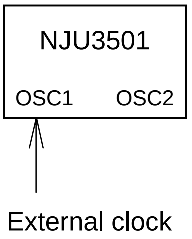
1) X'tal/Ceramic oscillation



2) CR oscillation



3) External clock input



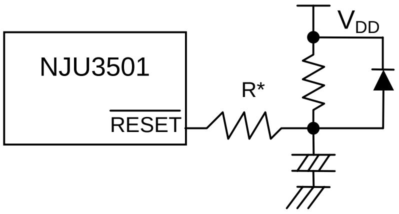
The resistor Rf* is sometimes required to connect when the Crystal operation.

■ RESET OPERATION

All of the internal circuits are initialized by inputting the low level signal to the RESET terminal.

A circuit example for Power On Reset Operation with a resistor, a capacitor, and a diode is shown in bellow. Power On Reset Operation requires to keep the low level of the input signal to RESET terminal until the stabilized oscillation of the internal oscillator. Therefore the constants on the reset circuit must be decided in accordance with the characteristics of the clock generator circuit.

[An example of Power On Reset circuit]



R*:A resistor as RESET terminal protector. It is required depending on the condition of an application.

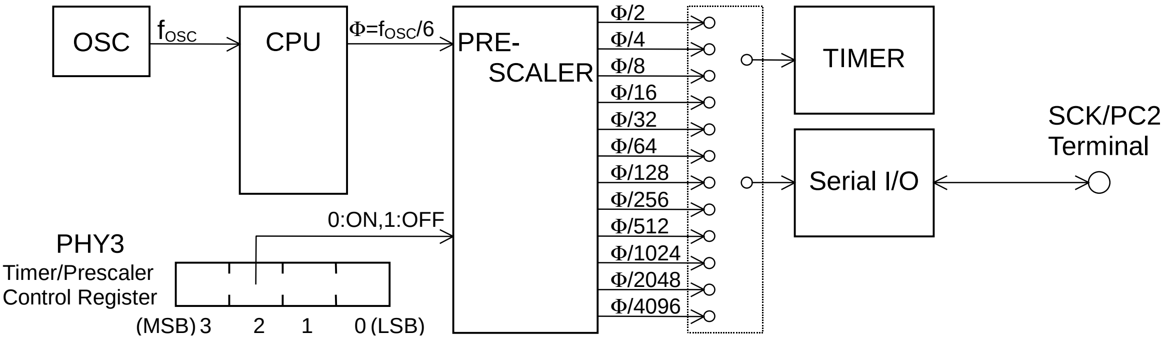
■ PRESCALER

The **NJU3501** prepares a built-in Prescaler consisted of 12-bit binary counter which counts the machine cycle period clock(1/f_{OSC} x 6) from 2 to 4096 times. The Prescaler can supply the clock to Timer, and Serial Input Output. A frequency of the clock can be selected from 12 kinds shown in follows.

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

When the bit2(b2) of Timer/Prescaler control register(PHY3) is set to "1", the Prescaler operation is stopped, but the output clock is also stopped to Timer and Serial Input Output. When the b2 of PHY3 is set to "0", the Prescaler operation is started to count from "0".

[AROUND THE PRESCALER BLOCK DIAGRAM]


OSC
fOSC
CPU
Φ=fOSC/6
PRE-
SCALER
Φ/2
Φ/4
Φ/8
Φ/16
Φ/32
Φ/64
Φ/128
Φ/256
Φ/512
Φ/1024
Φ/2048
Φ/4096
TIMER
Serial I/O
SCK/PC2
Terminal
0:ON,1:OFF
PHY3
Timer/Prescaler
Control Register
(MSB) 3
2
1
0 (LSB)

EX.)The output frequency of Prescaler at f_{OSC} = 4MHz (Φ=4MHz/6)

Prescaler Divider	Output Frequency
Φ/2	333.33kHz
Φ/4	166.67kHz
Φ/8	83.33kHz
Φ/16	41.67kHz
Φ/32	20.83kHz
Φ/64	10.42kHz
Φ/128	5.21kHz
Φ/256	2.60kHz
Φ/512	1.30kHz
Φ/1024	651kHz
Φ/2048	326kHz
Φ/4096	163kHz

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 – +7.0	V
Input Voltage	V_{IN}	-0.3 – V_{DD} + 0.3	V
Output Voltage	V_{OUT}	-0.3 – V_{DD} + 0.3	V
Operating Temperature	T_{opr}	-20 – +75	°C
Storage Temperature	T_{stg}	-55 – +125	°C

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 1

(V_{DD}=4.5–5.5V, V_{SS}=0V, Ta=-20–75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	3.6		5.5	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz X'tal Oscillation in Reset		2.0	4.0	mA	*3
	I_{DD2}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz Ceramic Oscillation in Reset		2.0	4.0	mA	*3
	I_{DD3}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz CR Oscillation in Reset		1.9	3.8	mA	*3
	I_{DD4}	V_{DD} V_{DD}=5V, STANDBY Mode			4.0	µA	*3
High-Level Input Voltage	V_{IH1}	PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0.7V_{DD}		V_{DD}	V	*1
	V_{IH2}	PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-1.0		V_{DD}	V	
Low-level Input Voltage	V_{IL1}	PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0		0.3V_{DD}	V	*1
	V_{IL2}	PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$	0		0.2V_{DD}	V	*1
	V_{IL3}	OSC1	0		1.0	V	
High-Level Input Current	I_{IH}	V_{DD}=5.5V, V_{IN}=5.5V PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$			10	µA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=5.5V, V_{IN}=0V Without pull-up resistance PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$			-10	µA	*1
	I_{IL2}	V_{DD}=5.5V, V_{IN}=0V With pull-up resistance PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0			-100	µA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-100µA PA0–PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=400µA PA0–PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1			0.5	V	*2
	V_{OL2}	I_{OL2}=15mA PB0–PB3			2.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=5.5V, V_{OH}=5.5V PB0–PB3			10	µA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz Other terminals : 0V		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 2

(V_{DD}=2.4–3.6V, V_{SS}=0V, Ta=-20–75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	2.4		3.6	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz X'tal Oscillation in Reset		1.0	2.0	mA	*3
	I_{DD2}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz Ceramic Oscillation in Reset		1.0	2.0	mA	*3
	I_{DD3}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz CR Oscillation in Reset		0.9	1.8	mA	*3
	I_{DD4}	V_{DD} V_{DD}=3V, STANDBY Mode			2.0	µA	*3
High-Level Input Voltage	V_{IH1}	PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0.8V_{DD}		V_{DD}	V	*1
	V_{IH2}	PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$	0.85V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-0.3		V_{DD}	V	
Low-level Input Voltage	V_{IL1}	PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0		0.2V_{DD}	V	*1
	V_{IL2}	PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$	0		0.15V_{DD}	V	*1
	V_{IL3}	OSC1	0		0.3	V	
High-Level Input Current	I_{IH}	V_{DD}=3.6V, V_{IN}=3.6V PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$			10	µA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=3.6V, V_{IN}=0V Without pull-up resistance PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{\text{RESET}}$			-10	µA	*1
	I_{IL2}	V_{DD}=3.6V, V_{IN}=0V With pull-up resistance PA0–PA3, PB0–PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0			-100	µA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-80µA PA0–PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=350µA PA0–PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1			0.5	V	*2
	V_{OL2}	I_{OL2}=5mA PB0–PB3			1.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=3.6V, V_{OH}=3.6V PB0–PB3			10	µA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz Other terminals : 0V		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

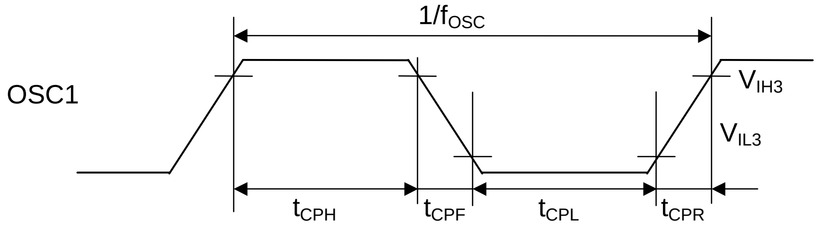
■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 1

(V_{SS}=0V, Ta= -20–75°C)

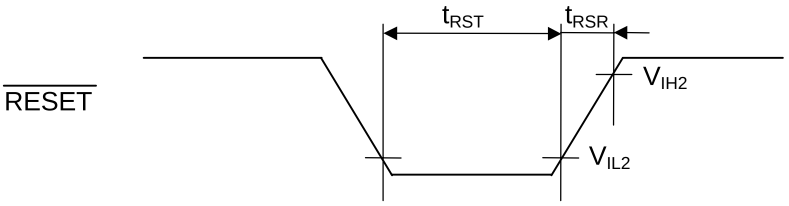
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Frequency	f_{OSC}	V_{DD}=2.4–3.6V	X'tal Resonator	0.03		2.0	MHz
			Ceramic Resonator	0.03		2.0	
			External Resistor Oscillation	0.03		1.0	
			External Clock	0.03		2.0	
		V_{DD}=3.6–5.5V	X'tal Resonator	0.03		4.0	
			Ceramic Resonator	0.03		4.0	
			External Resistor Oscillation	0.03		2.0	
			External Clock	0.03		4.0	
Instruction Cycle Time	t_C				6/f_{OSC}		s
External Clock Pulse Width	t_{CPH}	V_{DD}=2.4–3.6V		250		16600	ns
	t_{CPL}	V_{DD}=3.6–5.5V		125		16600	
External Clock Rise Time Fall Time	t_{CPR} t_{CPF}	V_{DD}=2.4–5.5V				20	ns
$\overline{\text{RESET}}$ Low-Level Width	t_{RST}	V_{DD}=2.4–5.5V		4/f_{OSC}			s
$\overline{\text{RESET}}$ Rise Time	t_{RSR}	V_{DD}=2.4–5.5V				20	ms
Port Input Level Width	t_{PIN}	V_{DD}=2.4–5.5V		6/f_{OSC}			s
Edge Detection (PD1) Rise Time Fall Time	t_{EDR} t_{EDF}	V_{DD}=2.4–5.5V				200	ns
Restart Signal (PD0) Rise Time	t_{STR}	V_{DD}=2.4–5.5V				200	ns
External interrupt input (EXTI) Rise Time	t_{EXR}	V_{DD}=2.4–5.5V				200	ns

■ AC CHARACTERISTICS 1 TIMING CHART

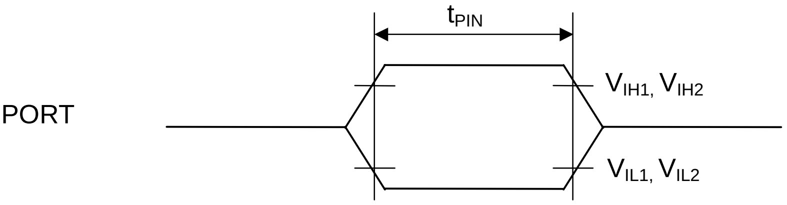
EXTERNAL CLOCK


1/fOSC
OSC1
VIH3
VIL3
tCPH
tCPF
tCPL
tCPR

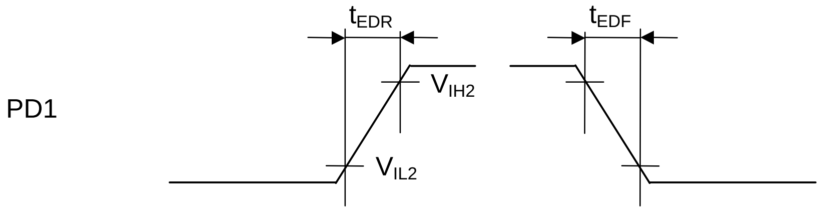
RESET INPUT


tRST
tRSR
RESET
VIH2
VIL2

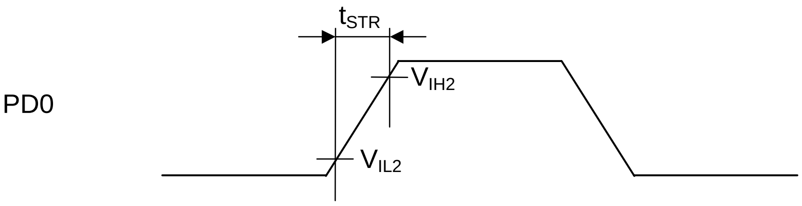
PORT INPUT


tPIN
PORT
VIH1, VIH2
VIL1, VIL2

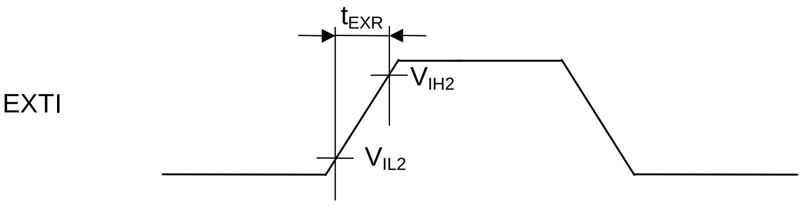
EDGE DETECTOR INPUT


tEDR
tEDF
PD1
VIH2
VIL2

RESTART SIGNAL INPUT


tSTR
PD0
VIH2
VIL2

EXTERNAL INTERRUPT


tEXR
EXTI
VIH2
VIL2

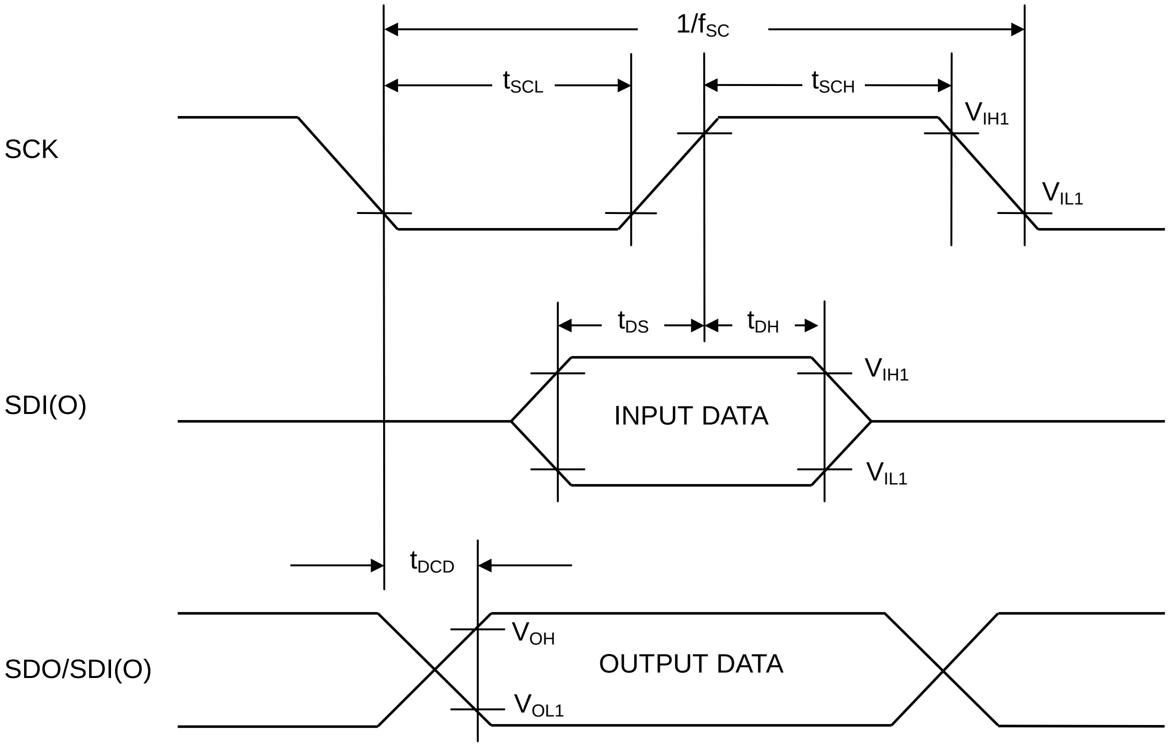
■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 2 SERIAL INTERFACE

(V_{SS}=0V, V_{DD}=2.4–5.5V, Ta=-20–75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Serial Operating Frequency	f_{SC}	Internal Clock				(1/12)×f_{OSC}*	Hz
		External Clock				500k	
Clock Pulse Width Low-Level	t_{SCL}	Internal Clock	V_{DD}=2.4–3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6–5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
Clock Pulse Width High-Level	t_{SCH}	Internal Clock	V_{DD}=2.4–3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6–5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
SDI setup Time To SCK	t_{DS}			0.5			µs
SDI Hold time To SCK	t_{DH}			0.5			µs
SDO Data Fix Time To SCK	t_{DCD}					0.5	µs

* The dividing ratio of the internal clock is 1/2.

■ AC CHARACTERISTICS 2 SERIAL INTERFACE TIMING CHART


1/fSC
tSCL
tSCH
SCK
VIH1
VIL1
tDS
tDH
SDI(O)
VIH1
INPUT DATA
VIL1
tDCD
SDO/SDI(O)
VOH
OUTPUT DATA
VOL1

■ OPTION as same as mask version

1) INPUT OUTPUT Terminal Selection

All of input-output terminals select a terminal type for each port from the following table by the mask option.

[CIRCUIT TYPE TABLE]

SYMBOL	TERMINAL TYPES					REMARKS	
	Input / Output Terminal*1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
PA0	IA IC	OB					
PA1	IA IC	OB					
PA2	IA IC	OB					
PA3	IA IC	OB					
PB0			C D				
PB1			C D				
PB2			C D				
PB3			C D				
SDO / PC0	IA IC	OB		SO	Serial data output	MSB LSB	MSB first LSB first
SDI(O) / PC1 *2	IA IC	OB		SD	Serial data input/output		
SCK / PC2 *2	IA IC	OB		SK	Serial clock input/output		
PD0	IB ID	OB			Restart signal input		
PD1	IB ID	OB			Edge detection	P N	Rise edge detection Fall edge detection
EXTI / PE0 *2	IB ID			EX	External interrupt input (EXTI)		

Note) The symbol in the above table is the same as in mask option generator software.

*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

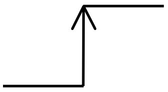
*2) The pull-up resistance is added to the terminal selected as the extra function.

2) Edge Detector Selection

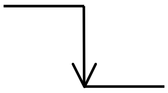
When the PORTD(PHY9) is set as the input, PD1 terminal operates as Edge Detector terminal. The result of the edge detection is set into bit(b2) of PORTD(PHY9).

The polarity of the edge, rising as “low to high” or falling as “high to low”, is selected by the mask option.

Rising edge



Falling edge



3) The data order(MSB, LSB) of the Serial Interface

The data order of the Serial Interface can select either MSB or LSB first by the mask option.

4) Each Internal Clock

The count clock of Timer, the Internal shift clock of the Serial Interface are clocks divided in the internal prescaler, and the frequency of this clock can be selected by the mask option from follows which are dividing numbers based on the inverse of the 1-instruction executing period(1/f_{OSC} x 6).

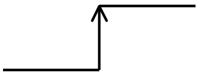
1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

Note) The shift clock of the serial interface can select the internal or external clock by the program.

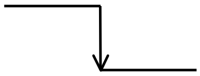
4) Edge Detector Selection

PD1 terminal is added the “Edge detect function” by the mask option.

Rising edge



Falling edge



5) The data order (MSB, LSB) of the Serial Interface

The data order of the Serial Interface is selected select either MSB or LSB first by the mask option.

6) Dividing ration of the internal clock

Each dividing ration of the count clocks of Timer, the Internal shift clock of the Serial Interface and the output clock through the SCK/CKOUT terminal is selected among the following by the mask option.

The frequency of each clock is determined by the dividing ration and the 1-instruction term (1/f_{OSC}x6).

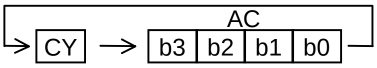
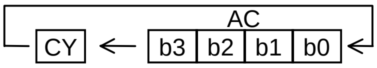
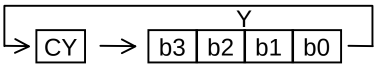
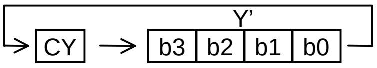
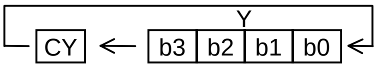
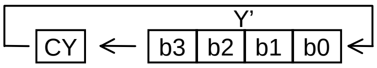
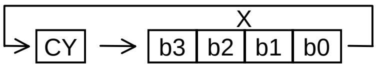
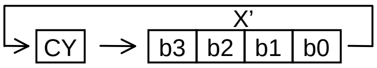
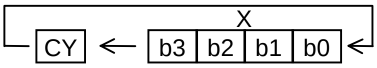
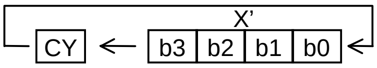
1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

Note) As the shift clock of the serial interface, the external clock or the internal is selected by the program.

Notes:

■ MNEMONIC LIST

	Mnemonic	Operation code	Function	Status	Cycle	Memo
DATA TRANSFERENCE	TAY	04	Y←AC	1	1	RPC=0
			Y'←AC	1	1	RPC=1
	TYA	14	AC←Y	1	1	RPC=0
			AC←Y'	1	1	RPC=1
	XAX	1B	AC↔X	1	1	RPC=0
			AC↔X'	1	1	RPC=1
	TAP	26	PH(Y')←AC	1	1	
	TPA	16	AC←PH(Y')	1	1	
	TAPICY	17	PH(Y')←AC, Y←Y+1	*	1	
	TAPDCY	27	PH(Y')←AC, Y←Y-1	*	1	
	TMA	0D	AC←M(X,Y)	1	1	
	TAM	1D	M(X,Y)←AC	1	1	
	TAMICY	0A	M(X,Y)←AC, Y←Y+1	*	1	
	TAMDCY	1A	M(X,Y)←AC, Y←Y-1	*	1	
	TMY	05	Y←M(X,Y)	1	1	RPC=0
			Y'←M(X,Y)	1	1	RPC=1
	XMA	0B	AC↔M(X,Y)	1	1	
	TPMICY	03	M(X,Y)←PH(Y'), Y←Y+1	*	1	
	TMPICY	13	PH(Y')←M(X,Y), Y←Y+1	*	1	
	TRM	23	M(X,Y)←ROM(PHY13,X',AC)	1	2	Y = an even number : ROM of 4bit low-data Y = an odd number : ROM of 4bit hi-data
	CLA	80	AC←0	1	1	
	LDI A,#K	80–8F	AC←#K	1	1	#K=0–15
	LDI Y,#K	90–9F	Y←#K	1	1	RPC=0, #K=0–15
			Y'←#K	1	1	RPC=1, #K=0–15
	LDI X,#K	A0–AF	X←#K	1	1	RPC=0, #K=0–15
			X'←#K	1	1	RPC=1, #K=0–15
CALCULATING	ADD A,M	0E	AC←AC+M(X,Y)	*	1	
	INC A	71	AC←AC+1	*	1	
	DEC A	7F	AC←AC-1	*	1	
	ADD A,#K	70–7F	AC←AC+#K	*	1	#K=0–15
	AND A,M	0F	AC←AC∧M(X,Y)	*	1	
	CMP A,M	2E	AC< >M(X,Y)	*	1	
	CMP Y,#K	B0–BF	Y< >#K	*	1	#K=0–15
	INC Y	08	Y←Y+1	*	1	RPC=0
			Y'←Y'+1	*	1	RPC=1
	DEC Y	18	Y←Y-1	*	1	RPC=0
			Y'←Y'-1	*	1	RPC=1
	INC M	09	AC←M(X,Y)+1	*	1	
	DEC M	19	AC←M(X,Y)-1	*	1	
	YNEA	01	Y< >AC	*	1	
	OR A,M	1F	AC←AC∨M(X,Y)	*	1	
	XOR A,M	2F	AC←AC⊕M(X,Y)	*	1	
	NEG	2D	AC←0-AC	1	1	
	SUB A,M	1E	AC←M(X,Y)-AC	*	1	
	AND A,#K	40–4F	AC←AC∧#K	*	1	#K=0–15
	OR A,#K	50–5F	AC←AC∨#K	*	1	#K=0–15

	Mnemonic	Operation code	Function	Status	Cycle	Memo
BRANCH	JPL addr	68–6F	ST=1:PC←addr, ST=0:No branch	1	2	2byte Mnemonic
	JMP addr	C0–FF	ST=1:PC←addr, ST=0:No branch	1	1	
	CALL addr	60–67	ST=1:(SP)←PC+2, SP←SP+1, PC←addr ST=0:No branch	1	2	2byte Mnemonic
	RET	2B	PC←(SP), SP←SP-1	1	1	
	RETI	2C	PC←(SP), AC←(SP), SP←SP-1 X←(SP), X'←(SP), Y←(SP), Y' ←(SP) RPC← (SP), ST← (SP)	∗	1	
BIT OPERATION	SBIT b	30–33	M(X,Y)b←1	1	1	B=0–3
	RBIT b	34–37	M(X,Y)b←0	1	1	B=0–3
	TBIT b	38–3B	ST←M(X,Y)b	∗	1	B=0–3
	TBA b	3C–3F	ST←(AC)b	∗	1	B=0–3
	RAR	21	 AC CY b3 b2 b1 b0	∗	1	
	RAL	22	 AC CY b3 b2 b1 b0	∗	1	
	RYR	24	 Y CY b3 b2 b1 b0	∗	1	RPC=0
			 Y' CY b3 b2 b1 b0	∗	1	RPC=1
	RYL	25	 Y CY b3 b2 b1 b0	∗	1	RPC=0
			 Y' CY b3 b2 b1 b0	∗	1	RPC=1
	RXR	28	 X CY b3 b2 b1 b0	∗	1	RPC=0
			 X' CY b3 b2 b1 b0	∗	1	RPC=1
	RXL	29	 X CY b3 b2 b1 b0	∗	1	RPC=0
			 X' CY b3 b2 b1 b0	∗	1	RPC=1
	SEC	0C	CY←1	1	1	
	CLC	1C	CY←0	0	1	
	SRPC	10	RPC←1	1	1	
	RRPC	20	RPC←0	1	1	
SPECIAL	NOP	00	No Operation	1	1	
	HLT	07	CPU Halted	1	1	
	MDT	06	Memory Dump Test	–	–	

Note)

←	:Transfer direction	AC	:Accumulator	SP	:Stack pointer
∧	:AND	X	:Xregister	RPC	:RPC flag
∨	:OR	X'	:X'register	CY	:Carry flag
⊕	:Exclusive OR	Y	:Yregister	ST	:Status flag
+	:Add	Y'	:Y'register	#K	:Immediate data
-	:Subtraction	PH	:Peripheral register	addr	:Blanch address
< >	:Comparison	M	:Data memory	( )	:A content of register or memory pointed by the address indicated in ( ).
		ROM	:Program memory		
		PC	:Program counter	b	:Bit position

Status description)

0:After the command execution, ST-flag is always set to “0”.
1:After the command execution, ST-flag is always set to “1”.
∗:Status

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