NEC

35 W C-BAND POWER GaAs MESFET | NEZ5964-35E

FEATURES

- **HIGH OUTPUT POWER:** 35 W TYP
- **HIGH LINEAR GAIN:** 10 dB TYP
- **HIGH POWER ADDED EFFICIENCY:** 40% TYP
- **INTERNALLY MATCHED (IN/OUT)**

DESCRIPTION

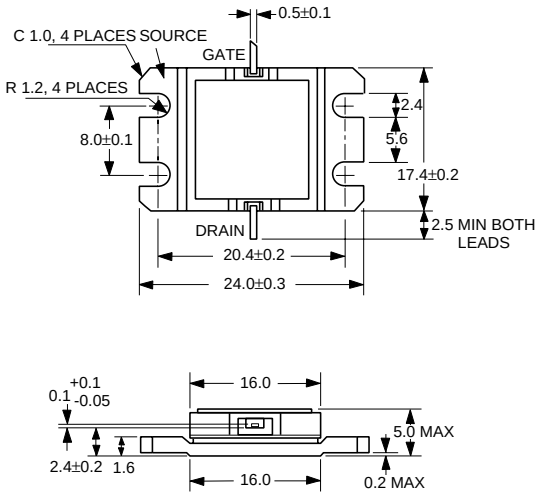
The NEZ5964-35E is a 35 W GaAs MESFET designed for high output power and high gain at C-band for VSAT and microwave communications. It is capable of delivering 35 W of output power (CW) with high linear gain, high efficiency, and excellent linearity.

The device employs a Tungsten Silicide gate structure, via holes, plated heat sink, and silicon dioxide and nitride passivation for superior performance, thermal characteristics, and reliability.

Reliability and performance uniformity are assured by NEC's stringent quality and control procedures.

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE T-65



ELECTRICAL CHARACTERISTICS (T_C = 25°C)

PART NUMBER			NEZ5964-35E			
SYMBOLS	**CHARACTERISTICS**	**UNITS**	**MIN**	**TYP**	**MAX**	**TEST CONDITIONS**
I_{DSS}	Saturated Drain Current	A		20		V_{DS} = 2.5 V, V_{GS} = 0 V
V_P	Pinch-off Voltage	V	-4.0	-2.5		V_{DS} = 2.5 V, I_{DS} = 90 mA
R_{TH}	Thermal Resistance	°C/W		1.0	1.2	Channel to Case
G_L	Linear Gain	dB	9.0	10		P_{IN} = 29 dBm
P_{-1dB}	Output Power	dBm	45.0	45.5		V_{DS} = 10 V f = 5.9 to 6.45 GHz I_{DSQ} = 8 A (RF OFF) R_G = 25 Ω
I_D	Drain Current	A		8	9.5	
η_{ADD}	Power Added Efficiency	%		40		

ABSOLUTE MAXIMUM RATINGS[1]

(T_C = 25 °C unless otherwise noted)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DS}	Drain to Source Voltage	V	15
V_{GS}	Gate to Source Voltage	V	-7
V_{GD}	Gate to Drain Voltage	V	-18
I_{DS}	Drain Current	A	20
I_G	Gate Current	mA	180
P_T	Total Power Dissipation	W	115
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Note:

1. Operation in excess of any one of these parameters may result in permanent damage.

RECOMMENDED OPERATING LIMITS

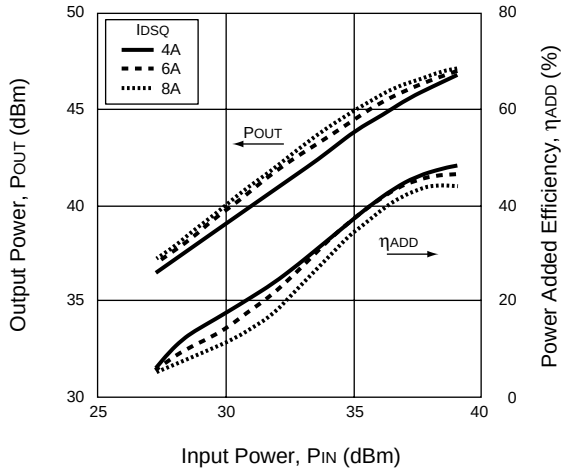
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{DS}	Drain to Source Voltage	V		10	10
G_{COMP}	Gain Compression	dB			3
T_{CH}	Channel Temperature	°C			+150
R_G	Gate Resistance[1]	Ω		25	

Note:

1. R_G is the series resistance between the gate supply and the FET gate.

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER



THIRD ORDER INTERMODULATION DISTORTION vs. TOTAL OUTPUT POWER