National Semiconductor

PRELIMINARY
August 1995

NCL354
Cordless Telephone IC

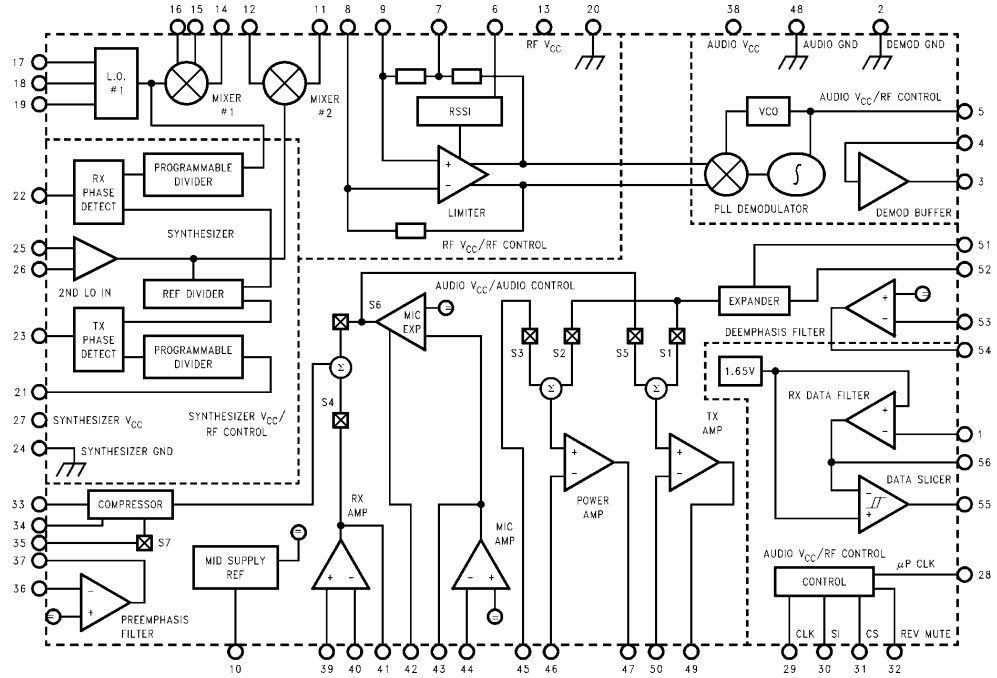
General Description

The NCL354 combines a high performance, dual conversion superheterodyne VHF radio receiver with the audio processing functions required to build a full featured narrow band FM cordless telephone system. Superior RF sensitivity, combined with advanced audio channel signal pre-emphasis/de-emphasis and compression/expansion processing, creates a high performance communications system with excellent noise characteristics and wide dynamic range. The built-in receive signal strength indicator (RSSI) allows for easy identification of channels which are not suitable for use or monitoring of the signal strength on the selected channel. A built-in phase locked loop (PLL) discriminator provides for low distortion demodulation of signals which have a wide dynamic range while eliminating the need for external adjustments. A microphone expander circuit reduces the transmitted background noise during silent periods, and enhanced power supply management techniques extend battery life. The audio portion includes digitally selected analog switches which allow the designer to easily incorporate speaker-phone and intercom features.

Features

- Low supply voltage 3V–5V
- Dual conversion receiver 46 MHz/49 MHz
- Companded audio channel 60 dB
- Microphone expander
- PLL discriminator
- Receive signal strength indicator for channel selection
- Highly selective filter for data reception
- Speaker phone and intercom capabilities
- Universal transmit and receive frequency synthesizers
- Battery saving features:
  - I_{CC} = 50 μA in standby state
  - I_{CC} = 5.5 mA in sniff mode
  - I_{CC} = 13 mA in communication mode
- Available in 56-pin TSSOP package

NCL354 Block Diagram



TL/W/12474–1

TRI-STATE® is a Registered Trademark of National Semiconductor Corporation.

RRD-B30M115/Printed in U. S. A.

1.0 Pin Names and Functions

Function	Name	Note	Pin #
RF Power	VCCRF		13
RF Ground	RFGND		20
Audio Power	VCCAUD		38
Audio Ground	AUDGND		48
Synthesizer Power	VCCSYNTH		27
Synthesizer GND	SYNTHGND		24
Demodulator Buffer Out	DMDOUT		3
Demodulator Buffer In	DMDIN		4
Demodulator Loop Filter	DMDFILT		5
Demodulator Ground	DMDGND		2
Expander Input	EXPIN		52
Expand Filter Cap	EXPCAP	C_{ext} = 2.2 μF	51
Deemphasis In	DEEMIN		53
Deemphasis Out	DEEMOUT		54
Data Filter In	DFIN		1
Data Filter Out	DFOUT		56
Data Slicer Out	RXDATA		55
Chip Select	CS	Active Hi, CMOS Levs	31
Serial In	SI	CMOS Levs	30
Serial Clock	CLKIN	CMOS Levs	29
Clock Out	CLKOUT	CMOS Levs	28
Receive Mute	RCVMUT	CMOS Levs	32
Hyb TX Amp + Out	HYTXOTP		49
Hyb TX Amp − In	HYTXIN		50
Auxilliary Amp Out	PAOUT		47
Auxilliary Amp − In	PAIN		46
Mic Amp − In	MICIN		44
Mic Amp Out	MICOUT		43

Function	Name	Note	Pin #
Speakerphone RX	SPKPHRX		45
Hybrid RX Amp Out	HYRXOUT		41
Hybrid RX Amp − In	HYRXINN		40
Hybrid RX Amp + In	HYRXINP		39
Mic Expander Filter Cap	MEXPCAP	C_{ext} = 0.4 μF	42
Int. Reference Bypass	IREFBYP	C_{ext} = 0.1 μF	10
Preemphasis − In	PREEMIN		36
Preemphasis Out	PREEMOT		37
Compressor Output	COMPOUT		33
Compressor Filter Cap	COMPCAP	C_{ext} = 2.2 μF	34
Compressor Error Cap	CPERCAP	C_{ext} = 1 μF	35
LO1	LO1A		17
LO1	LO1B		19
Varactor	VARAC		18
Mixer1 RF In1	MX1RFIN1		16
Mixer1 RF In2	MX1RFIN2		15
Mixer1 Out	MX1OUT		14
Mixer2 RF In	MX2RFIN		12
Mixer2 Out	MX2OUT		11
Limiter + In	LIMINP		9
Limiter − In	LIMINN		8
Limiter Bypass	LIMBYP		7
RSSI	RSSI		6
LO2 IN	LO2IN		25
LO2 OUT	LO2OUT	CMOS Levs	26
Receive Loop Phase Det	RXPD		22
Transmit Loop Phase Det	TXPD		23
Transmit RF In	TXRFIN		21
TOTAL			56

Frequency Synthesizer

The frequency synthesizer architecture (shown in *Figure 1*) uses two phase-locked loops to generate transmit and receive mix frequencies for most country channels; including US (25ch), China, Spain, France, Korea, New Zealand, U.K., Netherlands, and Australia. The frequencies are programmed through the microprocessor serial interface and a on board ROM. The 2nd LO and reference divider provides the reference frequencies for both transmit and receive loops. This synthesizer contains separate 14-bit dividers and phase detectors for each loop. In addition, the varactor for the 1st LO is on chip with two pins for connection to an external tank circuit.

Power Management

To maximize battery life, the NCL354 handset has 2 power down modes of operation. In Standby mode, all power is turned off except for the data registers so that logic control states are preserved. Power down is done in a manner that preserves the charge in all external capacitors. This minimizes the cycle time needed to restore operation, and eliminates the current needed to recharge the capacitors. Standby current is < 50 μA. In Sniff mode only those circuits needed to detect an incoming ring signal are turned on. This includes the RF section, Receive Synthesizer, and Data detector. In this mode, supply current is < 5.5 mA.

1.0 Pin Names and Functions (Continued)

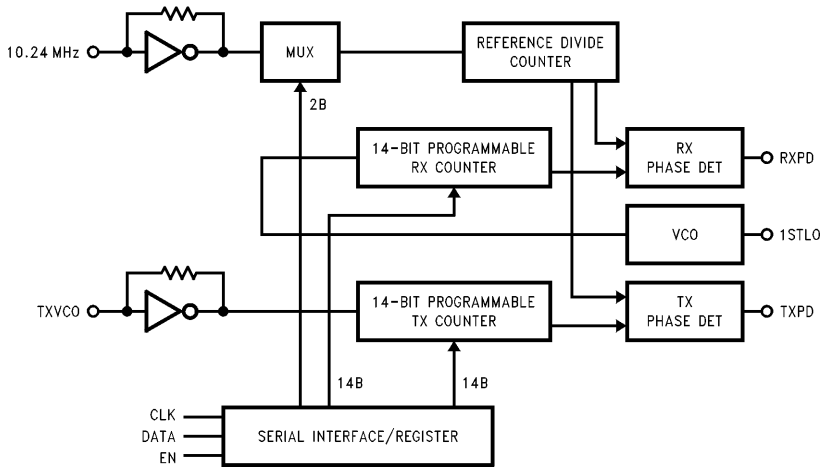


FIGURE 1. Block Diagram of Serial Interface and Frequency Synthesizer

2.0 Receiver System Characteristics (1st and 2nd IF Mixers, Limiter, RSSI, and PLL)

$T_A = 25°C$, RF $V_{CC} = 3.3\ V_{DC}$, $f_O = 50$ MHz, $\Delta f_O = \pm 1.0$ kHz, C Message Weight, fmod = 1.0 kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
P_{SIN}	RF Input for 12 dB SINAD	Measured @ Deemphasis Out Matched Input, w/C-message Weighting RF $V_{CC} \geq 3.0\ V_{DC}$		−110		dBm
THD	Total Harmonic Distortion			0.1	1.5	%
BW_{DEMOD}	Demodulation Bandwidth		20			kHz
	Ultimate Quieting	Measured @ Deemphasis Out w/C-message Weighting fmod = 1 kHz fdev = 1 kHz		35		dB
	AM to PM Conversion	Measured @ Deemphasis Out RF = −60 dBm, AM = 30% fmod = 1 kHz		−30	−20	dB

3.0 Electrical Specifications

3.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristic	Maximum	Units
RF V_{CC}	RF Supply Voltage	5.5	V_{DC}
AUDIO V_{CC}	Audio Supply Voltage	5.5	V_{DC}
T_J	Junction Temperature	150	°C
T_{STJ}	Storage Temperature	−50 to +150	°C

3.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	Min	Typ	Max	Units
RF V_{CC}	RF Supply Voltage	3.0		5.0	V_{DC}
AUDIO V_{CC}	Audio Supply Voltage (Base)	3.0		5.0	V_{DC}
AUDIO V_{CC}	Audio Supply Voltage (Handset)	3.0		5.0	V_{DC}
T_A	Ambient Operating Temperature Range	−30	+25	+80	°C
F_{RF}	RF Input Frequency		49	80	MHz
F_{if1}	Maximum 1st IF		10.7	23	MHz
F_{if2}	Maximum 2nd IF		0.455	3	MHz

3.3 RECEIVER CHARACTERISTICS (1st and 2nd IF Mixers, Limiter, RSSI, and PLL)

$T_A = 25°C$, RF $V_{CC} = 3.3\ V_{DC}$, $f_O = 50$ MHz, $\Delta f_O = \pm 1.0$ kHz, C Message Weight, $f_{mod} = 1.0$ kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
I_{CC}	Drain Current	No Input Signal, RF V_{CC} Enabled		4.2		mAdc
I_{CC}	Drain Current	No Input Signal, RF V_{CC} Disabled		20	100	μAdc

3.3.1 1st Mixer Characteristics $T_A = 25°C$, RF $V_{CC} = 3.3\ V_{DC}$, $f_{rf} = 50$ MHz, $f_{lo} = 40$ MHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
G_{MC1}	1st Mixer Conversion Voltage Gain	Loaded by 330Ω $f_{rf} = 50$ MHz $f_{lo} = 40$ MHz	11	15		dB
Z_{out1st}	1st Mixer Output Impedance	$f_O = 10$ MHz		330		Ω
Z_{in1st}	1st Mixer RF Input Impedance	$f_{rf} = 50$ MHz		2k		kΩ
V_{n1stm}	1st Mixer Input Noise Voltage	Referenced to 1st Mixer Input as an Amplifier		14		$nV/\sqrt{Hz}$
	1st Mixer LO Output Feedthrough	Measured @ 1st Mixer Output		28		dB
	1st Mixer LO Input Feedthrough	Measured @ 1st Mixer Input		28		dB
I_{P3m1}	1st Mixer 3rd Order Intercept	Referenced to 1st Mixer Input		30		mVrms
	1st Mixer 1dB Compression Point	Referenced to 1st Mixer Input		10		mVrms

3.0 Electrical Specifications (Continued)

3.3.2 2nd Mixer Characteristics $T_A = 25°C$, RF $V_{CC} = 3.3\ V_{DC}$, $f_{rf} = 10.695$ MHz, $f_{lo} = 10.24$ MHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
ZinRF2nd	2nd Mixer RF Input Impedance	$f_{rf} = 10.695$ MHz		330		Ω
Zout2nd	2nd Mixer Output Impedance	$f_O = 455$ kHz		1.5		kΩ
GMC2	2nd Mixer Conversion Voltage Gain	Loaded by 1.5 kΩ $f_{rf} = 10.695$ MHz $f_{lo} = 10.24$ MHz	10	15		dB
ZinLO2nd	2nd Mixer LO Input Impedance	$f_{lo} = 10.24$ MHz	20k			Ω
Vn2ndM	2nd Mixer Noise Voltage	Referenced to 2nd Mixer Input as an Amplifier		9		$nV/\sqrt{Hz}$
	2nd Mixer LO Output Feedthrough	Measured @ 2nd Mixer Output		40		dB
	2nd Mixer LO Input Feedthrough	Measured @ 2nd Mixer Input		40		dB
IP3m2	2nd Mixer 3rd Order Intercept	Referenced to 2nd Mixer Input		30		mVrms
	2nd Mixer 1 dB Compression Point	Referenced to 2nd Mixer Input		10		mVrms

3.3.3 Limiter Characteristics $T_A = 25°C$, RF $V_{CC} = 3.3\ V_{DC}$, $f_O = 455$ kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
	Limiter Voltage Gain			90		dB
	Limiter Input Noise Voltage	Referenced to Limiter Input		20		$nV/\sqrt{Hz}$
	Limiter Output Voltage Swing			400		mV_{PP}
BWlim	Limiter −3 dB Bandwidth			2		MHz
SENSlmt	Limiter Sensitivity	For 12 dB sinad @ DEOUT		25		μVrms

3.3.4 RSSI Characteristics $T_A = 25°C$, RF $V_{CC} = 3.3\ V_{DC}$, $f_O = 455$ kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
DRRSSI	RSSI Dynamic Range (Logarithmic Response)			60		dB
	RSSI Voltage Output	Limiter in = 10 μVrms Limiter in = 10 mVrms		0.2 1.2		V
	RSSI Attack Time				100	μs
	RSSI Decay Time				100	μs

3.3.5 PLL Demodulator Characteristics
$T_A = 25°C$, Audio $V_{CC} = 3.3\ V_{DC}$, $f_O = 455$ kHz, $\Delta f_O = \pm 1.0$ kHz, C Message Weight, $f_{mod} = 1.0$ kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
ko	VCO Gain			100		kHz/V
kd	Phase Detector Gain			0.20		μA/□
kv	PLL Open Loop Gain			360×10^3		1/s
f_c	VCO Center Frequency	Open Loop	398	455	512	kHz

3.0 Electrical Specifications (Continued)

3.4 AUDIO CHARACTERISTICS $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
Audio V_{CC} Enabled	Drain Current	I_{CCA}		8		mAdc
Audio V_{CC} Disabled	Drain Current	I_{CCA}		20	100	μAdc
From Enable Transition	Audio Switch Time	$t_{S1 \ldots S7}$			0.5	ms
	Audio Switch Isolation	$I_{S1 \ldots S7}$	65			dB
	Audio Switch Loss	L_{SW}			0.5	dB

3.4.1 Compressor Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	$V_{IN} \leq V_{IMAX}$ @ 1 kHz		0.5	1.0	%
G_{CO}	0 dB Gain	$V_{IN} = 90$ mVrms	−1.5	0	1.5	dB
t_{Ca}	Attack Time	G_{CO}, COMPCAP = 2.2 μF		6		ms
t_{Cd}	Decay Time	G_{CO}, COMPCAP = 2.2 μF		22		ms
G_T	Gain Tracking Linearity	11 dB > G_C > −20 dB	−2		+2	dB
PBW	Power Bandwidth	Unity Gain	10			kHz
DR_{IN}	Input Dynamic Range		−40		+22	dB
DR_{OUT}	Output Dynamic Range		−20		+11	dB
Vimax	Maximum Input Voltage Swing	$f_O = 1$ kHz		$V_{CC} - 0.4$	$V_{CC} - 0.2$	V_{PP}
Vomax	Maximum Output Voltage Swing	$f_O = 1$ kHz	$V_{CC} - 2.0$	$V_{CC} - 1.6$		V_{PP}
f_{lo}	Low Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB, CPERCAP = 1.0 μF $V_{IN} = G_{C0}$			180	Hz
f_{hi}	High Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB	4			kHz

3.4.2 Expander Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	$V_O \leq$ Vomax @ 1 kHz		0.5	1.0	%
G_{EO}	0 dB Gain	$V_{IN} = 90$ mVrms	−7.5	−6	−4.5	dB
t_{Ea}	Attack Time	G_{EO}, EXPCAP = 2.2 μF		19		ms
t_{Ed}	Decay Time	G_{EO}, EXPCAP = 2.2 μF		22		ms
G_T	Gain Tracking Linearity	11 dB > G_E > −20 dB	−2		+2	dB
PBW	Power Bandwidth	Unity Gain	10			kHz
DR_{IN}	Input Dynamic Range		−20		+11	dB
DR_{OUT}	Output Dynamic Range		−46		+16	dB
Vimax	Maximum Input Voltage Swing	$f_O = 1$ kHz		$V_{CC} - 0.4$	$V_{CC} - 1.6$	V_{PP}
Vomax	Maximum Output Voltage Swing	$f_O = 1$ kHz	$V_{CC} - 2.0$			V_{PP}
f_{lo}	Low Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB			180	Hz
f_{hi}	High Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB $V_{IN} = G_{C0}$	4			kHz

3.0 Electrical Specifications (Continued)

3.4.3 Deemphasis Filter Op Amp Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain		$2 \times R_L$			V/V
GBW	Gain-Bandwidth Product			200		kHz
Vinmax	Maximum Input Voltage Swing	$A_{CL} = 10$ dB			$V_{CC} - 1.6$	V_{PP}
Voutmax	Maximum Output Voltage Swing	$A_{CL} = 10$ dB	$V_{CC} - 2.0$			V_{PP}
I_B	Input Bias Current				200	nA
Requiv	Equivalent External DC Resistance for Minimal Input Offset to Expander			13.2		kΩ

3.4.4 TX Amplifier Characteristics $T_A = 25°C$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			200		kHz
T_D	Total Distortion	$f_O = 4$ kHz		0.5	1.0	%
Handset Application, Inductive Earpiece, Audio $V_{CC} = 3.6\ V_{DC}$						
Vinmax	Maximum Input Voltage Swing (1st Amp)	$f_O = 4$ kHz			$V_{CC} - 1.6$	V_{PP}
Vomax	Maximum Output Voltage Swing (1st Amp)	$f_O = 4$ kHz	$V_{CC} - 2.0$			V_{PP}
Vinmax	Maximum Input Voltage Swing (2nd Amp)	$f_O = 4$ kHz			$V_{CC} - 1.6$	
Vomax	Maximum Output Voltage Swing (2nd Amp)	$f_O = 4$ kHz	$V_{CC} - 2.0$			V_{PP}
Z_L	Differential Ended Output Load			270		Ω
Handset Application, Ceramic Earpiece, Audio $V_{CC} = 3.6\ V_{DC}$						
Vinmax	Maximum Input Voltage Swing (1st Amp)	$f_O = 4$ kHz			$V_{CC} - 1.6$	V_{PP}
Vomax	Maximum Output Voltage Swing (1st Amp)	$f_O = 4$ kHz	$V_{CC} - 1.0$	$V_{CC} - 0.6$		V_{PP}
Vinmax	Maximum Input Voltage Swing (2nd Amp)	$f_O = 4$ kHz			$V_{CC} - 0.2$	
Vomax	Maximum Output Voltage Swing (2nd Amp)	$f_O = 4$ kHz	$V_{CC} - 1.0$	$V_{CC} - 0.6$		V_{PP}
Z_L	Differential Ended Output Load			1000		Ω
Base Application, Audio $V_{CC} = 5\ V_{DC}$						
Vinmax	Maximum Input Voltage Swing (1st Amp)	$f_O = 4$ kHz			1.9	V_{PP}
Vomax	Maximum Output Voltage Swing (1st Amp)	$f_O = 4$ kHz	3			V_{PP}
Vinmax	Maximum Input Voltage Swing (2nd Amp)	$f_O = 4$ kHz			$V_{CC} - 1.6$	
Vomax	Maximum Output Voltage Swing (2nd Amp)	$f_O = 4$ kHz	3			V_{PP}
Z_L	Single Ended Output Load			450		Ω

3.0 Electrical Specifications (Continued)

3.4.5 RX Amplifier Characteristics $T_A = 25°C$, Audio $V_{CC} = 5\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			200		kHz
V_{IN} max	Maximum Input Voltage Swing (Differential)	$f_O = 4$ kHz		0.32	3.2	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	$f_O = 4$ kHz	3.2			V_{PP}
Z_L	Output Load			10k ‖ 70p		Ω ‖ F
TD	Total Distortion	$f_O = 4$ kHz		0.5	1.0	%
I_B	Input Bias Current				100	nA

3.4.6 Microphone Amplifier/Expander Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain		60			dB
GBW	Gain-Bandwidth Product			500		kHz
V_{IN} max	Maximum Input Voltage Swing	$A_{CL} = 20$ dB, $f_O = 4$ kHz			$V_{CC} - 1.6$	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	$A_{CL} = 20$ dB, $f_O = 4$ kHz	$V_{CC} - 0.6$	$V_{CC} - 0.4$		V_{PP}
A_{CLH}	Closed Loop Gain—High Output	$V_O > V_{SWH}$, $f_O = 1$ kHz		20		dB
A_{CLL}	Closed Loop Gain—Low Output	$V_O < V_{SWL}$, $f_O = 1$ kHz		14		dB
V_{SWL}	Low Gain Switching Output Voltage	90% of final gain		5		mVrms
V_{SWH}	High Gain Switching Output Voltage	90% of final gain		50		mVrms
t_{SPATCK}	Speech Response Attack Time	$C_{EXT} = 0.4\ \mu$F, @ 100 mVrms 90% of final gain		25		ms
t_{SPDECY}	Speech Response Decay Time	$C_{EXT} = 0.4\ \mu$F, @ V_{OUT} max 90% of final gain		85		ms
TD	Total Distortion	$f_O = 200$ Hz–4 kHz		0.5	1.0	%
f_{LOW}	Low Frequency Cut-off	$Z_{CL} = Z_{CL0} - 3$ dB		180		Hz
Z_s	Source Impedance			4.7		kΩ
	External Resistor Value for Defeat	Handset Base		75 200		kΩ
	Gain Switching Threshold			35		mVrms
I_B	Input Bias Current				100	nA

3.4.7 Preemphasis Filter Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			500		kHz
V_{IN} max	Maximum Input Voltage Swing	$A_{CL} = 0$ dB, $f_O = 4$ kHz			$V_{CC} - 1.6$	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	$A_{CL} = 0$ dB, $f_O = 4$ kHz	$V_{CC} - 2.0$			V_{PP}
Z_L	Output Load			10k ‖ 70p		Ω ‖ F
A_{CL}	Closed Loop Gain	$f_O = 4$ kHz		0		dB
f_P	Filter Pole Frequency (−3 dB)	$Z_{CL} = Z_{CL0} - 3$ dB		1.0		kHz
I_B	Input Bias Current				100	nA

3.0 Electrical Specifications (Continued)

3.4.8 Auxilliary Amplifier Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			200		kHz
V_{IN} max	Maximum Input Voltage Swing	$f_O = 4$ kHz			$V_{CC} - 1.6$	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	$f_O = 4$ kHz, $V_{CC} = 5V$	$V_{CC} - 2.0$	$V_{CC} - 1.6$		V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	$V_{CC} = 5V$	3			V_{PP}
Z_L	Output Load	$f_O = 4$ kHz		10k		Ω
A_{CL}	Closed Loop Gain	f_O = DC		6		dB
TD	Total Distortion	$f_O = 4$ kHz		0.5	1.0	%

3.5 RX Data Slicer Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.6\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
V_{IN} max	Maximum Input Voltage Swing				$V_{CC} - 1.6$	V_{PP}
V_O low	Output Voltage Low (OC Out)		0		0.25 V_{CC}	V
V_O high	Output Voltage High (OC Out)		0.75 V_{CC}		5.0	V
V_{SWIT}	Switching Point		$V_{REF} \pm$ 450 mV	$V_{REF} \pm$ 500 mV	$V_{REF} \pm$ 600 mV	V
t_r/t_f	Rise and Fall Time	10%–90% 90%–10%			2	μs
	Output State When No Data			Last Valid Data		
I_{SINK}	Sink Current	$V_{OL} = 0.45V$	2			mA

3.6 Serial Interface DC and AC Characteristics $T_A = 25°C$, Audio $V_{CC} = 3.0\ V_{DC}$–$5.0\ V_{DC}$, $V_{SS} = 0\ V_{DC}$

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
I_{IL}	Input Leakage	$V_{IN} = 0V$ to V_{DD}	−1		1	μA
V_{IH}	Input High Voltage	$I_{IN} = 20\ \mu A$	$V_{CC} - 0.3$		V_{CC}	V
V_{IL}	Input Low Voltage	$I_{IN} = 20\ \mu A$	0		0.3	V
t_r/t_f	Rise and Fall Times	20%–80% and 80%–20%			200	ns
f_{SK}	CLK Clock Frequency		0	256	260	kHz
t_{SKH}	CLK High Time		1.2			μs
t_{SKL}	CLK Low Time		1.2			μs
t_{CSS}	CS Setup Time	Relative to CLK	12			μs
t_{LH}	Data Latch Hold Time	Relative to CS Inactive	5			μs
t_{SIS}	SI Setup Time	Relative to CLK	800			ns
t_{SIH}	SI Hold Time	Relative to CLK	800			ns

3.0 Electrical Specifications (Continued)

3.7 PLL Synthesizer DC Characteristics $T_A = 25°C$, $V_{CC} = 3.6$ DC

Symbol	Characteristic	Conditions	Pin	Min	Max	Units
V_{IL}	Input Voltage Low		Data, Clk, En		0.3	V
V_{IH}	Input Voltage High		Data, Clk, En	$V_{CC} - 0.3$		V
I_{IL}	Input Current Low		Data, Clk, En	−5		μA
I_{IH}	Input Current High		Data, Clk, En		5	μA
I_{PDSRC}	Phase Detect Source Current		Rx PD, Tx PD	−0.5		mA
I_{PDSNK}	Phase Detect Sink Current		Rx PD, Tx PD		0.5	mA
V_{OLPD}	Phase Detect Output Voltage Low	$I_{PDSNK} = 0.5$ mA	Rx PD, Tx PD		0.6	V
V_{OHPD}	Phase Detect Output Voltage High	$I_{PDSRC} = -0.5$ mA	Rx PD, Tx PD	3.0		V
	TRI-STATE® Leakage Current		Rx PD, Tx PD	−50	50	nA
	Input Capacitance		Data,Clk,En		8	pF
	Output Capacitance		Rx PD, Tx PD		8	pF
t_{SU}	Setup Time Data to CLK		Data, CLK	100		ns
t_{SU}	Setup Time En to CLK		En, CLK	200		ns
t_H	Hold Time		Data, CLK	90		ns
t_{REC}	Recovery Time		En, CLK	90		ns
t_W	Input Pulse Width		En, Clk	100		ns
	2nd LO Frequency				12	MHz
	Tx VCO Input Frequency	$V_{IN} = 200$ mV$_{PP}$			80	MHz

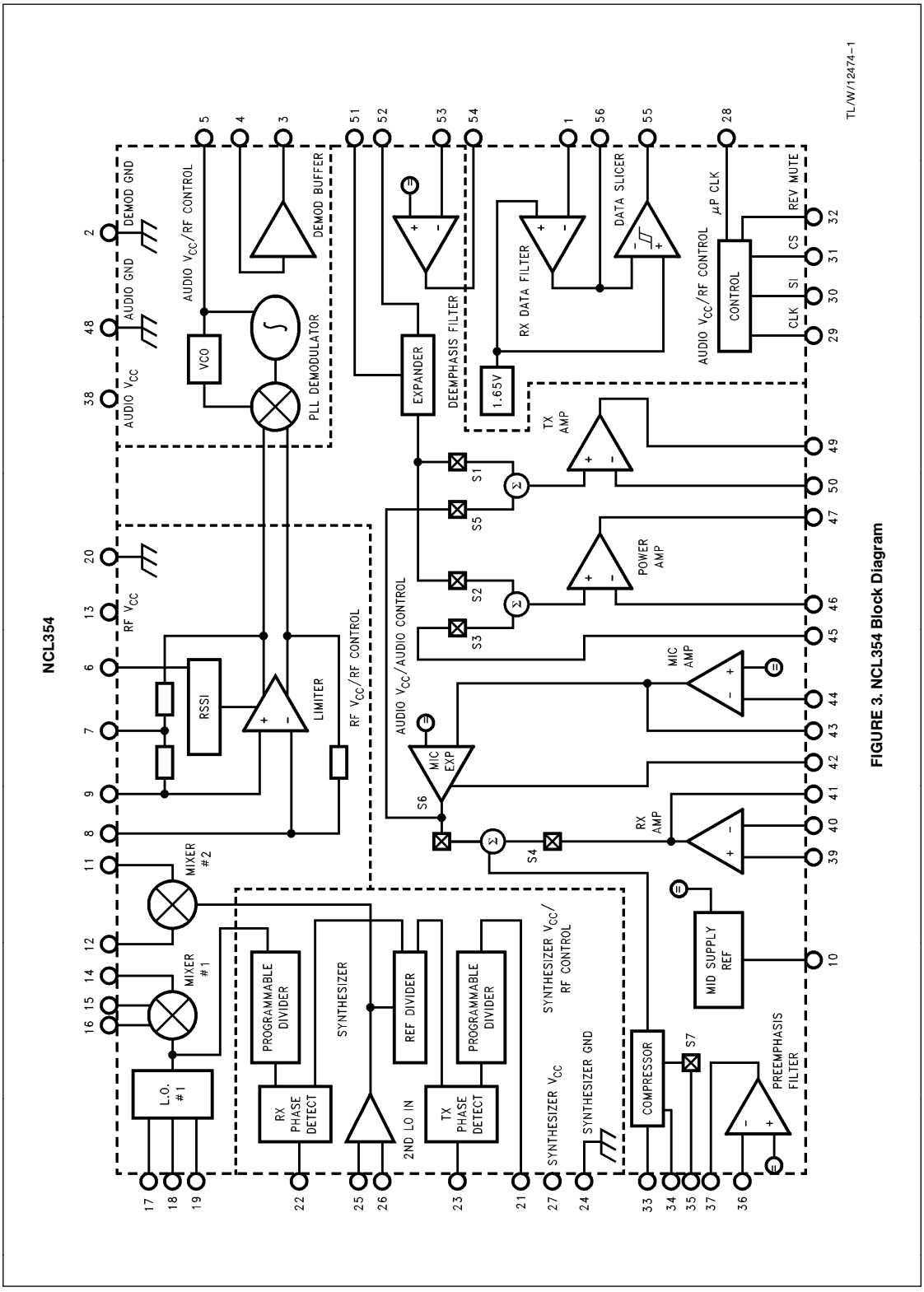
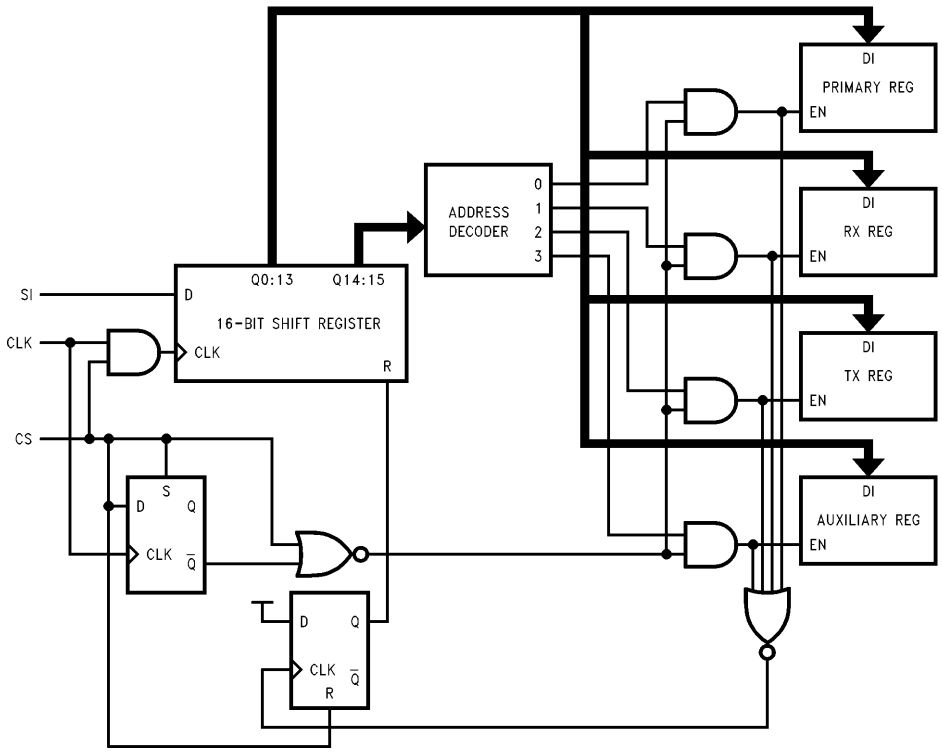


FIGURE 3. NCL354 Block Diagram

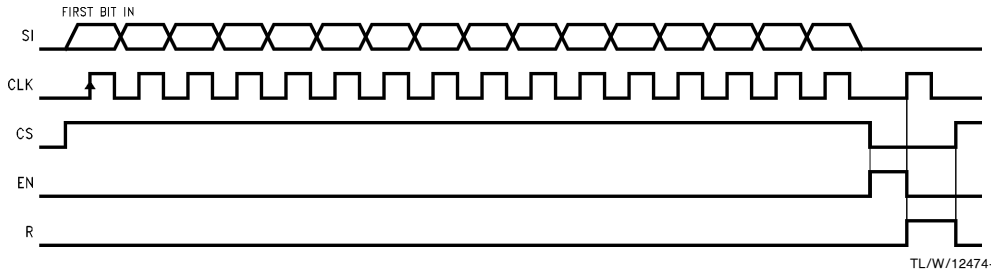
4.0 NCL354 Serial Interface Timing



TL/W/12474–3

FIGURE 4. Serial Interface

Serial Interface Timing

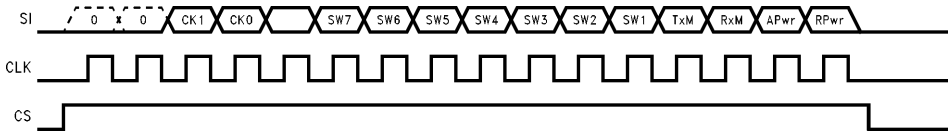


TL/W/12474–4

Note: "EN" is an internal signal that loads the registers.
"R" is an internal signal that resets the 16-bit shift register.
An extra clock pulse is required for resetting the shift register when < 16-bits are entered (SNFF mode).

4.0 NCL354 Serial Interface Timing (Continued)

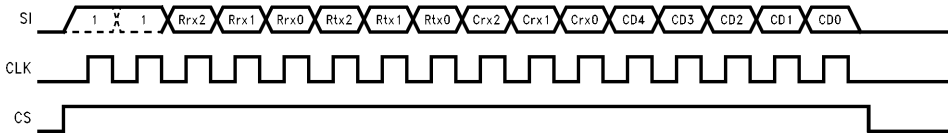
Serial Interface Timing—Primary Control Register



TL/W/12474–5

CK1–CK0	Clock Divider Select
SW7–SW1	Switch Select (“1” = switch closed)
TxM	Transmit Mute
RxM	Receive Mute
APwr	Audio Power Switch

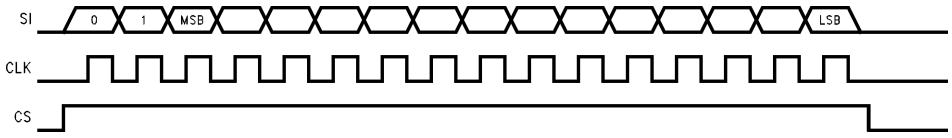
Serial Interface Timing—Auxiliary Control Register



TL/W/12474–6

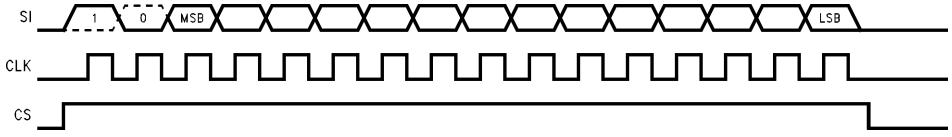
Rrx2–Rrx0	Receive Reference Frequency Select
Rtx2–Rtx0	Transmit Reference Frequency Select
Crx2–Crx0	Capacitor Select for Receive VCO
CD4–CD0	Carrier Detect Level
RPwr	RF Power Switch

Serial Interface Timing—Receive Divider



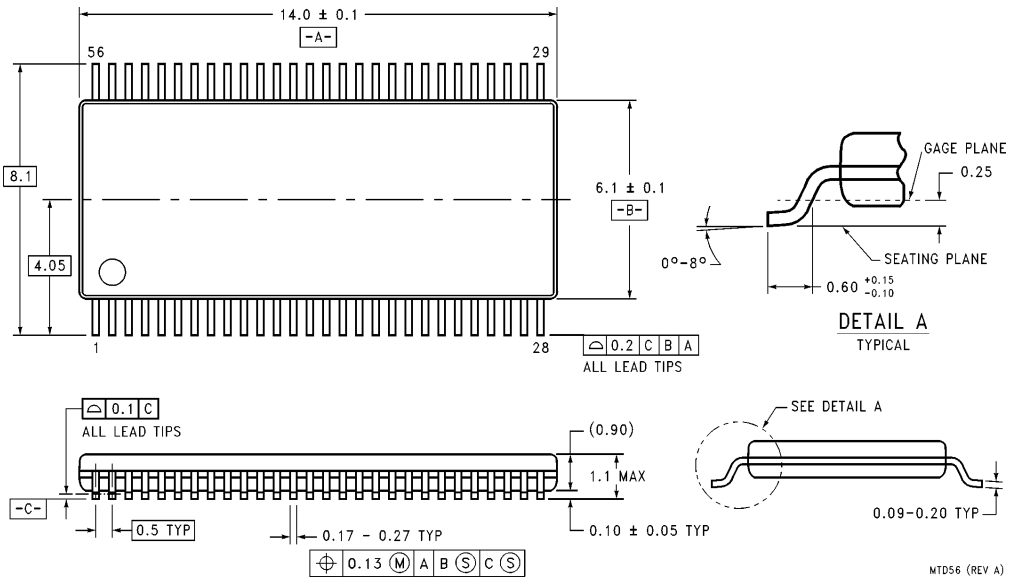
TL/W/12474–7

Serial Interface Timing—Transmit Divider



TL/W/12474–8

Physical Dimensions inches (millimeters)



56-Lead Molded TSSOP, JEDEC
Order Number NCL354
NS Package Number MTD56

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408