CHIP-MITTER™ - Single Chip FM Transmitter

130 - 1000 MHz

NT2800

FEATURES

- **Wide Bandwidth FM Transmitter**
- **Suitable for FM/FSK Modulation**
- **Direct-Modulation Scheme**
- **On-Chip PLL Synthesizer/VCO**
- **3-wire serial interface**
- **2.7 - 3.3V Operation / Standby Mode**
- **RF Output +1.5 dBm**
- **Low Cost, Quad Small Outline Package, (QSOP-16)**
- **BiCMOS Fabrication**

APPLICATIONS

Analog/Digital "900 MHz" Cordless Phones
Telemetry/Data Radios
Wireless Local Area Networks (WLAN)
ISM Band (900 MHz) Wireless Products

GENERAL DESCRIPTION

The NT2800 CHIP-MITTER™ is a complete, single chip, FM Transmitter solution, which will operate in any 26 MHz band from 130-1000 MHz, including the Industrial Scientific Medical (ISM) band (902-928 MHz). Utilizing a direct-modulation approach, the NT2800 CHIP-MITTER™ provides radio designers with a "simple" RF path design solution. The device is fabricated as a monolithic, BiCMOS, integrated circuit.

The device's transmitter section contains a directly modulated VCO and RF power amplifier (PA). An internal, high-performance phase locked loop (PLL) synthesizer/VCO allows transmitter operation over the entire RF tuning range. PLL programming, VCO trim, and power management, functions are accomplished via a 3-wire serial interface.

NUMA Technologies
5551 Ridgewood Drive, Suite 303
Naples Florida 34108
Phone: (941) 591-8008 FAX: (941) 591-8704
e-mail numatech@peganet.com
2Q/01

PRODUCT DESCRIPTION

The BiCMOS construction of the NT2800 CHIP-MITTER™ provides a high level of integration, with high performance operation and low power consumption. The CHIP-MITTER™ operates over an industrial temperature range of -20°C to +65°C and over the supply voltage of +2.7 V to +3.3 V. The device is available in an industry standard plastic package as a quad small outline package (QSOP-16).

FUNCTIONAL DESCRIPTION

A functional block diagram of the NT2800 CHIP-MITTER™ is shown in Fig.(1). The transmit section of the device consists of a PLL synthesizer / directly modulated voltage controlled oscillator (VCO), and a RF power amplifier (PA). Additionally, the device contains an on-chip crystal reference oscillator.

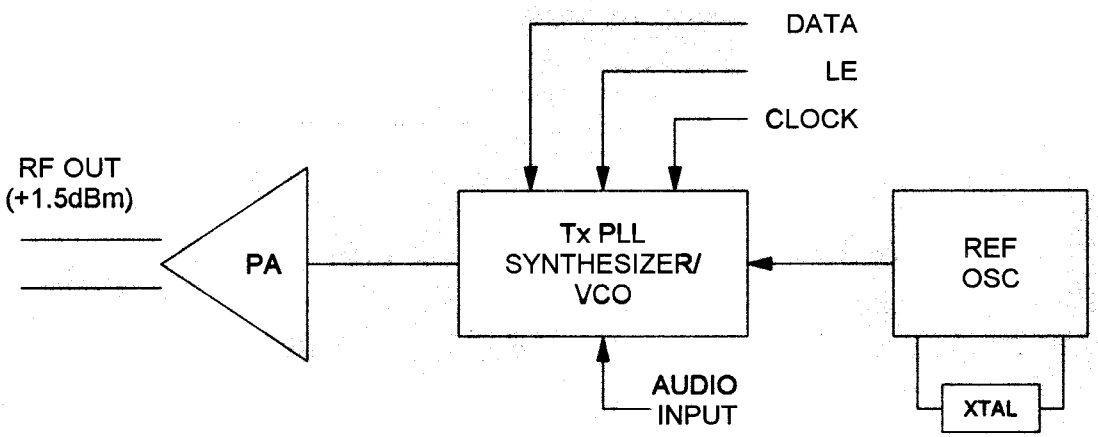


Figure (1), NT2800 CHIP-MITTER™ - Functional Block Diagram

The transmitter section of the NT2800 CHIP-MITTER™ is comprised of a modulation input circuit, a PLL synthesizer / VCO, and a RF power amplifier (PA) capable of providing +1.5 dBm into a 50Ω load. A description of each of the major function blocks follows:

PLL Synthesizer (Transmit) - The transmit (Tx) on-chip PLL synthesizer with an on-chip, voltage controlled oscillator (VCO), contains a dual-modulus prescaler (32/33) and employs a digital phase locked loop architecture. The transmit VCO can operate in any 24 MHz band from 130-1000 MHz. The transmit PLL accepts modulation audio to provide a frequency modulated (FM) RF carrier. Utilizing a direct modulation approach, the modulation voltage is

FUNCTIONAL DESCRIPTIONS - Cont.

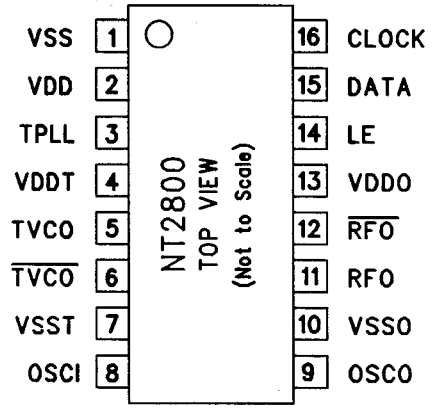
directly applied to the PLL loop filter. The VCO center frequency is determined by an external tank circuit comprised of two inductors connected to the TVCO (5) and /TVCO (6). An external PLL loop filter network, connected to the TPLL pin (3), filters the VCO control voltage. This control voltage (K_{VCO} 26 MHz/V) is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair. The transmit frequency for the CHIP-MITTER™ is programmed via a three (3) wire compatible, serial interface (Data, Clock, and Load Enable).

REFERENCE OSCILLATOR – The on-chip crystal reference oscillator is comprised of a CMOS colpits oscillator. The reference oscillator provides the reference frequency for the Tx PLL.

PA - The on-chip RF power amplifier is a differential gain stage. The power amplifier requires a combiner network as shown in the application circuit (Fig 2). The combiner network converts the amplifier's differential output (balanced 700Ω) to a single-ended output, capable of delivering +1.5 dBm into a 50Ω load.

PIN CONFIGURATION

Plastic Quad Small Outline Package (QSOP-16 pin)



PIN DESCRIPTIONS

This section summarizes the pin descriptions of the NT2800 CHIP-MITTER™ by pin name.

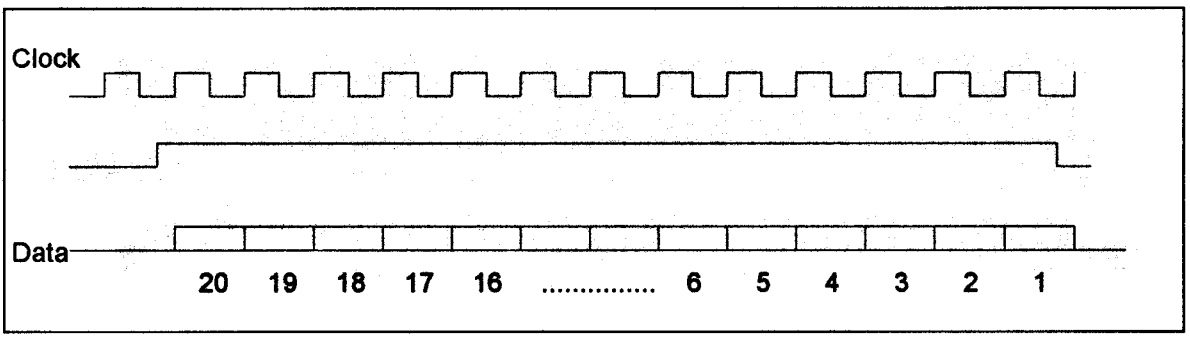
Pin Name	Pin Number	Description
VSS	(1)	Digital ground: This is the ground pin for the internal CMOS digital circuitry.
VDD	(2)	Digital power supply: This is the power supply pin for the internal CMOS digital circuitry for the synthesizer, reference sythesizer dividers, PLL charge-pump, PLL phase / frequency detector and crystal oscillator. This pin should be de-coupled to ground, as close to the pin as possible, with a high quality .1μF ceramic capacitor.
TPLL	(3)	Transmit Voltage Controlled Oscillator: This pin connects to an external PLL loop filter, which provides the tuning voltage for the internal varactor tuning diodes. The PLL loop dynamics are controlled by the loop filter component values. Transmitter modulation is accomplished by directly applying the modulating signal (Audio/Data) to the PLL loop, via an external AC coupled, pre-filter network.
VDDT	(4)	Transmit VCO supply: This is the power supply pin for the internal voltage controlled oscillator (VCO) and buffer. This pin should be de-coupled to ground, as close to the pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.
TVCO **/TVCO**	(5, 6)	Transmit VCO Tank: These single-end outputs drive the external, balanced, VCO resonant tank circuit. The tank circuit generates the overall oscillation frequency for the TxVCO. Since the VCO is directly modulated, the resultant carrier frequency is that of the VCO frequency.
VSST	(7)	Transmit VCO ground: This is the ground pin for the internal VCO and buffer circuitry.
OSCI	(8)	Oscillator Input: This CMOS input is the reference frequency input for both the Tx and Rx PLLs. When used with an external reference oscillator, the signal level should be within the range of 200-400mV peak. Additionally, this input can be used with the OSCO pin to form a Colpitts crystal oscillator.

PIN DESCRIPTIONS - Cont.

OSCO	(9)	Oscillator Output: This CMOS compatible output is used in conjunction with OSCIN to form a Colpitts oscillator using an external, low cost, crystal (parallel-resonant).
VSSO	(10)	Transmit RF ground: This is the ground pin for the internal power-amplifier (PA) and bi-polar sections of the sythesizer divider. This pin should be connected directly to an RF ground plane using through-hole vias.
RFO, \RFO	(11, 12)	RF Amplifier Outputs: These are the differential outputs of the power amplifier which require a combiner network as shown in the application circuit (Fig. 2). The output impedance of the power amplifier (PA) is $\approx 700\Omega$ (differential). The combiner circuit, (Fig. 2) allows the delivery of 1.5 dBm into a 50Ω load.
VDDO	(13)	Transmit PA supply: This is the power supply pin for the internal power-amplifier (PA) and bi-polar sections of the sythesizer divider. This pin should be de-coupled to ground, as close to the pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.
LE	(14)	Load Enable: This CMOS compatible input when HIGH allows data to be shifted into the internal shift register.
DATA	(15)	Serial Data Input: This CMOS compatible input accepts data MSB first. Refer to page (5) for additional information on the programming format.
CLK	(16)	Serial Clock: This CMOS compatible input shifts serial data into the internal 20-bit serial shift register, upon the rising edge of the clock signal.

Tx PLL PROGRAMMING and SERIAL INTERFACE

The Tx VCO divide ratios are controlled by a standard 3-wire bus comprised of Clock, Load Enable, and Data inputs. The programming word contains 20 bits, the first two bits select the programming of the transmit VCO frequency, the reference frequency or the device operational modes. The remaining bits contain the data to be programmed.



The above diagram shows the programming format.

Serial data is applied to the DATA (15) pin and is clocked into the internal shift registers on the positive edge of the CLOCK (16) pin, while Load Enable (14) pin is held HIGH. Data is loaded from the shift registers into the data registers on the negative edge of the Load Enable (LE). This load is NOT synchronized with the programmable divider, i.e. the load is controlled directly by the negative falling edge of the Load Enable.

Data Register Contents

Reference Frequency Select

Bit 1 (last bit loaded)		Load control bit 1 = (0)
Bit 2		Load control bit 2 = (0)
Bit 3	Ref(1) LSB	Reference divide register (count 1 to 1024)
Bit 4	Ref(2)	Reference divide register (count 1 to 1024)
Bit 5	Ref(3)	Reference divide register (count 1 to 1024)
Bit 6	Ref(4)	Reference divide register (count 1 to 1024)
Bit 7	Ref(5)	Reference divide register (count 1 to 1024)
Bit 8	Ref(6)	Reference divide register (count 1 to 1024)
Bit 9	Ref(7)	Reference divide register (count 1 to 1024)
Bit 10	Ref(8)	Reference divide register (count 1 to 1024)
Bit 11	Ref(9)	Reference divide register (count 1 to 1024)
Bit 12	Ref(10) MSB	Reference divide register (count 1 to 1024)

Internal Reference Frequency = (Reference Oscillator Frequency) / Ref(10:1)

PLL Data Register Contents Cont.

Transmit VCO Frequency Select

Bit 1 (last bit loaded)		Load control bit 1 = (0)			
Bit 2		Load control bit 2 = (1)			
Bit 3	LSB	VCO frequency	A	Ta(1)	A register
Bit 4		VCO frequency	A	Ta(2)	A register
Bit 5		VCO frequency	A	Ta(3)	A register
Bit 6		VCO frequency	A	Ta(4)	A register
Bit 7	MSB	VCO frequency	A	Ta(5)	A register
Bit 8	LSB	VCO frequency	M*	Tm(1)	M register
Bit 9		VCO frequency	M	Tm(2)	M register
Bit 10		VCO frequency	M	Tm(3)	M register
Bit 11		VCO frequency	M	Tm(4)	M register
Bit 12		VCO frequency	M	Tm(5)	M register
Bit 13		VCO frequency	M	Tm(6)	M register
Bit 14		VCO frequency	M	Tm(7)	M register
Bit 15		VCO frequency	M	Tm(8)	M register
Bit 16		VCO frequency	M	Tm(9)	M register
Bit 17	MSB	VCO frequency	M	Tm(10)	M register

Bit 18	Tx VCO Trim bit 1
Bit 19	Tx VCO Trim bit 2
Bit 20	Tx VCO Trim bit 3

*Future version to provide an additional M counter bit.

TxVCO Frequency = Internal Reference Frequency (50kHz) x (32 x M(10:1) + A(5:1))

Tx VCO Trim Bits			
3	2	1	Trim Number
0	0	0	0 – Minimum C
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 – Maximum C

PLL Data Register Contents - Cont.

Mode select

For Mode and Test Mode select Bit 1 = (1), BIT 2 = (1)

Bit 1	Load Control Bit 1	(Last bit loaded)	
Bit 2	Load Control Bit 2		
Bit 3	Not Used		
Bit 4	Not Used		
Bit 5	Transmit Section	0 = OFF	1 = ON
Bit 6	Not Used		
Bit 7	Transmit Charge Pump Current	0 = 0.2 mA	1 = 1.0 mA
Bit 8	Not Used		
Bit 9	Tx Charge Pump Polarity	0 = NORMAL	1 = INVERT

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
OVERALL DEVICE:					
Power Supply Voltage	Vdd	2.7	3	3.3	V
Operating Temperature	Topr	-20		65	C
Tx Current Consumption (w/RF VCO)	Idd(Tx)		25		mA
Standby Current	Istb		50		µA
Frequency of Operation	Fopr	130		1000	MHz
SYSTEM LEVEL SPECIFICATIONS: (See applications circuit (Fig. 2) for additional details)					
Channel Spacing			150		kHz
Channel Step Size		50			kHz
L.O. Spurious Output			-60	-57	dBc
Tx Output Power (At Antenna Output)	Po	-3	-0.5	1	dBm
Tx Tuning Range		130	902-935	1000	MHz
DEVICE LEVEL SPECIFICATIONS:					
PLL (Tx)					
Phase Noise (10kHz Offset)			-85		dBc/Hz
Phase Noise (100kHz Offset)			-105		dBc/Hz
Phase Noise (1.0MHz Offset)			-125		dBc/Hz
Phase Noise (22.75MHz Offset)			-150		dBc/Hz
Spurious Products (Unwanted)		-60			dBc
Step Size		50			kHz
Reference Oscillator (Internal)		5		20	MHz
Power Amplifier (PA)					
Power Output		0	1.5	3	dBm
Output Impedance (Differential)		500	600	700	
Harmonic Level (2nd) - 909MHz			-54.2		dBc
Harmonic Level (3rd)			-44.2		dBc
Harmonic Level (4th)			-70.9		dBc
Transmit Audio Response					
Input Level (Standard Test Conditions)			200		mVrms
Input Sensitivity	Kvco		26MHz/V		V
Bandwidth (-3dB)		0.3		70	kHz

BOARD LAYOUT

Designing ultra-high frequency (UHF) RF circuits requires careful attention to detail and layout. Careful attention to layout should be observed to minimize stray inductance and capacitance effects. This attention to detail will preserve RF sensitivity of the NT2800 CHIP-MITTER™. At high frequencies, microstrip or strip-line transmission line techniques must be employed. Using "state-of-the-art" CAD techniques for PCB layout, standard FR-4 fiberglass PCB material (1.6-mm thickness) may be employed. For maximum performance, however, RF quality substrate material should be used.

SUPPLY DECOUPLING

Positive supply connections for the NT2800 are nominally 2.7V to 3.3V. All supply pins must be bypassed to an RF, Analog, or Digital ground plane depending upon the type of supply pin. For RF supply pins, a 100 pF ceramic capacitor in parallel with a 1.0 nF ceramic capacitor, both RF quality, should provide adequate decoupling. For analog and digital supply pins, 0.01-0.1μF RF quality capacitors should be used. The bypass capacitors should be placed as close to all power supply pins as possible. An effort should be made to minimize the trace length between the capacitor leads and the respective NT2800 power supply and common pins.

GROUNDING

The circuit designer should attempt to locate the NT2800 CHIP-MITTER™, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid RF analog ground should be placed around the LNA and associated RF filter circuitry, while a solid digital ground should be placed around the reference oscillator. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. Ground connections for the NT2800. Connect all ground pins together to a low impedance ground plane, as close to the device as possible. Observe proper RF grounding and shielding techniques. The NT2800 CHIP-MITTER™ should be used with separate analog and digital ground planes. The digital and analog ground planes should be "summed" at one point, typically at the power supply filter capacitor.

OPERATING PRECAUTIONS

NUMA Technologies' plastic molded BiCMOS LSI devices are designed and manufactured for trouble-free operation when used under normal operating conditions. Our products are subjected to stringent electrostatic, mechanical strength, and environmental tests for assured reliability. When working with our products the user should observe the following precautions:

(1) Use the product in the range of the rated operating voltage, operating temperature, operating input/output voltage and input/output current. If the product is used outside these operating parameters, the user may experience high failure rates.

(2) Do not expose the product to excessive mechanical vibration, repetitive shock, or rapid or cyclic temperature changes. These factors can cause the bond wires in the plastic package to break.

(3) Although all terminals have electrostatic protection, damage may still occur if very high electrostatic potentials are applied. Use of a conductive container or aluminum foil for packaging and transportation is recommended. (Untreated plastic containers are NOT recommended.) Use grounded soldering tools and test equipment.

(4) The NT2800 employs Electrostatic Discharge (ESD) protection. CMOS inputs shall be rated to 2Kv human body model / 1Kv charge contact model. Bipolar RF inputs shall be protected to the greatest extent possible and consistent with industry standards, while meeting RF performance parameters.

APPLICATION INFORMATION -- "900 MHz" Transmitter

A circuit diagram for a high performance wireless transmitter is shown in Figure (2). This circuit is applicable to wireless audio/data/telemetry links, compliant for use in the USA operating in the 902-928 MHz ISM band. The circuit will operate with a supply voltage of 2.7V to 3.3V. The "adjustment free" discriminator of the CHIP-MITTER™, along with the elimination of IF filters, provides a cost effective solution to cordless telephone applications.

Tuning and power management functions for the NT2800 (U1) are accessed via an industry standard 3-wire compatible serial interface. The "printed" VCO inductors (L1, and L2) provide the reactive elements for the on-chip VCO. The Transmitter can be tuned over the range of 902 to 928 MHz via the 3-wire interface. The modulation input accepts either data or analog signal types depending upon the application, i.e. audio (FM) or data (FSK).

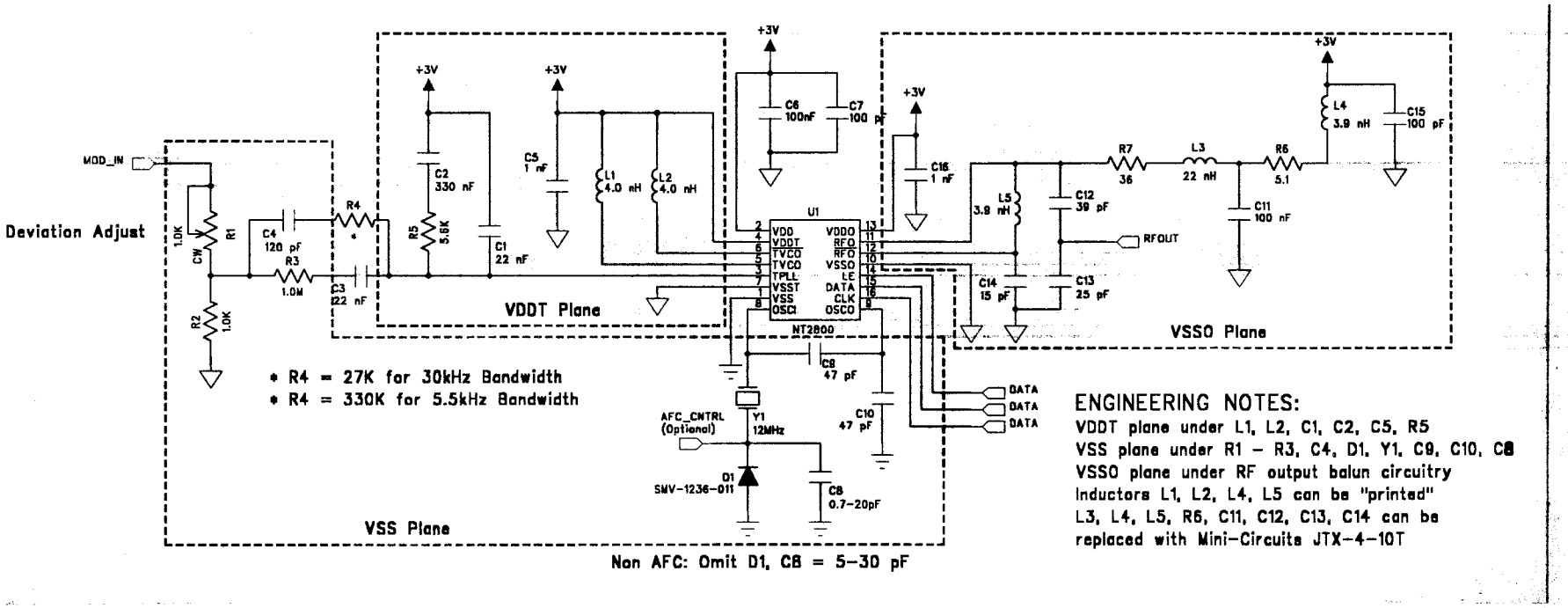


Figure (2), "900 MHz", High Performance, ISM Band Transmitter

Tx VCO:

The Tx VCO shall tune over a frequency range of 130-1000 MHz and over the temperature range of –20 to 65°C. The amplitude variation over the total tuning range should be less than 1dB.(± 0.5dB) The maximum change in the VCO frequency in the locked state due to different loads (short/open) or when an antenna is touched or brought near a metal object at the antenna input shall be ±2.5 kHz.

Tx Amplifier:

Power level at the output of the amplifier shall be +1.5dBm with a variation in power level < ±1.5 dB. (This includes the variations in amplitude from the VCO as well)

Load Pull:

The Tx amplifier should be stable (in-band) over VSWR of 10:1, the transmitter frequency change under the similar circumstances should not be more than ± 2.5kHz.