Nordic VLSI ASA

Stereo, 24-Bit, DVD-Ready, Low-Voltage Delta-Sigma DAC

nDA24192

FEATURES

- Complete Stereo DAC
- No External Analog Filter Needed
- Accepts All DVD Audio Data Formats
- Supports 24-Bits @ 192kHz
- I^2S-Compatible Digital Input
- Digital Volume Control
- Mute and Zero-Detect Mute
- Digital De-Emphasis
- 2.7-3.6V Analog Power Supply
- 1.6-2.0V Digital Power Supply
- Power-Down Mode
- SNR=113dB (A-Weighted Stereo)
- Group Delay Matching

APPLICATIONS

- DVD/CD Players
- HDTV Receivers
- Set-Top Boxes
- Home Theater Systems
- Car Audio Systems
- Digital Mixing Consoles
- Sampling Musical Keyboards
- Computer Multimedia Products

GENERAL DESCRIPTION

The nDA24192 is a complete high performance stereo audio digital-to-analog converter system (DAC). The DAC supports all common audio sample rates up to 192kHz, with up to 24 bits word lengths. The nDA24192 contains a serial data input port, a high performance digital interpolation filter, a 3rd order multibit delta-sigma modulator, an analog switched-capacitor pre-filter, and an analog continuous-time post-filter.
The nDA24192 also includes “clickless” mute and volume control, and digital de-emphasis. To ease integration in multi-channel applications the nDA24192 features group delay matching, which ensures that the group delay of nDA24192 cores running at different interpolation ratios is equal. The DAC is implemented in a 0.18µm standard CMOS process with thick oxide analog option.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DV_{DD}	Digital Supply Voltage		1.6	1.8	2.0	V
AV_{DD}	Analog Supply Voltage		2.7	3.3	3.6	V
P_D	Power Dissipation			150		mW
T_a	Ambient Temperature Range		-10		70	^oC
SNR	Signal-to-Noise Ratio	A-Weighted		113		dB
THD+N	Total Harmonic Noise+Distortion			-96		dB
R	Input Sample Rate		32		192	kHz

Table 1: Quick reference data

GENERAL DESCRIPTION (Continued)

The nDA24192 uses delta-sigma modulation with variable oversampling depending on input sample rate. A block diagram of the complete core is shown in Figure 1. The serial data input port (SCLK, LRCK, and SDATA) accepts audio data on the I^2S digital audio format. The DAC provides a separate pin for mute (MUTE) and has built-in zero detect mute functionality. The serial control interface (CCLK, CLATCH, and CDIN) can be used to control mute, volume and de-emphasis settings.

BLOCK DIAGRAM

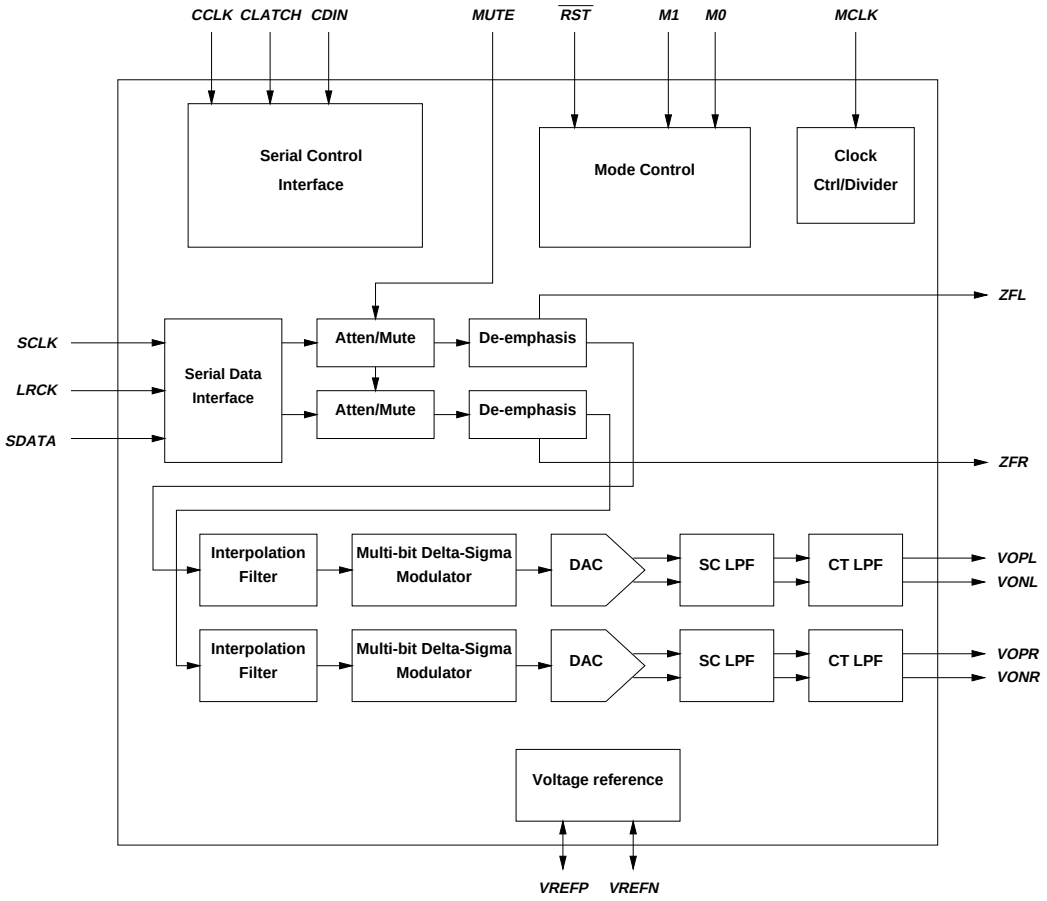

Figure 1: nDA24192 block diagram

ELECTRICAL SPECIFICATIONS

(T_A = 25°C, AV_{DD} = AV_{DDCK} = DV_{DDIO} = 3.3V, DV_{DD} = 1.8V, Input Sample Rate: 48kHz, Input Signal Frequency = 997Hz, Word Width: 24 Bits, Measurement Bandwidth: 20Hz to 20kHz, Input Signal -0.5dBFS, Clocks: 50% Duty Cycle With 2.5ns Rise and Fall Times Unless Otherwise Noted)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Unit
	Dynamic Performance					
SNR	Signal-to-Noise Ratio					
	A-weighted			113		dB
	Unweighted			110		dB
DR	Dynamic range (-60dBFS input signal)					
	A-weighted		110	116		
	Unweighted			113		
THD	Total Harmonic Distortion			-96	-92	dB
CRTLK	Interchannel Crosstalk			-92		
PSRR	Power Supply Rejection Ratio					
	1kHz 300mVp-p on AVDD			60		dB
	DC Accuracy					
	Interchannel Gain Mismatch			0.1		dB
	Gain Drift			100		ppm/°C
V_{OFF}	Differential DC Offset			2	10	mV
	Analog Output					
V_{p-p}	Full Scale Differential Output Voltage		4.0	4.4	4.8	Vpp
V_{CM}	Common Mode Output Voltage		1.3		2	V
R_L	AC Load Resistance		5			kΩ
C_L	Load Capacitance				75	pF
	Out-of-Band Energy (0.5×F_s to 96kHz)				-90	dB
	Digital Filter Response, OSR=128					
	Passband					
	±0.002dB				0.454	F_S
	-3dB corner				0.490	F_S
	Stopband		0.5465			F_S
	Passband Ripple				±0.002	dB
	Stopband Attenuation		95			dB
t_{gd}	Group Delay			$43/F_S$		s
	De-Emphasis Error (F_S = 32, 44.1, 48 kHz)				±0.1	dB
	Digital Filter Response, OSR=64					
	Passband					
	±0.002dB				0.433	F_S
	-3dB corner				0.484	F_S
	Stopband		0.570			F_S
	Passband Ripple				±0.002	dB
	Stopband Attenuation		88			dB

Table 2: Electrical specifications

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Unit
t_{gd}	Group Delay			$86/F_S$		s
	De-Emphasis Error				N/A	dB
	Digital Filter Response, OSR=32					
	Passband					
	±0.002dB				0.372	F_S
	-3dB corner				0.470	F_S
	Stopband		0.612			F_S
	Passband Ripple				±0.002	dB
	Stopband Attenuation		86			dB
t_{gd}	Group Delay			$172/F_S$		s
	De-Emphasis Error				N/A	dB
	Analog Filter Response					
	Frequency Response					
	f = 20kHz			-0.05		dB
	f = 44.1kHz			-0.45		dB
f_c	Cut-Off Frequency (-3dB)			110		kHz
	Switching Characteristics					
F_S	Input Sample Rate					
	OSR = 128		32		50	kHz
	OSR = 64		50		100	kHz
	OSR = 32		100		200	kHz
f_{MCLK}	MCLK Frequency					
	OSR = 128			256		F_S
	OSR = 64			256		F_S
	OSR = 32			128		F_S
	MCLK Duty Cycle		45		55	%
t_j	MCLK Jitter				200	psRMS
f_{LRCK}	LRCK Frequency			1		F_S
f_{SCLK}	SCLK Frequency			64		F_S
t_{slrd}	SCLK rising to LRCK edge delay		20			ns
t_{slrs}	SCLK rising to LRCK edge setup time		20			ns
t_{sdlrs}	SDATA valid to SCLK rising setup time		20			ns
t_{sdh}	SCLK rising to SDATA hold time		20			ns
t_{cccds}	CDIN valid to CCLK edge setup time		20			ns
t_{cccdh}	CCLK rising to CDIN hold time		20			ns
t_{clccd}	CLATCH falling to CCLK rising delay		20			ns
t_{clcch}	CCLK rising to CLATCH rising delay		20			ns
t_{clhh}	CLATCH high hold time		300			ns
	Digital Inputs					
V_{OH}	Logic “1” voltage		80%			DV_{DDIO}
V_{IL}	Logic “0” voltage				20%	DV_{DDIO}
I_{IH}	Logic “1” current ($V_{IN} = DV_{DD}$)				0.1	µA
I_{IL}	Logic “0” current ($V_{IN} = DV_{SS}$)				-0.1	µA
C_{IND}	Input Capacitance				TBD	pF

Table 2: Electrical specifications

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Unit
	Digital Outputs					
V_{OH}	Logic "1" voltage (I_{OH} = -2mA)		85%			DV_{DDIO}
V_{OL}	Logic "0" voltage (I_{OL} = +2mA)				0.4	V
	Power Supply					
DV_{DD}	Digital Core Supply Voltage		1.6	1.8	2.0	V
DV_{DDIO}	Digital I/O Supply Voltage		2.7	3.3	3.6	V
AV_{DD}	Analog Supply Voltage		2.7	3.3	3.6	V
AV_{DDCK}	Analog Clock Driver Supply Voltage		2.7	3.3	3.6	V
P_D	Power Dissipation (total)					
	Normal Operation			150		mW
	Power-Down			0.1		mW
T_a	Ambient Temperature Range		-10		70	^oC
I_{AVDD}	Analog Supply Current (AV_{DD} + AV_{DDCK})					
	Normal Operation			30		mA
	Power-Down			0.015		mA
I_{DVDD}	Digital Supply Current					
	Normal Operation (F_S = 44.1kHz)			20		mA
	Normal Operation (F_S = 96kHz)			30		mA
	Normal Operation (F_S = 192kHz)			40		mA
	Power-Down			0.03		mA
I_{DVDDIO}	Digital I/O Supply Current					
	Normal Operation (F_S = 44.1kHz)			4		mA
	Normal Operation (F_S = 96kHz)			6		mA
	Normal Operation (F_S = 192kHz)			8		mA
	Power-Down			0.005		mW

Table 2: Electrical specifications

Test Levels

Test Level I: 100% production tested at +25˚C

Test Level II: 100% production tested at +25˚C and sample tested at specified temperatures

Test Level III: Sample tested only

Test Level IV: Parameter is guaranteed by design and characterization testing

Test Level V: Parameter is typical value only

Test Level VI: 100% production tested at +25˚C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply Voltages

AV_{DD} and AV_{DDCK} ..... -0.3V to +4.5V
DV_{DDIO}..... -0.3V to +4.5V
DV_{DD} ..... -0.3V to +2.5V
AV_{DD} to AV_{DDCK} Difference.....±0.1V
AV_{DD} to DV_{DDIO} Difference.....±0.1V

Input voltages

Analog In ..... -0.3V to AV_{DD}+0.3V
Digital In.....-0.2V to DV_{DDIO}+0.2V
MCLK.....-0.3V to AV_{DDCK}+0.3V

Temperatures

Operating Temperature..... -10 to +70° C
Storage Temperature ..... -65 to +125° C

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
VOPL, VONL	Analog output (differential). Left channel
VOPR, VONR	Analog output (differential). Right channel
VREFP, VREFN	Differential voltage reference pins. Should be decoupled externally
MCLK	Master clock input. Connect to external clock source.
SCLK	Bit clock input.
LRCK	Left/right clock input.
SDATA	Serial data input.
ZFL	Left channel zero flag output. Goes high when left channel has zero input signal for more than 1024 LRCK clock cycles.
ZFR	Right channel zero flag output. Goes high when right channel has zero input signal for more than 1024 LRCK clock cycles.
MUTE	Mute. Assert HI will ramp both analog outputs to muted state.
$\overline{\text{RST}}$	Reset input pin, active low. When LO the nDA24192 is in power-down mode. The device is reset on the rising edge of this signal.
CCLK	Serial control port bit clock input.
CLATCH	Serial control port latch input.
CDIN	Serial control port data input. MSB first, 16 bits of unsigned data.
M1, M0	Mode select. Selects the digital oversampling ratio (OSR). See “Application Information” on page 11.
AVDD	Analog power supply pin. Should be connected to outside AV_{DD}
AVDDCK	Analog clock driver power supply pin. Should be connected to outside AV_{DD}
DVDD	Digital power supply pin. Should be connected to outside DV_{DD}
DVDDIO	Digital power supply to I/O. Should be connected to outside AV_{DD} through RF choke.
VSS	Ground pins.
N/C	This pin is for test purposes. Do **not** connect anything to this pin, leave open circuited.

Table 3: Pin Functions

PIN ASSIGNMENT

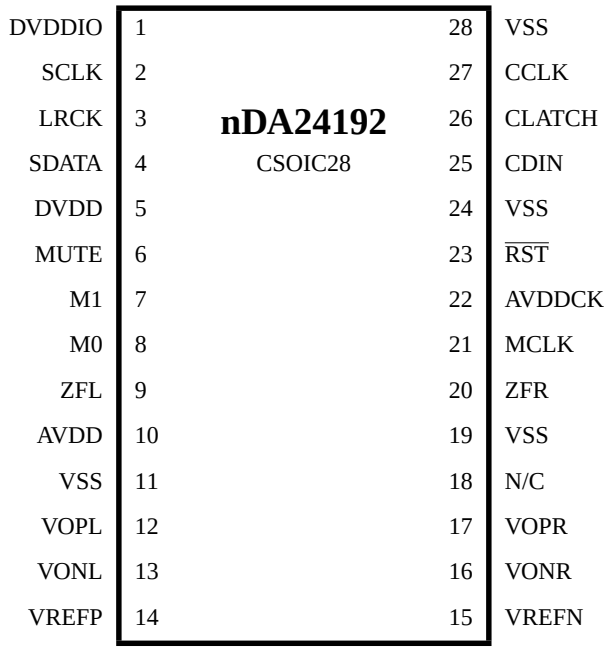

Figure 2: Pin assignment

TIMING DIAGRAMS

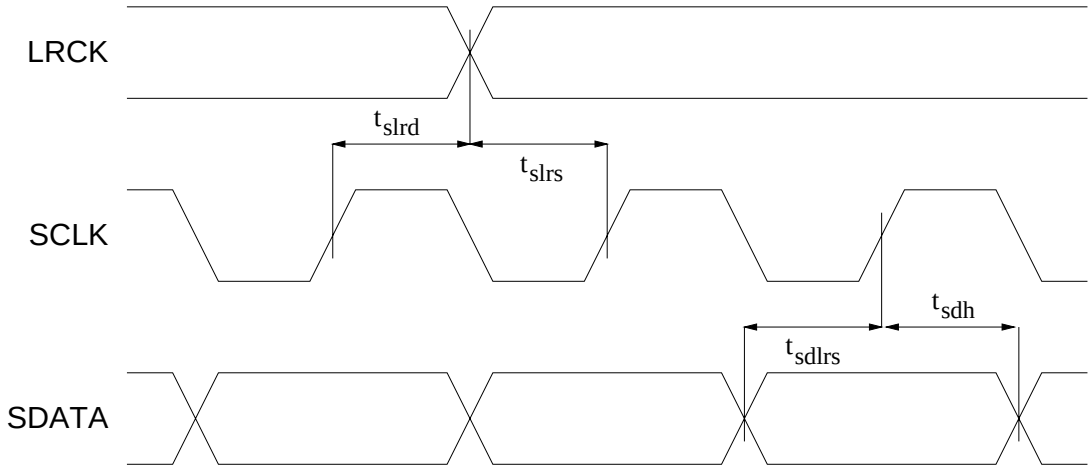

Figure 3: Serial Audio Input Timing

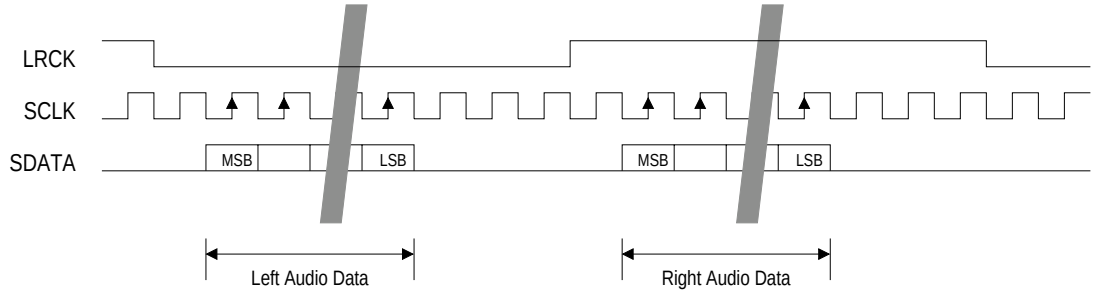

Figure 4: Serial Audio Input Format

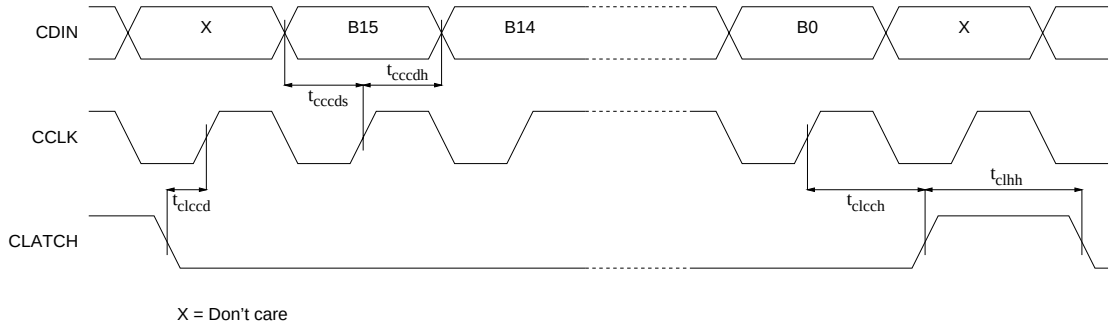

Figure 5: Serial Control Port Timing

TYPICAL PERFORMANCE CURVES

(TBD)

DEFINITIONS

Data sheet status	
Objective product specification	This data sheet contains target specifications for product development.
Preliminary product specification	This data sheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later
Product specification	This data sheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 4: Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

Mode Control Pins (MUTE, M1, and M0)

Logic “1” voltage on the MUTE pin will ramp both analog outputs to muted state. The ramping prevents the perception of a “click” sound. The ramp is logarithmic, and the outputs will be completely muted after a time $1024/F_S$. When the device is unmuted the ramp is reversed.

The mode control pins M1 and M0 are used to set the interpolation rate of the digital interpolator. Table 1 shows the valid values.

M1	M0	OSR	MCLK Frequency	Typical Input Sample Rates (F_S)
0	0	128	$256xF_S$	32kHz, 44.1kHz, 48kHz
0	1	64	$256xF_S$	88.2kHz, 96kHz
1	0	32	$128xF_S$	176.4kHz, 192kHz
1	1	DO NOT USE. Used for internal testing.		

Table 5: Mode Control Pins

Serial Control Port

In addition to the dedicated control pins (MUTE, M1, and M0) the nDA24192 can also be configured through the three-wire serial control port interface. CDIN is used for the configuration data. CCLK is used to clock in the configuration data, and CLATCH is used to latch in the configuration data. The timing is shown in Figure 5 on page 9. The operation of the control port may be asynchronous to the master clock, but for highest audio performance these pins should remain static under normal operation.

The control port requires 16 bits of unsigned serial data in MSB-first format. The top two bits are reserved. These should always be zero. The next two bits select one out of three registers. The bottom 12 bits are the data written to the selected register. The register mapping is shown in Table 6.

B13	B12	Register
0	0	Volume Left Register
0	1	Volume Right Register
1	0	Control Bit Register

Table 6: Control Register Mapping

The contents of the volume registers are used to multiply the signal. This means that the volume control is linear, and the 12 bits result in an attenuation range from 0 to 72 dB. The attenuation level is given by:

$$ATT = 20 \log((X+1)/4096) \text{ [dB]}$$

Where X is the volume register content (unsigned). To avoid the perception of a “click” sound when varying the volume, a write operation to one of the volume registers will result in a ramping of the volume to the new level. The ramp is completed after at time of approximately $1024/F_S$ in worst case. The default value of the volume registers (after reset) is “111111111111”, resulting in 0 dB attenuation.

The bit mapping of the control register (B13 = 1, B12 = 0) is shown in Table 7.

B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	res	res	E1	E0	MUTE	M1	M0

Table 7: Control Register Bit Mapping

Note that B11 to B3 are reserved and should be “0”. The MUTE, M1, and M0 bits are OR’d with the pins of the same name. For usage see the pin definitions. The default after reset is mute OFF and OSR=128.

The E1 and E0 bits select the de-emphasis filter to use. The de-emphasis bits are only

E1	E0	De-Emphasis Filter Select
0	0	No Filter
0	1	44.1 kHz Filter
1	0	32 kHz Filter
1	1	48 kHz Filter

Table 8: De-Emphasis Filter Select

used for OSR=128. The default after reset is “No Filter”.

Reset and Power-Down

The nDA24192 is in power-down mode when $\overline{RST}$ is low. The nDA24192 is reset on the rising edge of $\overline{RST}$. All configuration registers are reset to their default values.

References

The nDA24192 incorporates an internal voltage reference. The differential reference voltage is externally available on the VREFP and VREFN pins. To achieve the stated performance each of these pins should be decoupled to ground using 2.2µF capacitors with low internal impedance (For example Murata GRM42-6X7R225K10PT85). No additional circuitry should be connected to these pins!

Clock Input (MCLK)

The MCLK input should be connected to a high quality clock source with a duty-cycle of 50%. The “0” voltage should be equal to VSS, while the “1” voltage should be equal to AVDDCK.

Serial Audio Input Interface

The serial audio input interface consists of the following input pins:

- Left/Right Clock: LRCK
- Serial Clock: SCLK
- Serial Data: SDATA

The timing is shown in Figure 3, while the data format is shown in Figure 4. Both LRCK and SCLK must be synchronous to the system master clock (MCLK). The bit clock (SCLK) should be operated at 64 times the sampling frequency (F_S). The SDATA input requires MSB-first, binary two’s complement audio data. Note that the left channel data precedes the right channel data.

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