NX26F640C

NEXFLASH® Technologies, Inc.

64M-BIT SERIAL FLASH MEMORY WITH 2-PIN NXS INTERFACE

ADVANCED
JANUARY 2001

FEATURES

- **Flash Storage for Resource-Limited Systems**
  - Ideal for portable/mobile and microcontroller-based applications that store data, audio, and images
- **Nonvolatile Memory Technology**
  - Single transistor EEPROM memory
  - Erase/Write time of 10 ms/sector (typical)
  - Small DOS compatible sectors 512+16 (528) bytes for erase and write
  - AutoVerify function ensures that a sector is written accurately.
  - Optional 32KB block and sector erase for programming
  - 10K (Sector), 100K (Block) erase/write cycles
  - Ten years data retention
- **2-pin NXS-2 Serial Interface**
  - Easily interfaces to popular microcontrollers
  - Clock operation as fast as 16 MHz (standard)
- **Ultra-low Power for Battery-Operation**
  - Single 2.7-3.6V supply for Read, Erase/Write
  - 1 µA standby, 5 mA active (typical)
- **Special Features for Media-Storage Applications**
  - On-board 528 Byte SRAM Buffer
  - Byte-level addressing
  - Auto-increment sector read
  - Transfer and Compare sector to SRAM
  - Configurable software write-protection
  - In-system electronic serial number.
  - Serial Flash Development Kit
- **Package Options**
  - 32 Pin TSOP Surface Mount
  - Removable Cards and Modules

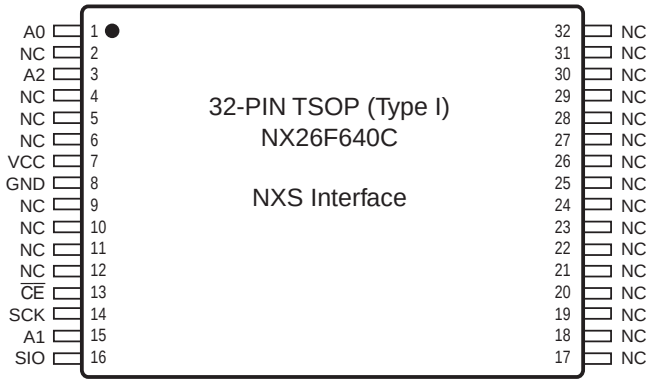
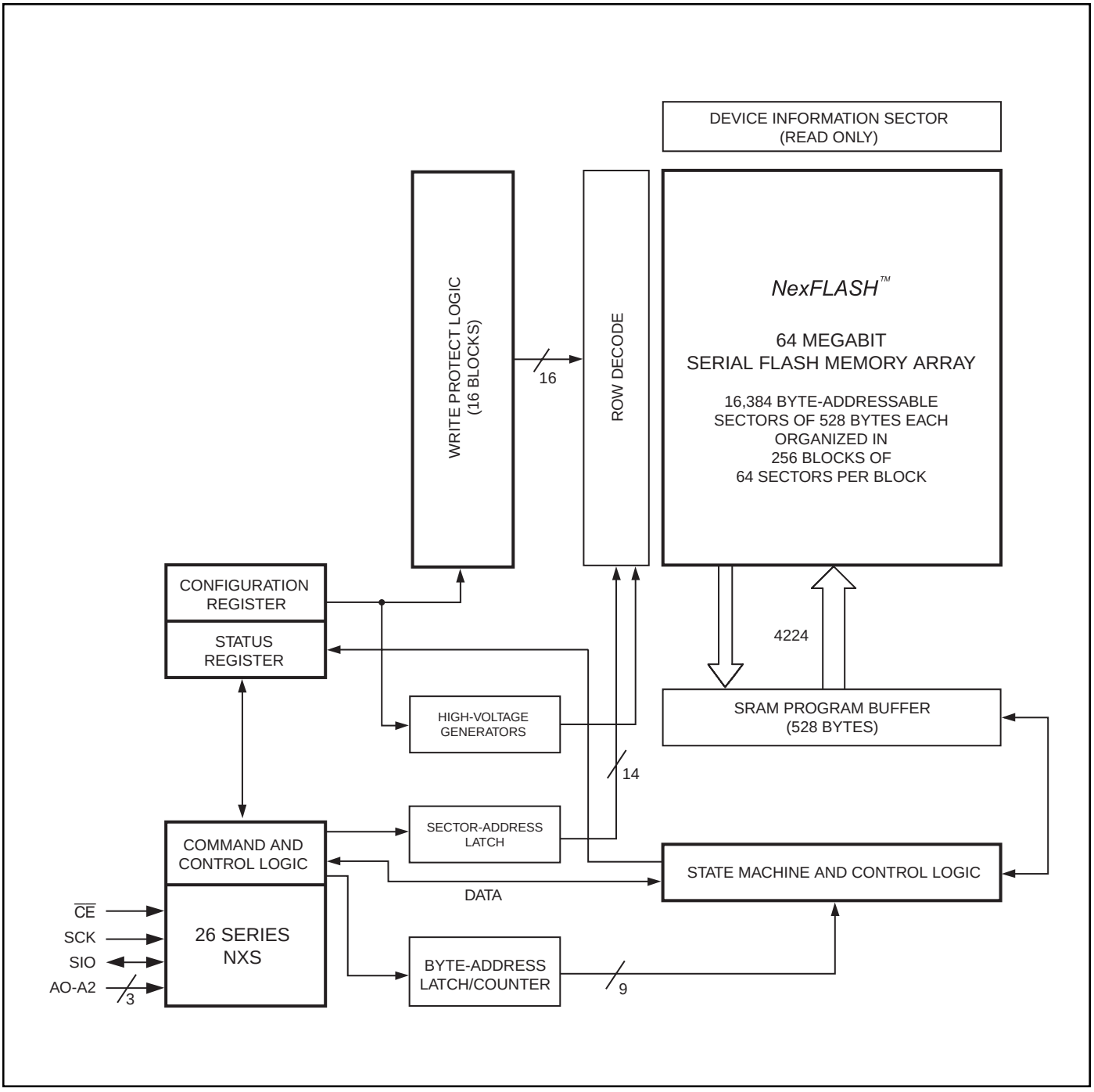


Table 1. Pin Descriptions for the 26F640

A0, A1, A2	Device Address
SIO	Serial Data Input/Output
SCK	Serial Clock Input
$\overline{CE}$	Chip Enable
VCC	Power Supply
GND	Ground



NX26F640C Architectural Block Diagram

Pin Descriptions

Static Address (A0, A1, A2**)**
The static address bits are used to allow up to 8 chips to be connected via a daisy chain on the same SCK and SIO pins. The NXS2 protocol selects the chip to address in the first byte of the command bit stream by matching the Device Address Field (DA2..0) to the A2..A0 pins.

Serial Data Input/Output (SIO)
The SIO pin transmits data into and out of the device with the SCK pin. All data transmitted to or from the chip is clocked relative to the rising edge of SCK.

Serial Clock Input (SCK)
All commands and data written to the SIO pin or read from the SIO pin are clocked relative to the rising edge of SCK. The clock rate may be up to 16Mhz. When the device is reset, the first low to high transition of the clock wakes the device up, the second low to high transition clocks the first command bit to the device on SIO. When the SIO line switches from an input to an output, the first transition of the clock switches the direction of the SIO line to an output.

Chip Enable ($\overline{CE}$)
The Chip Enable pin, when active, allows the device to decode the bit stream on the SCK and SIO pins. When the Chip Enable pin is not active, the device ignores any bit stream present on the SCK and SIO pins.

Power Supply Pins (Vcc and Gnd)
The NX26F640 supports a single power supply between 2.7V and 3.6V connected to the Vcc and Gnd pins.

Configuration Register

The Configuration register stores the current configuration of the Write protect range and direction, and NXS TRESET time.

All Reserved bits (RSVD) should be set to 0 while programming.

NXS Reset Timing (RST)
This bit determines the length of time for the timing parameter TRESET. With RST reset (0), the timing of TRESET should be minimum 1.5us, maximum 5us. With RST set (1), the timing of TRESET should be minimum 5us, maximum 10us.

Write Protect Range and Direction (WR3-WR0,WD)
The WR3-WR0 bits define the write-protect range. The WD bit defines the write-protect direction.

The WE bit in the status register controls the write protect function. If the WE bit is set in the status register, then the write protect range and direction are active. If the WE bit is reset in the status register, then the entire array is write-protected. Note each bit represents 64 sectors in the write-protect range.

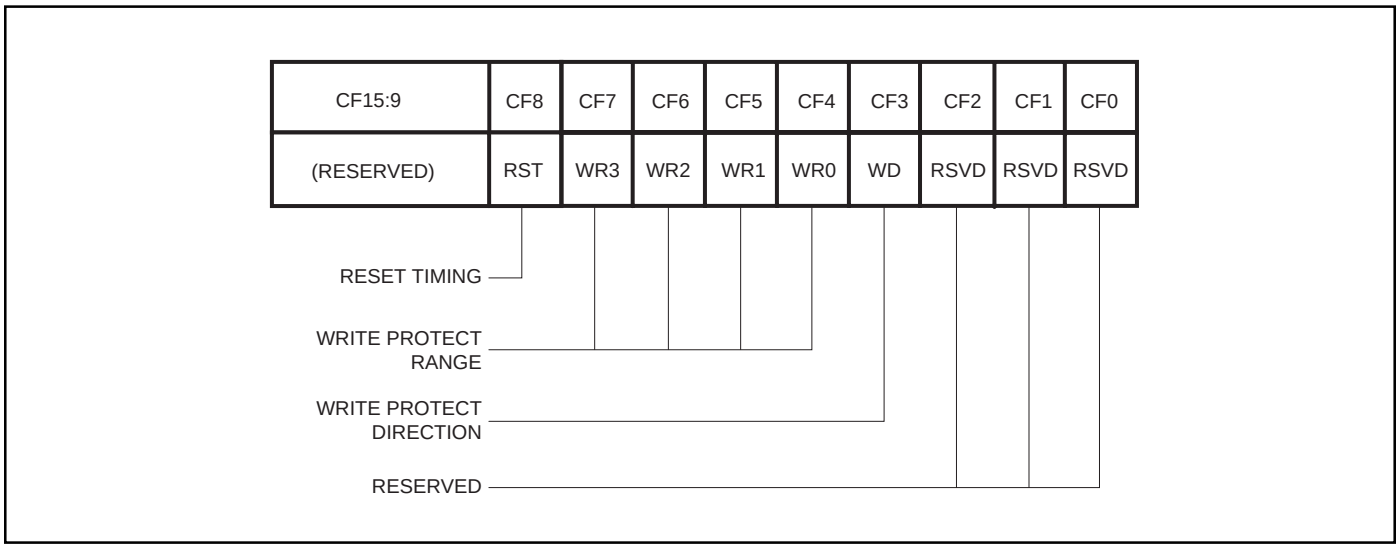


Figure 7. Configuration Register Bit Locations

Table 2. Write Protect Range Sector Selection (Hex)

Write Protect Range Config. Bits				Write Protected Sectors	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	0000-003F	3FC0-3FFF
0	0	1	0	0000-007F	3F80-3FFF
0	0	1	1	0000-00BF	3F40-3FFF
0	1	0	0	0000-00FF	3F00-3FFF
0	1	0	1	0000-013F	3EC0-3FFF
0	1	1	0	0000-017F	3E80-3FFF
0	1	1	1	0000-01BF	3E40-3FFF
1	0	0	0	0000-01FF	3E00-3FFF
1	0	0	1	0000-023F	3DC0-3FFF
1	0	1	0	0000-027F	3D80-3FFF
1	0	1	1	0000-02BF	3D40-3FFF
1	1	0	0	0000-02FF	3D00-3FFF
1	1	0	1	0000-033F	3CC0-3FFF
1	1	1	0	0000-037F	3C80-3FFF
1	1	1	1	ALL	ALL

Status Register

The status register contains the status for all operations of the device. The following table defines the bit definition of the status register.

Ready/Busy status (Busy)
The busy status bit reflects the ready/busy status of the chip. If the busy status bit is set, then a SRAM transfer, SRAM compare, array program, or array erase operation is in progress. No operations on the flash array may be performed while the Busy bit is set. If a non-array and non-SRAM oriented command needs to be performed, it can be performed at any time.

SRAM buffer 0 Transfer (TR0)
The TR0 bit indicates that a transfer operation involving SRAM buffer 0 is in operation. The Busy bit will also be set when TR0 is set. When this bit is set, a command which uses SRAM Buffer 0 cannot be executed.

Write Enable (WE)
This bit indicates whether the main flash array and the configuration register can be written to. The Write Enable and Write Disable command control this bit. Upon power-up, the WE bit is reset, and the main flash array write protected.

Compare Not Equal (CNE)
This bit provides the result of a Compare Sector with SRAM command. The CNE bit is clear at power-up. At the completion of a Compare Sector with SRAM command, this bit is set if the compare failed, and clear if the compare succeeded.

Error Erase (EE)
This bit provides status for the last erase operation on the main flash array. If this bit is set, then the last erase operation failed, and some bits did not program to the erased state (“1”). If this bit is clear, then the last erase operation succeeded. This bit could be used in conjunction with an ECC algorithm and/or a sector relocation algorithm.

Error Write (EW)
This bit provides status for the last AutoVerify write operation on the main flash array. If this bit is set, then the last verify operation failed, and some bits did not program to the non-erased state (“0”). If this bit is clear, then the last AutoVerify write operation succeeded. This bit could be used in conjunction with an ECC algorithm and/or a sector relocation algorithm.

Power Detect (PD)
This bit provides allows the detection of whether power has been removed from the device. It works in conjunction with the Set Power Detection Bit and Reset Power Detection Bit commands. When the device powers up this bit is cleared. Application firmware can use this bit to detect when a Serial Flash Module has been removed, by setting this bit, and polling the bit during status reads. If the bit is clear, then power has been removed, and the module changed.

Refresh Status (RS)
This bit provides the user with an indication that the flash sectors in the current block may need to be refreshed. When this bit is clear no refresh is required. When this bit is set, the block of the last accessed sector needs to be refreshed.

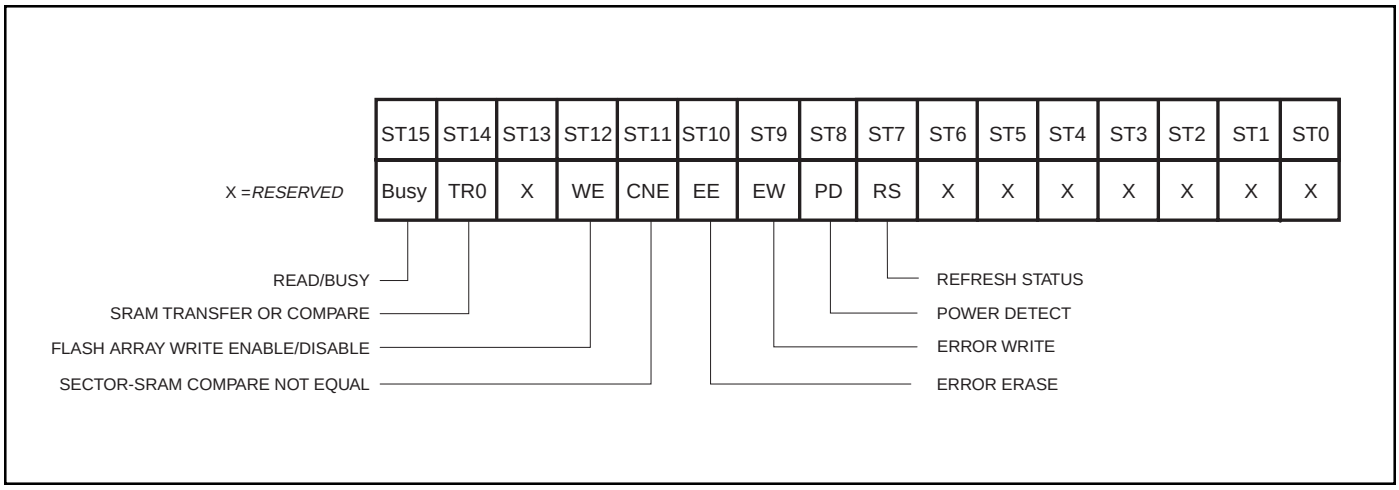


Figure 8. Status Register Bit Locations

NXS Command Set

Features

- Support 8 chips/Clock & Data pair.

The following are rules used for all commands in NXS mode:

- All data is shifted into the device MSB first.
- All data is shifted out of the device MSB first.
- Chip reset is achieved by holding the SCK pin low for more time than Treset.
- All commands must start while the chip is in the reset state.
- When the chip decodes the static address of the command stream, if it is not selected, it should tri-state SCK, SIO and power down.
- To start a command, an extra clock must be sent preceding the static address bit field.
- During commands where SIO must change direction, an extra clock is used between writing and reading data. This ensures that there is enough time to avoid contention on the SIO line.

Command Block Bit Definition

The commands for the NXS mode have a static address byte followed by a standard command from the NexFlash Common Command Set. This allows an efficient 2 wire interface using the NexFlash Common Command Set.

Command Set for the NX25F640C Serial Flash Memory

Command Name	Byte 0	Byte 1	Byte 2-3[4]	Byte 4-5[4]	n- bytes *(Italics indicate devise output)*		
Sector ***Commands***							
Read From Sector	DA7:0	52H	SA15:0	BA15:0	0000h	*Ready/Busy*	*Read Data*
Read From Sector w/AutoInc	DA7:0	50H	SA15:0	0000h	0000h	*Ready/Busy*	*Read Data*
Write Enable [1]	DA7:0	06H					
Write Disable [1]	DA7:0	04H					
Write to Sector (through SRAM) [2]	DA7:0	F3H	SA15:0	BA15:0	Write Data	00h	
Re-Write Sector through SRAM [2]	Device	58H	SA15:0	BA15:0	Write Data		
Serial SRAM Commands							
Write to SRAM [5]	DA7:0	72H	BA15:0	Write data	00h		
Read from SRAM [5]	DA7:0	71H	BA15:0	00h	Read Data		
Transfer all of SRAM to Sector [2]	DA7:0	F3H	SA15:0	0000h			
Transfer all of Sector to SRAM [2]	DA7:0	53H	SA15:0	0000h			
Compare all of Sector to SRAM [2]	DA7:0	8DH	SA15:0	0000h	0000h		
Configuration and Status Commands							
Read Configuration [1]	DA7:0	8CH	CF15:0				
Write Non-Volatile Configuration Register [1]	DA7:0	8AH	CF15:0	0000h			
Read Status Register [1]	DA7:0	84H	ST15:0				
Set Power Detection Bit [1]	DA7:0	03H					
Reset Power Detection Bit [1]	DA7:0	09H					
Read Device Information Sector	DA7:0	15H	0000h	0000h	0000h	*Ready/Busy*	*DIS Data*
Special Sector Commands							
Erase Sector [3]	DA7:0	F1H	SA15:0	0000h			
Erase Block [3]	DA7:0	F4H	BL15:0	0000h			
Write-Only to Sector thru SRAM [3]	DA7:0	F2H	SA15:0	BA15:0	Write Data	00h	

Notes:
1. Command may be used when device is busy
2. Command may not be used when device is busy
3. Warning: Read description of these commands before using to ensure reliable operation.
4. Device, Sector, Block and Byte are address references.
5. Command may be used when device is busy

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		0 to +4.0	V
V_{IN}, V_{OUT}	Voltage Applied to Any Pin	Relative to Ground	–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to +150	°C
T_{LEAD}	Lead Temperature	Soldering 10 Seconds	+300	°C

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.

OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	3.0V	2.7	3.6	V
T_A	Ambient Temperature, Operating	Commercial	0	70	°C
		Industrial	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (PRELIMINARILY)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.4	—	Vcc 0.2	V
V_{IH}	Input High Voltage		Vcc 0.7	—	Vcc +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 2.7V	—	—	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = 2.7V	Vcc 0.85	—	—	V
V_{OLC}	Output Low Voltage CMOS	V_{CC} = 2.7V, I_{OL} = 10 µA	—	—	0.15	V
V_{OHC}	Output High Voltage CMOS	V_{CC} = 2.7V, I_{OH} = –10 µA	V_{CC}–0.3	—	—	V
I_{IL}	Input Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{OL}	I/O Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Erase/Write	—	2.5	5	mA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Read	—	5	10	mA
I_{CCSB} (standby)	Standby Vcc Supply Current	CS = V_{CC}, V_{IN} = Vcc or 0 Standby	—	1	10	µA
C_{IN}	Input Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF
C_{OUT}	Output Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF

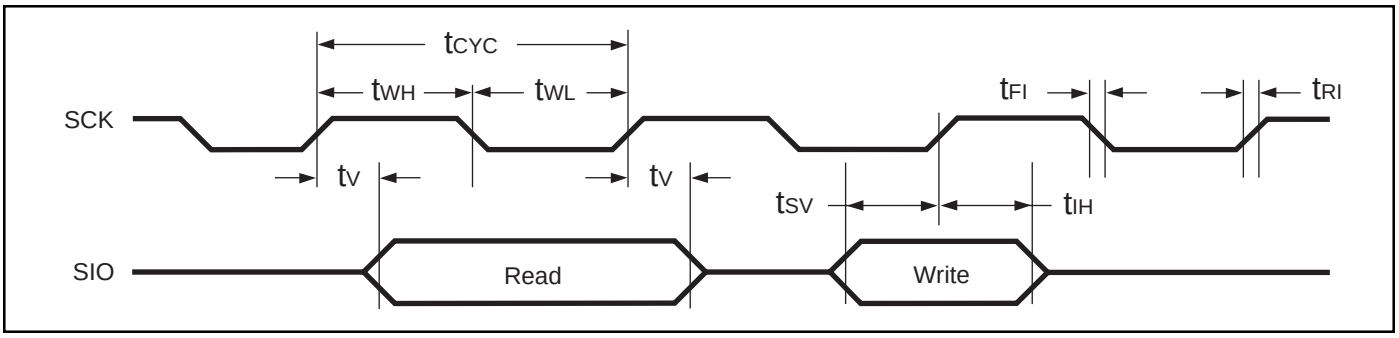
Note:
1. Tested on a sample basis or specified through design or characterization data.

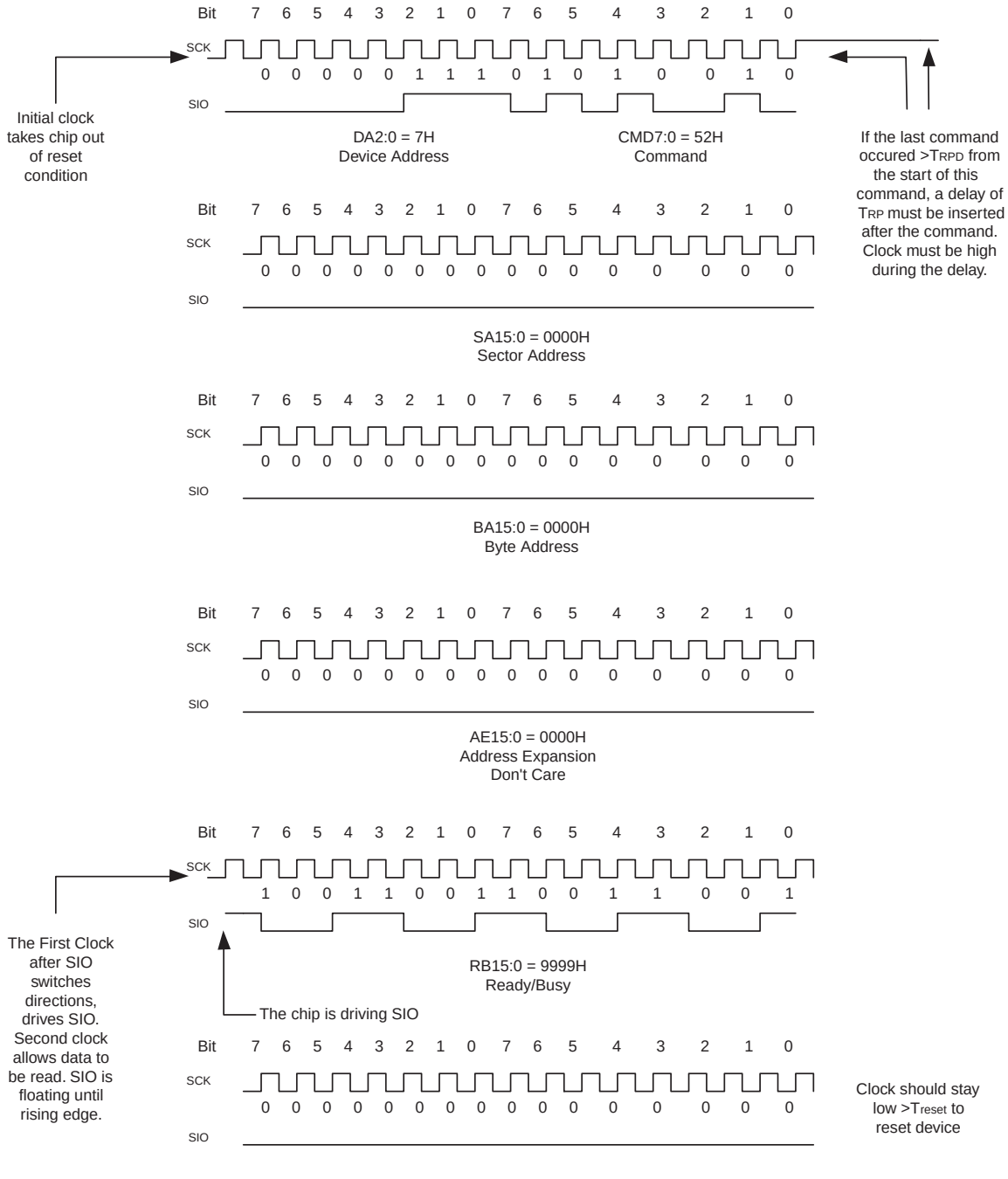
AC ELECTRICAL CHARACTERISTICS (Preliminary)

		16 MHz				
Symbol	**Description**	**Min**	**Typ**	**Max**		**Unit**
t_{CYC}	SCK Serial Clock Period With RCE=1	62	—	—		ns
t_{WH} t_{WL}	SCK Serial Clock High or Low Time	t_{CYC}/2	—	—		ns
t_{RI} t_{FI}	SCK Serial Clock Rise or Fall Time (2)	—	—	5		ns
t_{SU}	Data Input Setup Time to SCLK	20	—	—		ns
t_{IH}	Data Input Hold Time from SCLK	0	—	—		ns
t_V	Data Output Valid after SCLK (1,3)	—	—	25		ns
t_{LEAD}	$\overline{CS}$ Setup Time to Command	100	—	—		ns
t_{LAG}	$\overline{CS}$ Delay Time after Command	100	—	—		ns
t_{WP}	Erase/Write Program Time (4) *(see Command)*		—	10	15	ms
t_{EO}	Erase Only Time *(see Command)*	—	3	5		ms
t_{WO}	Write Only Time *(see Command)*	—	7	10		ms
t_{XS}	Transfer Sector *(see Command)*	—	—	100		µs
t_{HD}	SCK Setup Time to $\overline{HOLD}$	10	—	—		ns
t_{CD}	SCK Hold Time from $\overline{HOLD}$	30	—	—		ns
t_{CS}	$\overline{CS}$ Deselect Time	160	—	—		ns
t_{RB}	READY / BUSY Valid Time	160	—	—		ns
t_{DIS}	Data Output Disable Time	—	—	160		ns
t_{OH}	Data Output Hold Time After SCK	0	—	—		ns
t_{RP}	Prechange Delay for Read	—	—	10		µs
t_{RPD}	Delay Between Read Commands without t_{RP}	—	—	1		ms

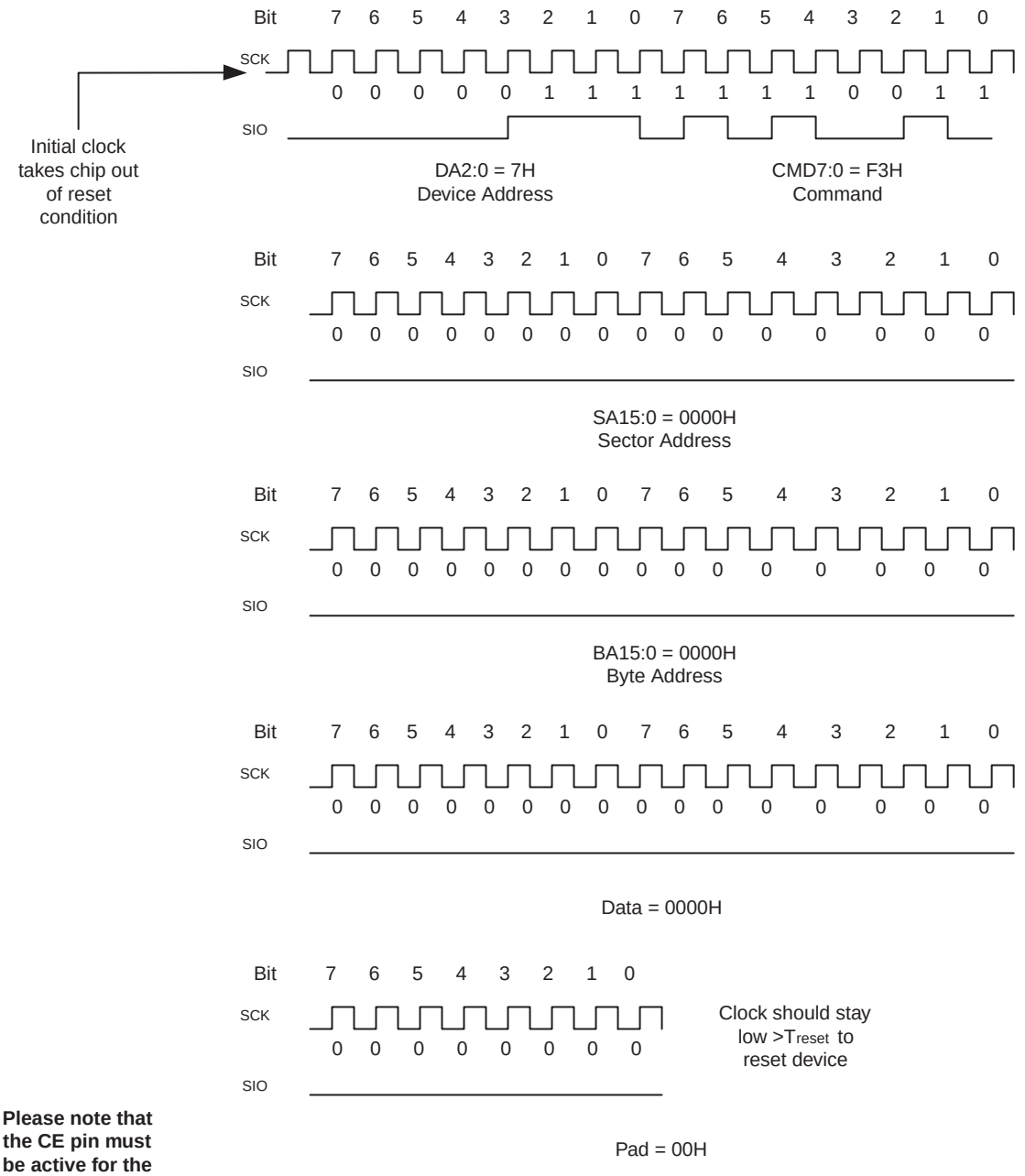
Notes:
1. To achieve maximum clock performance, the read clock edge will need to be set for rising edge operation in the configuration register (RCE=1).
2. Test points are 10% and 90% points for rise/fall times. All others timings are measured at 50% point.
3. With 30 pF (16 MHz) load SO to GND.
4. Maximum program time for 99% of sectors, <1% may require 4x this value.

CLOCK AND DATA TIMING





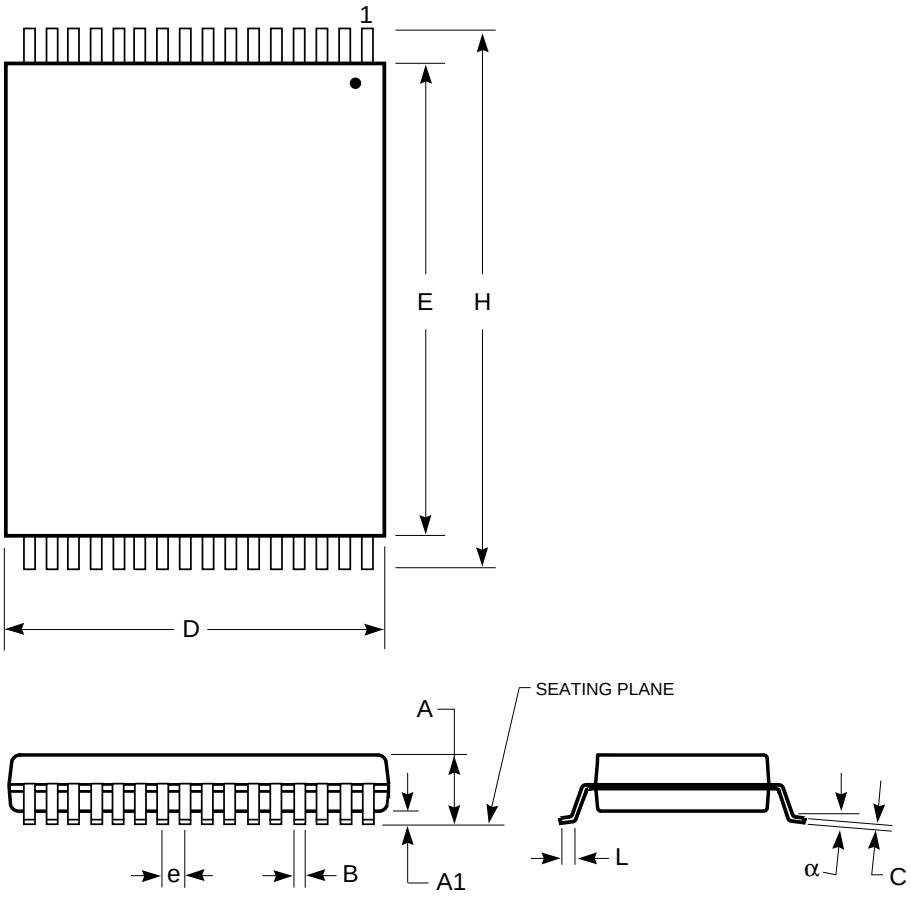
NXS Clock Diagram for Read Command



NXS Clock Diagram for Write Command

PACKAGING INFORMATION

Plastic TSOP - 32-pins
Package Code: Type I (T)



Plastic TSOP Type I (T)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	1.00	1.20	0.039	0.047
A1	0.05	0.20	0.002	0.008
B	0.15	0.25	0.006	0.010
C	0.10	0.20	0.004	0.008
D	7.80	8.20	0.307	0.323
E	18.30	18.50	0.720	0.728
H	19.80	20.20	0.780	0.795
e	0.55 BSC		0.022 BSC	
L	0.50		0.020	
a	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

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