SyncCAM-1R Module

NLM8x620R

Description

The NLM8x620R is a Synchronous Content Addressable Memory (SyncCAM®-1R) Module of up to 2M bits in density. The module consists of one, two, four, or eight monolithic NL84620R devices. The module can be used to perform high-speed parallel search operations on memory tables. Its primary application is as an address filter or an address translator for Fast Ethernet, Gigabit Ethernet, and ATM switches.

Features

- Match Flag times: 25/28 ns
- CAM Index output (pipeline mode): 14/16 ns
- Sustained searches of up to 33 Million/Second
- Separate 64-bit Comparand I/O bus, 32-bit Results bus and 14-bit Instruction bus
- Four 64-bit wide Mask Registers for easy masking of compare or write operations in each CAM
- 14-bit instruction bus enables single cycle execution of all instructions
- 3.3V TTL compatible CMOS, 168-pin DIMM Package

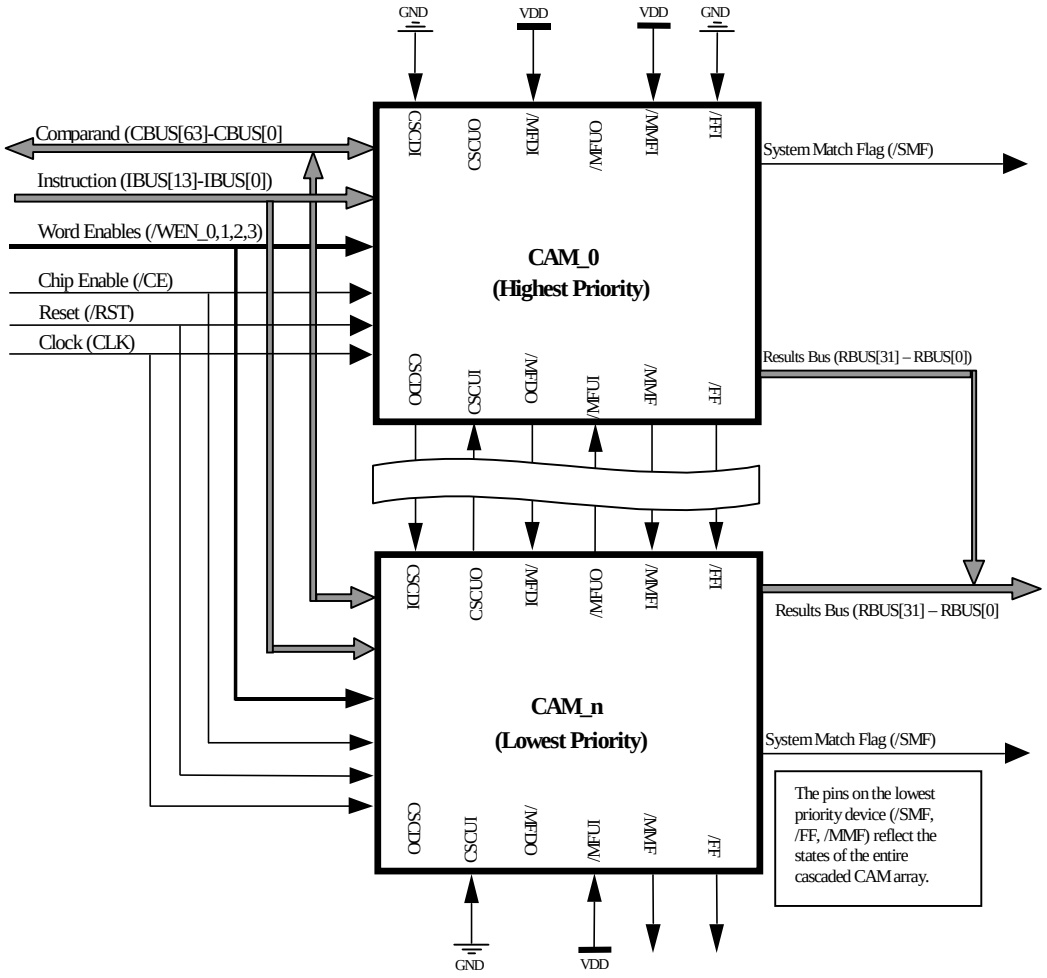


Figure 1 NLM8x620R Module Block Diagram

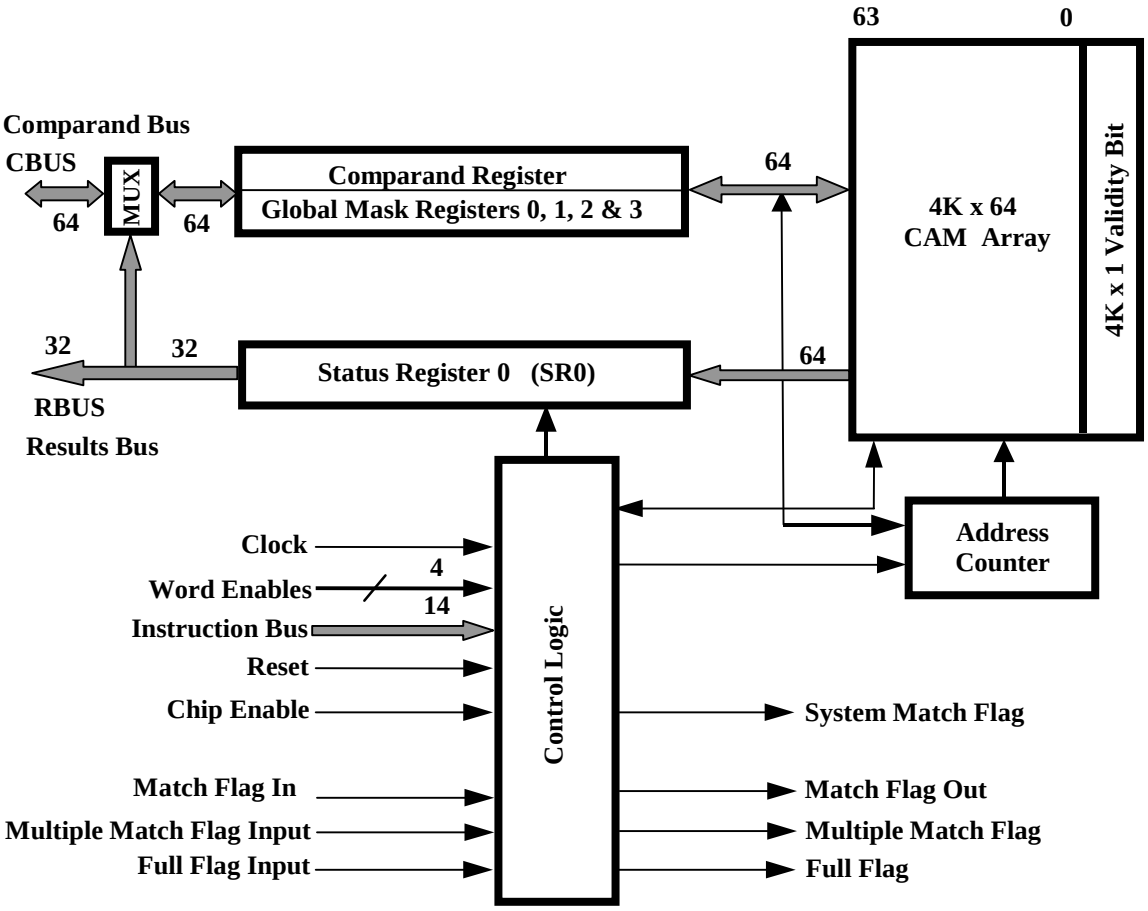


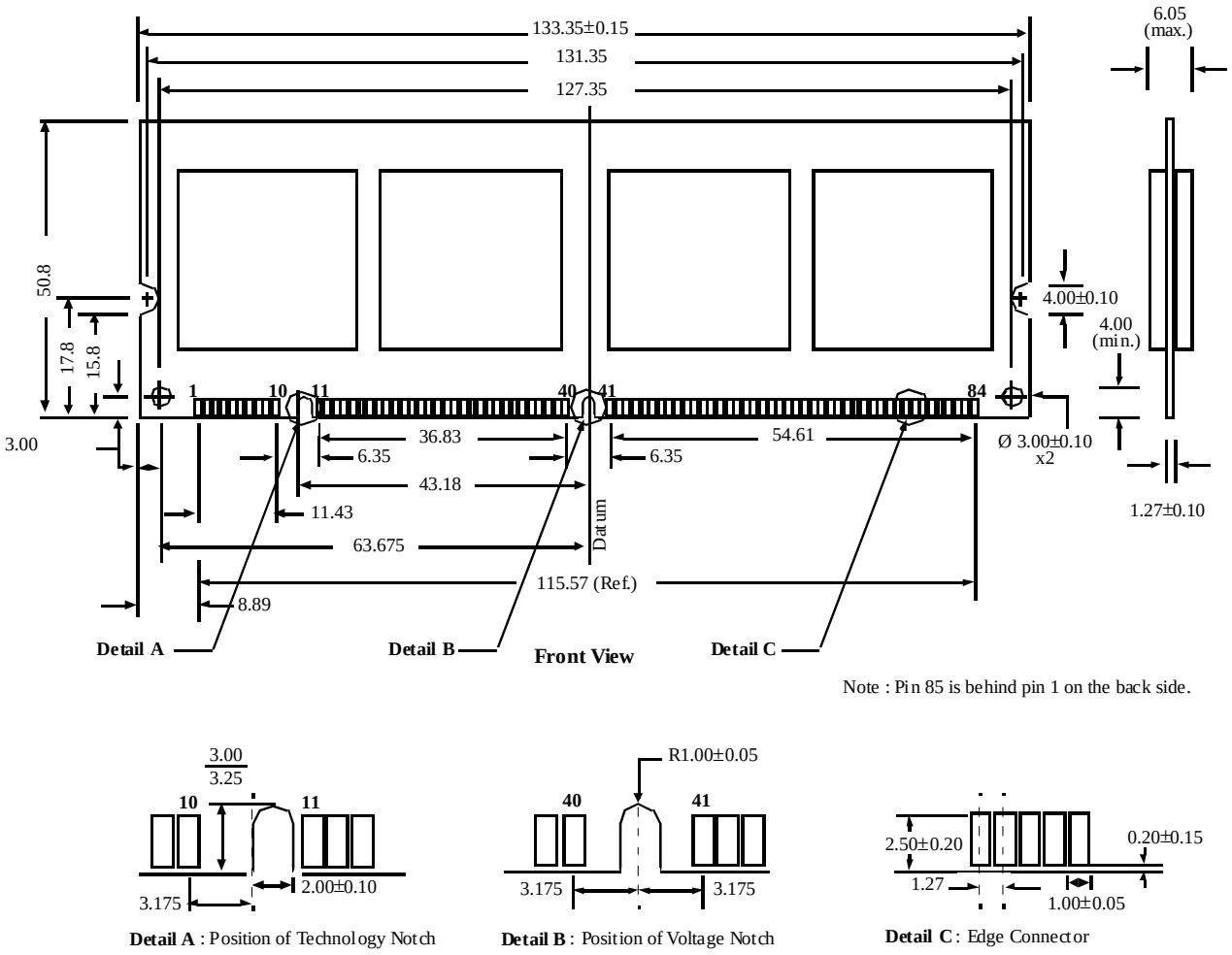
Figure 2 Individual Device Block Diagram

	Front Side	Rear Side	
1	GND	GND	85
2	C0	C32	86
3	C1	C33	87
4	C2	C34	88
5	C3	C35	89
6	VDD	VDD	90
7	C4	C36	91
8	C5	C37	92
9	C6	C38	93
10	C7	C39	94
	Left Key		
11	GND	GND	95
12	C8	C40	96
13	C9	C41	97
14	C10	C42	98
15	C11	C43	99
16	C12	C44	100
17	VDD	VDD	101
18	C13	C45	102
19	C14	C46	103
20	C15	C47	104
21	GND	GND	105
22	C16	C48	106
23	C17	C49	107
24	C18	C50	108
25	C19	C51	109
26	C20	C52	110
27	C21	C53	111
28	VDD	VDD	112
29	C22	C54	113
30	C23	C55	114
31	GND	GND	115
32	C24	C56	116
33	C25	C57	117
34	C26	C58	118
35	C27	C59	119
36	C28	C60	120
37	C29	C61	121
38	C30	C62	122
39	C31	C63	123
40	/RST	NC	124
	Center Key		
41	VDD	VDD	125
	Front Side	Rear Side	

	Front Side	Rear Side	
42	CLK	I13	126
43	GND	GND	127
44	WE0	I12	128
45	WE1	I11	129
46	WE2	I10	130
47	WE3	I9	131
48	VDD	VDD	132
49	/CE	I8	133
50	GND	I7	134
51	GND	GND	135
52	GND	I6	136
53	I0	I5	137
54	I1	I4	138
55	I2	I3	139
56	R0	R16	140
57	R1	R17	141
58	R2	R18	142
59	R3	R19	143
60	GND	GND	144
61	R4	R20	145
62	VDD	VDD	146
63	R5	R21	147
64	R6	R22	148
65	R7	R23	149
66	R8	R24	150
67	R9	R25	151
68	R10	R26	152
69	R11	R27	153
70	R12	R28	154
71	GND	GND	155
72	R13	R29	156
73	R14	R30	157
74	R15	R31	158
75	/FFI	/FF	159
76	VDD7	VDD10	160
77	/MFDI	/MFDO	161
78	/MFUI	/MFUO	162
79	/MMFI	/MMF	163
80	/SMF	GND	164
81	GND	GND	165
82	CSCDI	CSCDO	166
83	CSCUI	CSCUO	167
84	VDD	VDD	168
	Front Side	Rear Side	

Figure 3: NLM8x620R Pin Assignment (168 Pin DIMM)

Top and Bottom Half, Top View



(All dimensions are in millimeters with ±0.13mm tolerance unless specified otherwise.)

Figure 4 168 Pin DIMM Module Dimensions (units: mm)

1.0 Functional Description

The NLM8x620R is a Synchronous Content Addressable Memory (SyncCAM-1R) Module designed for use as an address filter or an address translator in 100/1000 Mb/s Ethernet and ATM switches and routers. This module can also be used to implement fast routing tables in Internet Protocol (IP) switches. The NLM8x620R has a total associative memory capacity of up to 2M bits organized with a width of 64 bits.

A bi-directional 64-bit Comparand Bus (CBUS) enables all internal registers and memory to be accessed. An output only, 32-bit Results Bus (RBUS) provides the CAM index and status information after a compare operation. A 14-bit Instruction Bus (IBUS) allows instructions to be presented to the module once every cycle. All operations on the module are timed synchronously with the rising edge of a free running clock. This architecture permits back to back compare cycles to be executed without any bus latencies.

Note: The registers below reside in each discrete NL84620R device and may be written to globally.

The Comparand Register (CR) is a 64-bit register that enables one to write the comparand data (key) and compare it with the contents of memory. This is the only register that enables a user to store and compare data with memory.

The NLM8x620R has four Global Mask Registers (GMR3-GMR0) that can each be selected on an operation by operation basis for write or compare operations. For a write operation, when the bits in these registers are programmed with '1's, the corresponding bits in memory will be masked, i.e. will not be modified. For compare operations, the corresponding bits in the associative data word will be forced to a match.

The 16-bit Device Configuration Register (DCR) enables the user to configure the module operation. The RBUS for the SyncCAM-1R Module operates in pipeline mode only. The address counter may be set to be incremented automatically during write and so on. See Table 3c for a complete list. After a hardware or software reset, the default mode is "Global Mode"

Status Register SR0 holds status information after compare, read, write or copy operations.

A 12-bit Address Counter (ACR) supplies the address to each monolithic NL84620R CAM on the module. This counter may be loaded with any valid start address and can be configured to increment once every cycle for read or write operations. This allows data to be loaded into or read out of the memory continuously.

Four Word Enable (/WEN3-/WEN0) inputs allow access to the internal registers and memory on 16-bit boundaries. These inputs allow matching to 16, 32 and 64 bit buses without glue logic.

The NLM8x620R can be clocked up to frequencies of 33MHz with a free running clock. A Chip Enable (/CE) input allows the module to be selected or deselected. The module has flag inputs and outputs that enable depth cascading without glue logic.

2.0 Pin Description

Note: While the code keying for this CAM module is compatible with the JEDEC Standard for LVTTL modules, this CAM module has both a different pinout and a different height than standard LVTTL (DRAM) DIMMs.

2.1 Clock (CLK):
This is a free running clock that is used to time all transactions on the CAM. The rising edge of the clock is the timing reference.

2.2 Chip Enable (/CE):
This is a synchronous input that selects the module for all operations when asserted Low. When asserted High, the module is deselected and is in idle mode. In idle mode, the CBUS and the RBUS are High-Z. For modules in idle mode (/CE asserted High) the Match, Multiple Match and System Match Flags are High and Full Flag is Low.

2.3 Reset (/RST):
This is an asynchronous input and provides the hardware reset for the module. During initialization, this pin must be asserted low for a minimum of *three (3) cycles*. This will set all CAM words to empty, initialize the control logic, and clear all registers. The reset operation must be followed by at least one NOP instruction. Table 2 and Tables 3a-f illustrate the logical states of the outputs and the registers after reset.

2.4 Word Enable (/WEN_0,1,2,3):
This is a synchronous input which enables access to the CAM array and all the registers with 16-bit granularity. For 64-bit entities in the CAM, /WEN_3 enables access to bits 63-48, /WEN_2 to bits 47-32, /WEN_1 to bits 31-16 and /WEN_0 to bits 15-0. These control pins are effective only for read and write to memory and the registers; for all other operations they are a "don't care".

2.5 Instruction Bus (IBUS[13]..IBUS[0]):
This is a synchronous 14-bit bus that provides the operation code (Opcode) to the CAM.

2.6 Comparand Bus (CBUS[63]..CBUS[0]):
This is a 64-bit synchronous I/O bus that conveys data to and from the memory and the registers.

2.7 Cascade Down Output (CSCDO):
For proper module operation this pin must be left unconnected.

2.8 Cascade Up Output (CSCUO):
For proper module operation this pin must be left unconnected.

2.9 Full Flag (/FF):
This is a synchronous output and is updated after Write to Memory, Copy to Memory, set VBIT or Set Full Flag operations. After reset, this pin is high. When the module is full, /FF is asserted low.

2.10 System Match Flag (/SMF):
This synchronous output provides the System Match Flag (either for single module or cascaded modules). This output is updated for all compare operations. After reset /SMF is high.

2.11 Multiple Match Flag (/MMF):
This synchronous output provides the Multiple Match Flag. This output is updated for all compare operations. After reset /MMF is high.

2.12 Results Bus (RBUS[31]..RBUS[0]):
This is a 32-bit synchronous bus (RBUS) that outputs the results of a compare operation. During a compare operation, when there is no match, RBUS is High-Z. For a compare operation, when there is a match, this bus outputs the CAM index of the Highest Priority Match (HPM), the Device ID, and the status of the flags.

The CAM index of HPM will be output on RBUS[31] through RBUS[20]. The lower 12 bits of Device ID are output on RBUS[19] through RBUS[8]. Bits RBUS[7] through RBUS[5] are reserved and will read '0'. RBUS[4] is the match flag status and will reflect the state of the external /MF pin. RBUS[3] is the multiple match flag status and will reflect the external /MMF pin. RBUS[2] is the full flag status and will reflect the state of the external /FF pin. RBUS[1] is reserved and will read '0'. RBUS[0] will reflect the state of the validity bit – '0' for Valid or '1' for empty, when a compare operation is issued referencing the validity bit.

The SyncCAM-1R Module operates in **pipeline mode** only. In pipeline mode, the results of a compare instruction are output on RBUS in the following cycle.

The user must set bit b7 to '1' in the Device Configuration Registers of each CAM device in the module to setup the RBUS to be in pipeline mode. **The default setting of this internal register after a hardware or software reset is '0'.** Refer to Table 3c for more details.

2.13 Full Flag Input (/FFI)
For proper module operation this pin must be connected to GND.

2.14 Match Flag Up Input (/MFUI)
For proper module operation this pin must be connected to Vdd.

2.15 Match Flag Down Input (/MFDI)
For proper module operation this pin must be connected to Vdd.

2.16 Multiple Match Flag Input (/MMFI)
For proper module operation this pin must be connected to Vdd.

2.17 Cascade Down Input (CSCDI)
For proper module operation this pin must be connected to GND.

2.18 Cascade Up Input (CSCUI)
For proper module operation this pin must be connected to GND.

2.19 Match Flag Up Output (/MFUO)
For proper module operation this pin must be left unconnected.

2.20 Match Flag Down Output (/MFDO)
For proper module operation this pin must be left unconnected.

3.0 SyncCAM-1R Module Internal Registers

Note: Each device in the SyncCAM-1R Module contains each of the following registers.

3.1 Status Register (SR0)
The Status Register SR0 holds the results of Compare, Read, Write or Copy operations. The RBUS outputs results after a comparison in SR0 format. The user can also access the Status Register from the CBUS by executing a "read status register" instruction. The table 3b describes the contents of these registers after reset. Note: This register is read only and is updated internally. Table 3i describes the contents of this register after all other operations.

3.2 Comparand Register (CR)
The Comparand Register (CR) is a 64-bit register for loading the comparand (key) data for compare and other operations. For bus widths of 16 or 32 bits, the Word Enable (/WEN3-/WEN0) inputs enable the user to load data into the CR and then compare its contents with the contents of memory. This feature enables the SyncCAM-1R Module to interface to buses that are 16, 32 and 64-bit wide seamlessly. This is the only register that enables the user to store and compare data with memory.

3.3 Global Mask Registers (GMR)
There are four 64-bit Global Mask Registers (GMR) that may be used either to mask compares or to mask data during memory writes. Each GMR may be selected on a cycle by cycle basis by specifying the GMR address in the instruction.

For compare instructions calling for a masked compare, if a mask bit is '1', the corresponding bits in the memory will not enter the compare operation. If a mask bit is '0', the corresponding bits in the memory will enter the compare operation.

For memory write instructions calling for a masked write, if a mask bit is '1', the corresponding bits in the memory will not be altered. If a mask bit is '0', the corresponding bits in the memory will be written to.

3.4 Highest Priority Match Index Register (HPMR) (In each CAM device)
This register holds the address of the highest priority match. This register is updated after all compare operations. This register is read only and is updated internally. See table 3a.

3.5 Next Free Address Register (NFAR) (In each CAM device)
This register holds the address of the next free address in the array. This is updated for all write to memory, copy to memory, and set VBIT instructions. This register is read only and is updated internally. See table 3a and Section 5.0.

3.6 Device Configuration Register (DCR)
This register holds the bits for selecting modes of operation of the CAM module. This register includes a field (read only) indicating the type of device. If the user wants the address Counter to be auto incremented during read and write operations, bit b4 needs to be set to a "1". **Bit b7 must be set to a "1" for proper Module operation (pipeline mode). For details, see table 3c.**

3.7 Device ID Register (DIDR)
This register holds the Device ID value. This register is written into as part of the initialization sequence. This register is reset only during hardware reset. The software reset instruction does not alter this register. See table 3b.

Note: All registers may be globally written with the exception of the Device ID Register

Table 1: Logical State of the Outputs with /CE High

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results bus	RBUS	High-Z
System Match Flag	/SMF	Same as Match Flag Down Input (/MFDI)
Multiple Match Flag	/MMF	Same as Multiple Match Flag Input (/MMFI)
Full Flag	/FF	Same as Full Flag Input (/FFI)

Table 2: Logical State of the Outputs after Hardware or Software Reset

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results Bus	RBUS	High-Z
System Match Flag	/SMF	High
Multiple Match Flag	/MMF	High
Full Flag	/FF	High

Table 3a: Address Counter, NFAR, and HPM Registers after Hardware or Software Reset (In each CAM device)

b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0

Table 3b: Status Register 0 (SR0) after Hardware or Software Reset (In each CAM device)

b63 b52	b51 b40	b39 b37	b36	b35	b34	b33	b32
CAM Index	**Device ID [a]**	**RSV**	**/MF**	**/MMF**	**/FF**	**RSV**	**Vbit**
0 0 0 Hex	0 0 0 Hex	000	1	1	1	0	1

a) Only the lower 12-bits of the Device ID Register will appear. This field is unchanged after software reset.

Table 3c: Device Configuration Register (DCR) after Hardware or Software Reset (In each CAM device)

b15 b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type [b]	**RSV**	**Mode [c]**	**RSV**	**RSV**	**ACNT**	**RSV**	**RSV**	**RSV**	**RSV**
000 0000	0	0	0	0	0	0	0	0	0

b) 000 0000 indicates a 4K x 64 SyncCAM-1. This entry is read only.

c) Bit b7 must be set to 1 after hardware or software reset for proper SyncCAM-1R Module operation.

Note: Tables 3d and 3e are intentionally omitted.

Table 3f: State of the SyncCAM-1R Module after Hardware or Software Reset (In each CAM device)

#	Memory, Registers and Outputs	Status after Hardware Reset	Status after Software Reset
1	Device ID Registers	All bits reset to '0'	Remains **unchanged**
2	Address Counter	All bits reset to '0'	All bits reset to '0'
3	Next Free Address Register	All bits reset to '0'	All bits reset to '0'
4	Global Mask Registers	All bits reset to '0'	All bits reset to '0'
5	Status Register 0	See table 3b	See table 3b
6	Device Configuration Registers	See table 3c	See table 3c
7	Memory [d]	Undefined	Undefined
8	Vbit in Memory	Empty=1	Empty=1
9	Full Flag	Reset to '1'	Reset to '1'
10	Comparand Bus (CBUS)	High-Z	High-Z
11	Results Bus (RBUS)	High-Z	High-Z
12	System Match Flag (/SMF)	High	High
13	Multiple Match Flag (/MMF)	High	High

d) Memory indicates CAM Words and Local Mask Words

Table 3g: CBUS State under Operating Mode and Control Inputs

Control Inputs State	Comparand Bus (CBUS) State
Reset (/RST) = Low	High-Z
Chip Enable (/CE) = High	High-Z
Chip Enable (/CE) = Low	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z

Global Device Mode Operation, /RST='1', /CE='0'	
Highest Priority Device (/MFDI='1' & /MFDO='0')	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
Device with Next Free Address (/FFI='0' & /FF ='1')	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
All Other Devices in the Module	High-Z

Single Device Mode Operation, /RST='1', /CE='0'	
Selected Device (Device with Matching Device ID)	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
All Other Devices in the module	High-Z

Table 3h: Device Configuration Register Format (In each CAM device)

b15 b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type	RSV	Mode	RSV	RSV	ACNT	RSV	RSV	RSV	RSV

Notes:

b15-b9 CAM Type field. Reads "000 0000" for 4K x 64 SyncCAM-1R. This CAM Type field is read only.

b8 Reserved. Will read '0'.

b7 This bit must be set to "1" for proper module operation. This bit is set to '0' after reset. (Hardware or Software)

b6 Reserved. Will read '0'.

b5 Reserved. Will read '0'.

b4 When set to '1' this bit enables the **Address counter** to be **incremented**. When set to '0' it disables the address counter incrementing. This bit is set to '0' after Hardware or Software reset.

b3-b0 Reserved. Will read '0'. Do not write to these bits.

Table 3i: Status Register 0 (SR0) Format (In each CAM device)

b63 b52	b51 b40	b39 b37	b36	b35	b34	b33	b32
CAM Index	Device ID	RSV	/MF	/MMF	/FF	RSV	Vbit

Notes:

b63-b52 CAM Index field. Updated after all compare instructions. Updated with Highest Priority Match (HPM) index when there is a match.

b51-b40 Lower 12 bits of the 16-bit Device ID. Updated when Device ID is written.

b39-b37 Reserved; will read '000'.

b36 Match flag. Updated after all compare operations; reflects the internal match flag status.

b35 Multiple match flag. Updated after all compare operations; reflects the internal multiple match flag status.

b34 Full flag. Updated after write to memory, copy to memory, or set VBIT instructions; reflects internal full flag status.

b33 Reserved; will read '0'.

b32 Vbit (valid or empty). Updated after all compare operations with the type of words compared; updated with the settings of VBIT after write to memory or copy to memory; updated with VBIT after set VBIT operation.

4.0 CAM Address Counter (ACR)

The CAM Address Counter (ACR) in the SyncCAM-1R Module allows a user to perform read, write or copy operations continuously. The user may set the start address in the counter and program the Device Configuration Register to increment the counter after write, read or copy operations. The ACR is set to increment by setting bit b4 in the Device Configuration Register to a '1'. When the counter is set **not to Increment**, (bit b4='0'), then the counter address will not increment even for instructions that specify that the Address Counter be incremented.

When the CAM Address Counter is **set to increment** in the Device Configuration Register, the counter will be incremented after any of the following instructions are executed:

1. Copy operations to and from memory that reference the address counter.
2. Set VBIT to Valid or Empty at the address indicated by the Address Counter.
3. Write to memory and set VBIT to Valid or Empty at the address indicated by the Address Counter.
4. Write to memory masked by Global Mask Register, set VBIT to Valid or Empty at the address indicated by the Address Counter.
5. Read memory at address indicated by the Address Counter and increment Address Counter.

The following memory operations that reference the Address Counter **do not increment** the Address Counter even if b4 in the Configuration Register is set to '1' (Increment):

1. Write to memory, no change to VBIT.
2. Read memory.
3. Read memory (CAM Word).

These restrictions should be kept in mind when interfacing SyncCAM-1R Modules to buses smaller than 64-bits wide.

5.0 Next Free Address Register (NFAR)

The Next Free Address Register (NFAR) holds the address of the memory word that has its VBIT set to Empty, and that is numerically closest to zero. This is noted as the Next Free Address (NFA). This address is generated from the output of the priority encoder in the IPCAM-1R Module. When the device has no empty locations the NFAR holds the address of the last empty location before the device became full.

The following operations will update the NFAR:

1. Write to Memory at NFA; set VBIT to Valid.
2. Set VBIT to empty at the Address indicated by the Address Counter.
3. Set VBIT to empty at HPM address.
4. Set VBIT to empty at all matching locations.
5. Copy operations that reference the NFAR.

The NFAR will **not be updated** for the following operation:

1. Write to memory at next free address; no change to VBIT.

These restrictions should be kept in mind when interfacing SyncCAM-1R Modules to buses smaller than 64-bits wide or when updating memory in segments smaller than 64-bits wide.

6.0 Validity Bit

Every location in the memory array has a corresponding Validity bit associated with it. This bit is referred to as the VBIT. This bit can be written to or read from just like locations in memory. Any Compare instruction indicates the type of words to be searched during the cycle and only words belonging to that group participate in the search operation; all other words not belonging to the group do not participate in the match operation (indicate a no match). After hardware/software reset all words belong to the "Empty" group.

When the Validity bit is set to reflect the Valid State for a particular word, then that particular word will take part in compare operations only when the compare operation with VBIT set to valid instruction is executed.

7.0 Initializing the SyncCAM-1R Module

Each device in the SyncCAM-1R Module needs to be initialized after power up for proper operation. The following steps show how to initialize the SyncCAM-1R Module.

7.1 Module Initialization

1. Assert /RST pin low for a minimum of three cycles.
2. Execute NOP instruction (at least once).
3. Write to Device ID Register (any 16-bit value).
4. Set Full Flag.
5. Write to Device ID Register (any 16-bit value).
6. (Repeat 4 & 5 until all devices have ID written).
7. Execute a software Reset.
8. Execute NOP instruction (at least once).
9. Write to Device Configuration Register and set bit b7 to “1”.

The Device IDs must all be unique for proper operation. At step 3, the first device has the ID written; at step 5, the second device has the ID written and so on. The SyncCAM-1R Module is now ready for memory write, compare and other operations.

8.0 Writing to the CAM Module

After initialization, the user can write into the SyncCAM-1R Module in many ways. Two common methods of accomplishing this are described below:

8.1 Writing to Memory: Option 1

One method of writing into the CAM array is to execute “Write to memory at next free address and set VBIT to Valid” instruction repeatedly until the memory is full or all data is written into the CAMs. The write operation begins in the module with /FFI = 0 and /FF=1, and continues until all locations have been written into (no EMPTY locations remain). When the last empty location has been written to, the /FF of that device will assert a ‘0’ preventing any further “Write to memory at NFA” operations from occurring in that device. This will then enable the next lower priority device in the cascade to accept “Write to memory at NFA” operation. This continues until the last device in the module becomes full and asserts /FF pin low, indicating that all the CAM devices are now full, and no empty locations remain.

8.2 Writing to the Memory: Option 2

Another method of writing to the CAM is to use the address from the internal address counter as opposed to the NFAR. The steps involved in this method are as follows:

1. Select Single Device Mode with Device ID on the least significant bits of the CBUS.
2. Write to memory at address from ACR and set VBIT to valid.
3. Repeat Step 2 as many times as needed to fill the device. The user must keep track of the word count in order to determine when an individual device within the module is full.
4. Select Single Device Mode (Select another device).
5. Repeat steps 2-4 until all devices or full or no more entries are desired.
6. Select Global Device Mode

The above sections 9.1 and 9.2 show two of many possible ways of writing to the Memory Array.

When interfacing the SyncCAM-1R Module to a bus smaller than 64-bits and updating memory in segments (16/32-bits), the user is advised to execute either “Write to memory at NFA, no change to VBIT” or “Write to memory, no change to VBIT” followed by “Write to memory at NFA and set VBIT” or “Write to memory and set VBIT”.

9.0 Electrical Characteristics

9.1 Absolute Maximum Ratings [a]

Supply voltage to GND	+0.5 to +4.6V
DC output voltage (Vout)	-0.5 to VDD + 0.5V [b]
DC output current	50mA [c]
T_{BIAS} Temperature under bias	-40°C to +85°C
T_{STG} Storage temperature	-65°C to +150°C

a) Stresses greater than ABSOLUTE MAXIMUM RATINGS will cause permanent damage to the module, resulting in functional or reliability type failures.
b) -2.0V for 10 ns, measured at the 50% point.
c) Per output, one at a time, one-second duration.

9.2 Power Supply Characteristics

			33 MHz	25 MHz	
Symbol	**Parameter**	**Test Conditions**	**Max.**	**Max.**	**Unit**
I_{DDO}	Operating Current	$t_{CYC} = t_{CYC}$ (min)	TBD	TBD	mA
I_{SB}	Idle Mode Current	/CE = '1'	TBD	TBD	mA

9.3 Capacitance

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Input Capacitance	TBD	pF	f=1MHz, V_{IN}=0V
C_{OUT}	Output Capacitance	TBD	pF	f=1MHz, V_{OUT}= 0V

9.4 DC Electrical Characteristics over Operating Range (T_A = 0°C - 70°C, VDD = 3.3V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Max.	UNIT
V_{IH}	Input HIGH Voltage	Logic high for all Inputs	2.2	VDD + 0.5	V
V_{IL}	Input LOW Voltage	Logic low for all Inputs	-0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA, VDD = Min.	2.4	-	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA, VDD = Min.	-	0.4	V
I_{LI}	Input Leakage	VDD = 3.47V; GND ≤V_{IN}≤VDD	-5	5	µA
I_{LO}	Output Leakage	GND ≤ VOUT ≤ VDD	-10	10	µA

10.0 AC Timing Parameters:

#	Parameter	Type	Description	33MHz		25 MHz	
				Min	Max	Min	Max
1	t_{CYC}	IN	Cycle	30		40	
2	t_{CYH}	IN	Cycle high	13.5		18.5	
3	t_{CYL}	IN	Cycle low	13.5		18.5	
4	t_{CSU}	IN	Chip Enable Set-up	4		5	
5	t_{CHD}	IN	Chip Enable Hold	0		0	
6	t_{WNSU}	IN	Word Enable Set-up	4		5	
7	t_{WNH}	IN	Word Enable Hold	0		0	
8	t_{DSU}	IN	Data Setup	4		5	
9	t_{DHD}	IN	Data Hold	0		0	
10	t_{INSU}	IN	Instruction Setup	4		5	
11	t_{INHD}	IN	Instruction Hold	0		0	
12	t_{RB1}	OUT	RBUS Data Output (Pipeline Mode)		14		16
13	t_{RB2}	OUT	RBUS Data Output Hold (Pipeline Mode)	1		1	
14	t_{RB3}	OUT	RBUS Data Output (Index in Flow Through Mode)		27		31
15	t_{RB4}	OUT	RBUS Data Output (Flags in Flow Through Mode)	_	_		33
16	t_{RBH}	OUT	RBUS Data Output Hold Time (Flow Through Mode)	2		2	
17	t_{CDO}	OUT	CBUS Data Output		25		30
18	t_{CDH}	OUT	CBUS Data Output Hold	2		2	
19	t_{MFI}	IN	Match Flag Input Setup	4		4	
20	t_{MF}	OUT	Match Flag Assertion and Deassertion (/MFDO, /MFUO)	2	25	2	28
21	t_{SMF}	OUT	System Match Flag Assertion and Deassertion	2	25	2	28
22	t_{MMF}	OUT	Multiple Match Flag Assertion and Deassertion	2	27	2	30
23	t_{FFI}	IN	Full Flag Input Setup	4		4	
24	t_{FF1}	OUT	Full Flag Assertion and Deassertion (Write, Copy instructions)	2	27	2	31
25	t_{FF2}	OUT	Full Flag Assertion and Deassertion (VBC instructions)	2		2	

1. **V_{DD} = 3.3V +- 5%, T_A=0°C – 70°C, V_{IH}/V_{IL} = 3.0V/0V.**
2. **All timings are with reference to the rising edge of the clock. All timing numbers in nano seconds.**
3. **Output hold times are guaranteed by design, but not tested in production.**

11.0 SyncCAM-1R Module Instruction Set

The SyncCAM-1R Module instruction bus is 14-bits wide. It consists of a 11-bit "Opcode field" consisting of bits 13-3, a 2-bit global mask field "GMSK" consisting of bits 2-1.

Instruction Word (Opcode) Format

IBUS13	IBUS12	IBUS11	IBUS10	IBUS09	IBUS08	IBUS07	IBUS06	IBUS05	IBUS04	IBUS03	IBUS02	IBUS01	IBUS00
W2			W1				W0				y1	y1	z0
Opcode Field											GMSK		0

IBUS[13:3]: Opcode field. This field determines all possible instructions.
IBUS[2:1]**:** Selects between the four Global Mask Registers.

#	IBUS02	IBUS01	Selects Global Mask Register
1	0	0	0
2	0	1	1
3	1	0	2
4	1	1	3

Instruction: **[Opcode field] [y1] [y0] [z0]**
[Opcode field] Bits 13 - 3, coded as [w2 w1 w0]; w2 is bits 13-11; w1 is bits 10 – 7; w0 is bits 6 - 3

12.0 SyncCAM-1R Module Instruction Opcodes and Descriptions

12.1 Compare Instructions

#	Opcode in Hex [Opcode][GMSK][0] [w2w1w0] [x] [0]	Instruction Description
1	[610] [0] [0] H	Compare Valid Entries
2	[614] [y1y0] [0] H	Compare Valid Entries using Global Mask Register
3	[620] [0] [0] H	Write to Comparand Register and Compare Valid Entries
4	[624] [y1y0] [0] H	Write to Comparand Register and Compare Valid Entries using Global Mask Register

12.2 Write Instructions (All write operations are controlled by the four Word Enables)

1	[000] [0] [0] H	NOP (No Operation)
2	[001] [0] [0] H	Write to Comparand
3	[002] [y1y0] [0] H	Write to Global Mask Register
4	[003] [0] [0] H	Write to Memory at address, No Change to VBIT
5	[004] [0] [0] H	Write to Memory at address, Set VBIT to Valid
6	[007] [y1y0] [0] H	Write to Memory at address, masked by Global Mask Register, No Change to VBIT
7	[008] [y1y0] [0] H	Write to Memory at address, masked by Global Mask Register, Set VBIT to Valid
8	[00C] [0] [0] H	Write to Memory at HPM address, Set VBIT to Valid
9	[013] [0] [0] H	Write to Memory at NFA, No change to VBIT
10	[014] [0] [0] H	Write to Memory at NFA, Set VBIT to Valid
11	[01B] [0] [0] H	Set VBIT to Valid at Address Counter
12	[01C] [0] [0] H	Set VBIT to Empty at Address Counter
13	[020] [0] [0] H	Set VBIT to Empty, at HPM address
14	[024] [0] [0] H	Set VBIT to Empty at all matching address

- All write functions are controlled by the four Word Enables.

12.3 Copy Instruction

#	Opcode in Hex [Opcode][GMSK][0] [w2w1w0] [x] [0]	Instruction Description
1	[02F] [0] [0] H	Copy Comparand Register to memory at NFA, Set VBIT to Valid

- Copy instruction is a 64-bit wide operation.

12.4 Local Mask Write Instructions

1	[050] [0] [0] H	Write to Local Mask Word
2	[051] [0] [0] H	Write to Local Mask Word and Increment Address Counter
3	[054] [0] [0] H	Write to Local Mask Word at Next Free Address

12.5 Special Instructions

1	[047] [0] [0] H	Write to Device Configuration Register
2	[048] [0] [0] H	Write to Device ID Register[a]
3	[04B] [0] [0] H	Set Full Flag [a]
4	[04C] [0] [0] H	Select Single Device Mode
5	[04D] [0] [0] H	Select Global Mode.
6	[04E] [0] [0] H	Software Reset [b]
7	[04F] [0] [0] H	Write Address Counter

a) This instruction will be executed in the device with /FI = 0 and /FF = 1. All other devices will treat this as NOP.
b) A Software instruction must be followed by a NOP instruction.

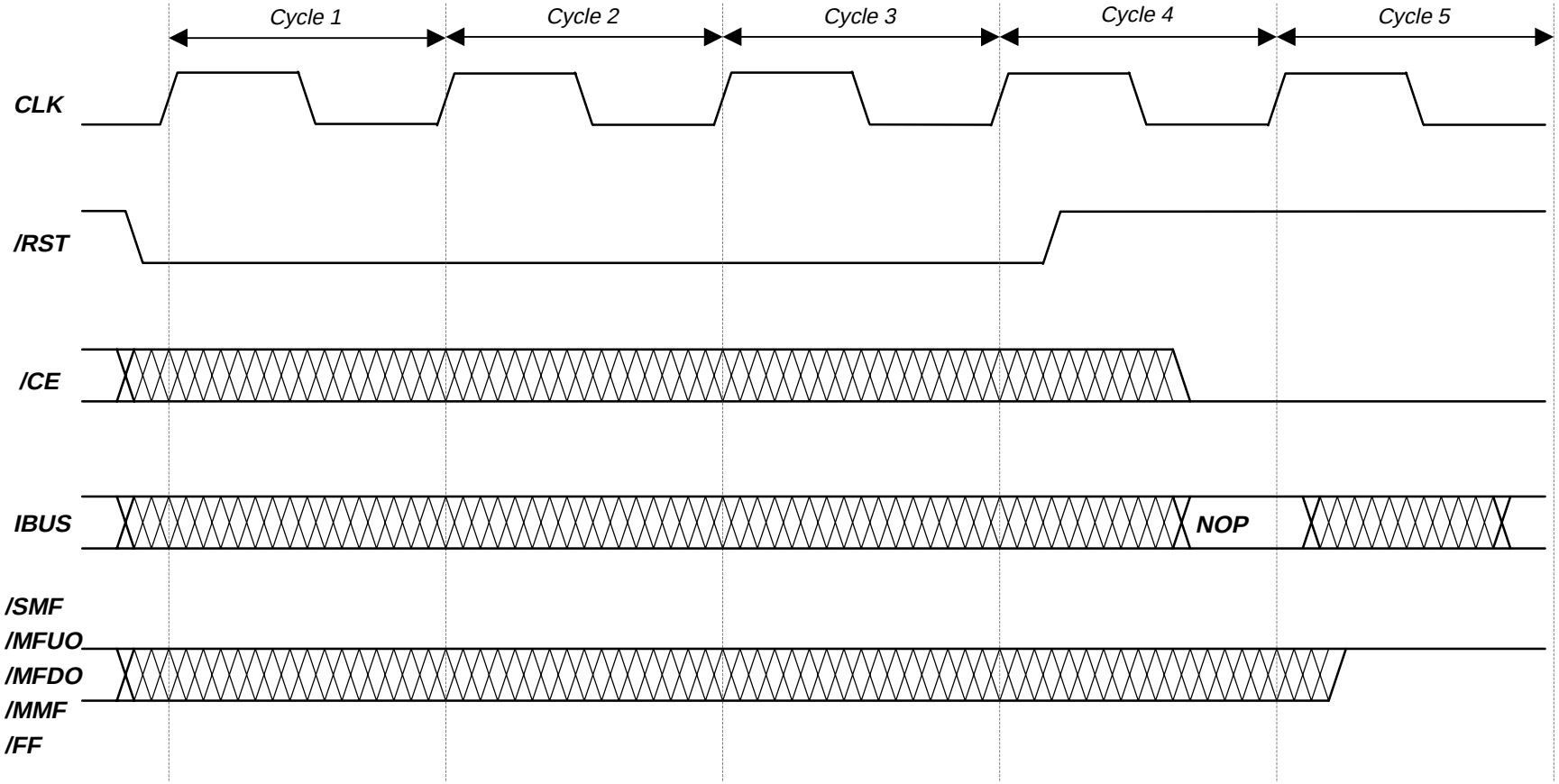
12.6 Read Operations

1	[200] [0] [0] H	Read Address Counter (Address output on CBUS[15:0]
2	[201] [0] [0] H	Read Memory
3	[202] [0] [0] H	Read Memory and Increment Counter
4	[203] [0] [0] H	Read Status Register
5	[204] [y1y0] [0] H	Read Global Mask Register
6	[205] [0] [0] H	Read Comparand Register
7	[206] [0] [0] H	Read Next Free Address Register [c]
8	[207] [0] [0] H	Read Memory at HPM Address
9	[209] [0] [0] H	Read Device Configuration Register (Data output on CBUS[15:0])
10	[20A] [0] [0] H	Read Device ID Register (Device ID output on CBUS[31:16])
11	[20B] [0] [0] H	Read Local Mask Word at Address
12	[20C] [0] [0] H	Read Local Mask Word at Address and Increment Counter
13	[20D] [0] [0] H	Read Local Mask Word at HPM Location

c) The NFA will appear on bits b15-b0 of the CBUS and the Device ID will appear on bits b31 - b16.

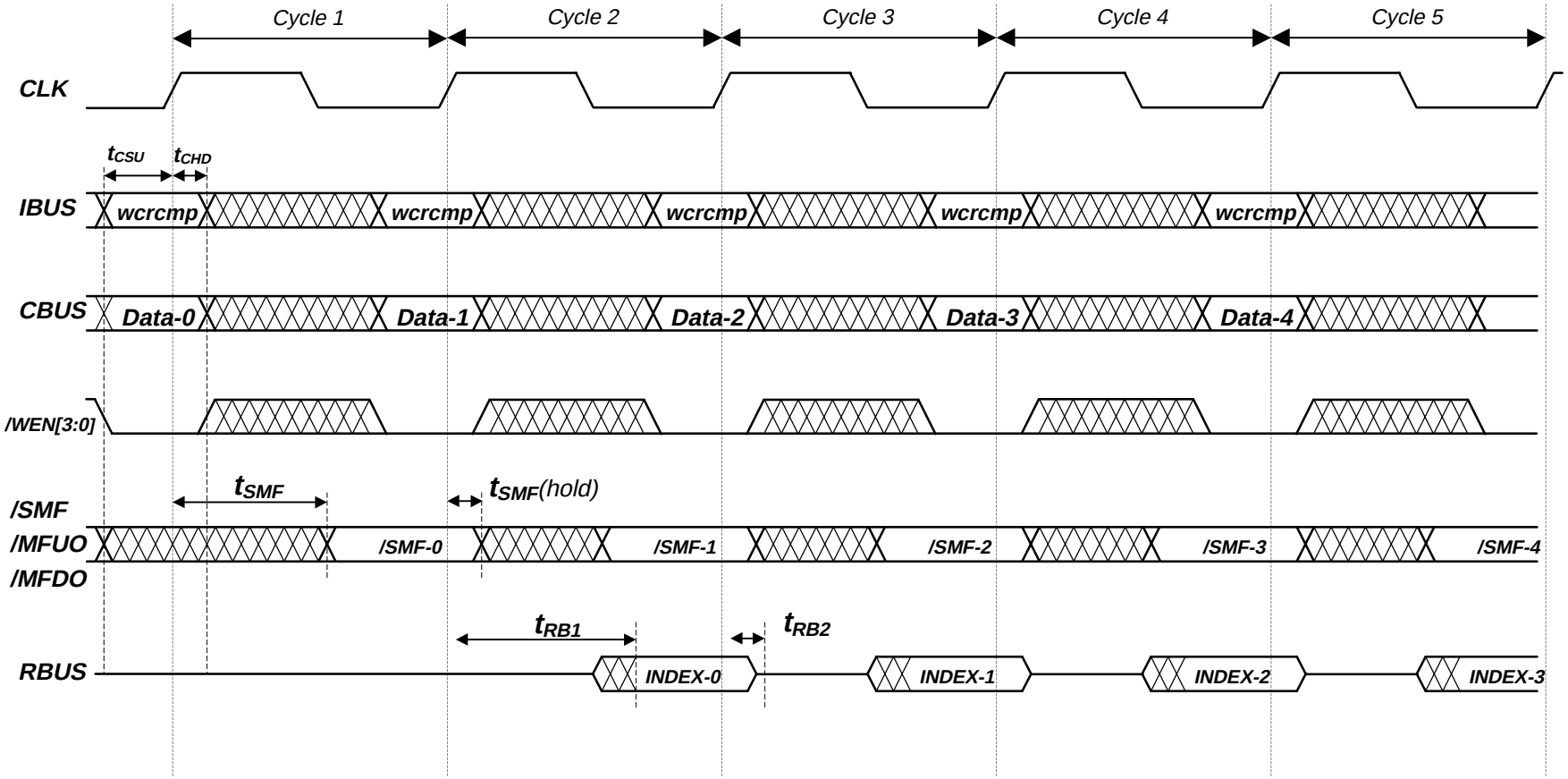
13.0 Timing Diagrams

RESET CYCLE



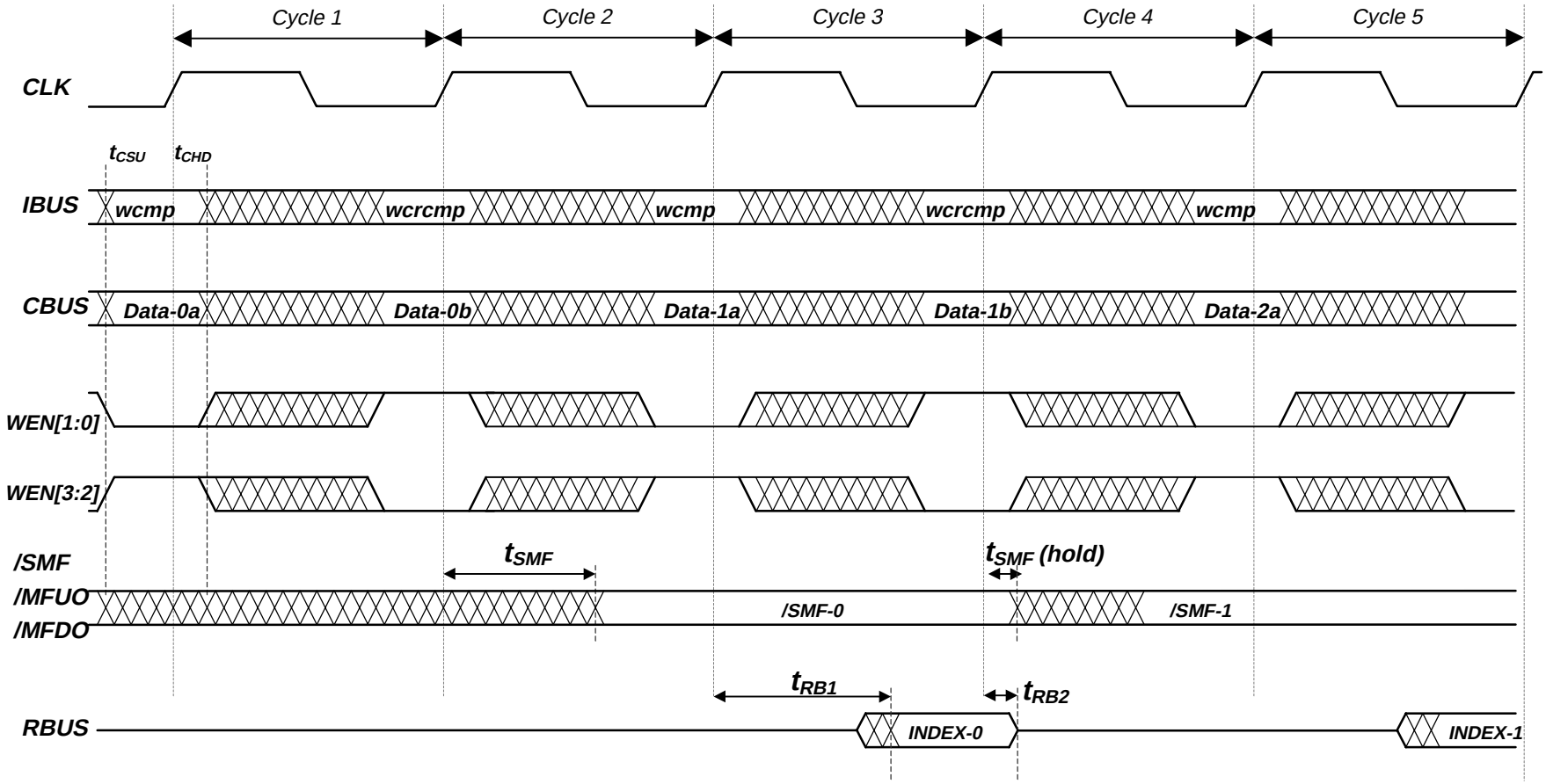
During Reset, CBUS[63:0], IBUS[13:0], and WEN[3:0] inputs are 'don't care'. RBUS is in High-Z. Reset must be followed by at least one "NOP" cycle.

64-bit Word Compare (64-bit interface)



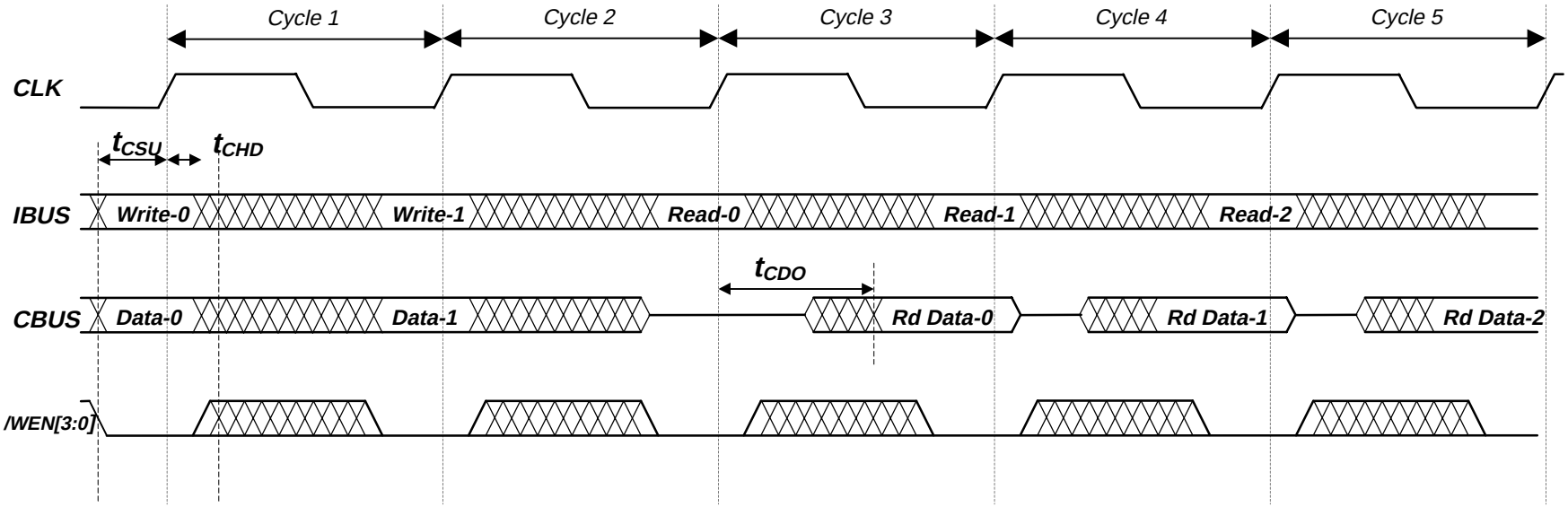
The Compare instruction is issued in the 1st cycle. The corresponding match flag is output in the 1st cycle and the RBUS output in the 2nd cycle. If a compare indicates no match (/SMF='1'), the corresponding RBUS output is High-Z. The instruction "Write to Comparand register and Compare" is denoted as "wcrcmp". /CE = '0' during these cycles. Bit b7 of the DCR must be set to '1' after software or hardware reset for proper SyncCAM-1R Module operation; this enables pipeline mode.

64-bit Word Compare (32-bit interface)



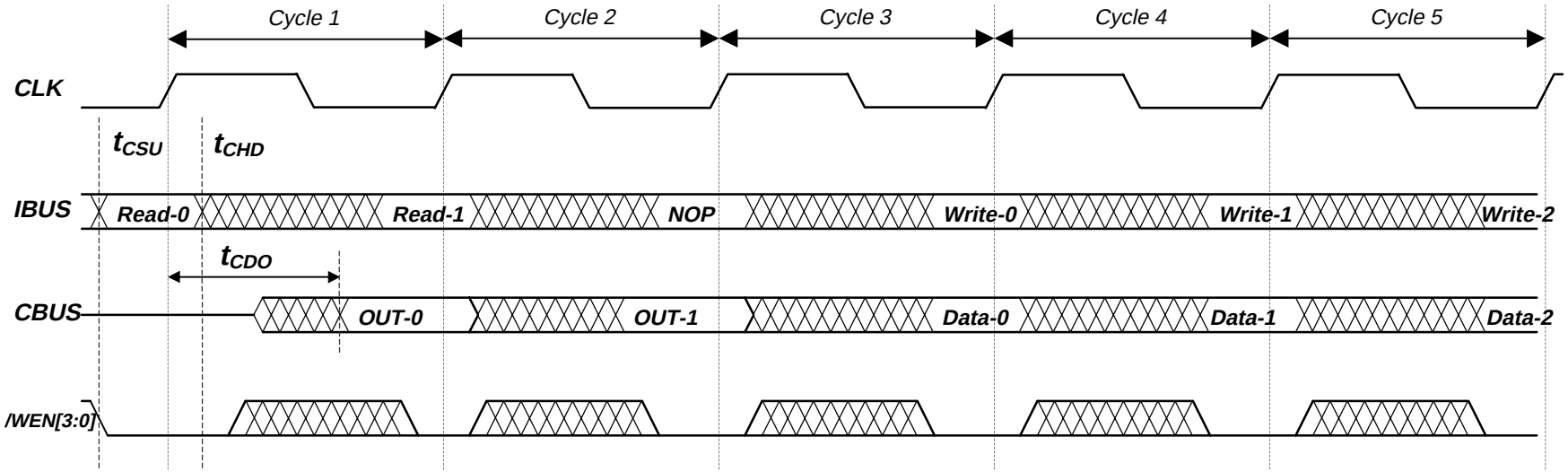
The Compare instruction is issued in the 2nd cycle. The corresponding match flag is output in the 2nd cycle and the RBUS in the 3rd cycle. If the compare instruction indicates no match (/SMF='1') the corresponding RBUS output is High-Z. The instruction "Write to Comparand" is denoted as "wcmp" and "Write to Comparand and Compare" as "wcrcmp". /CE = '0' during these cycles. Bit b7 of the DCR must be set to '1' after software or hardware reset for proper SyncCAM-1R Module operation; this enables pipeline mode.

Memory Write-Memory Read Cycles (64-bit interface)



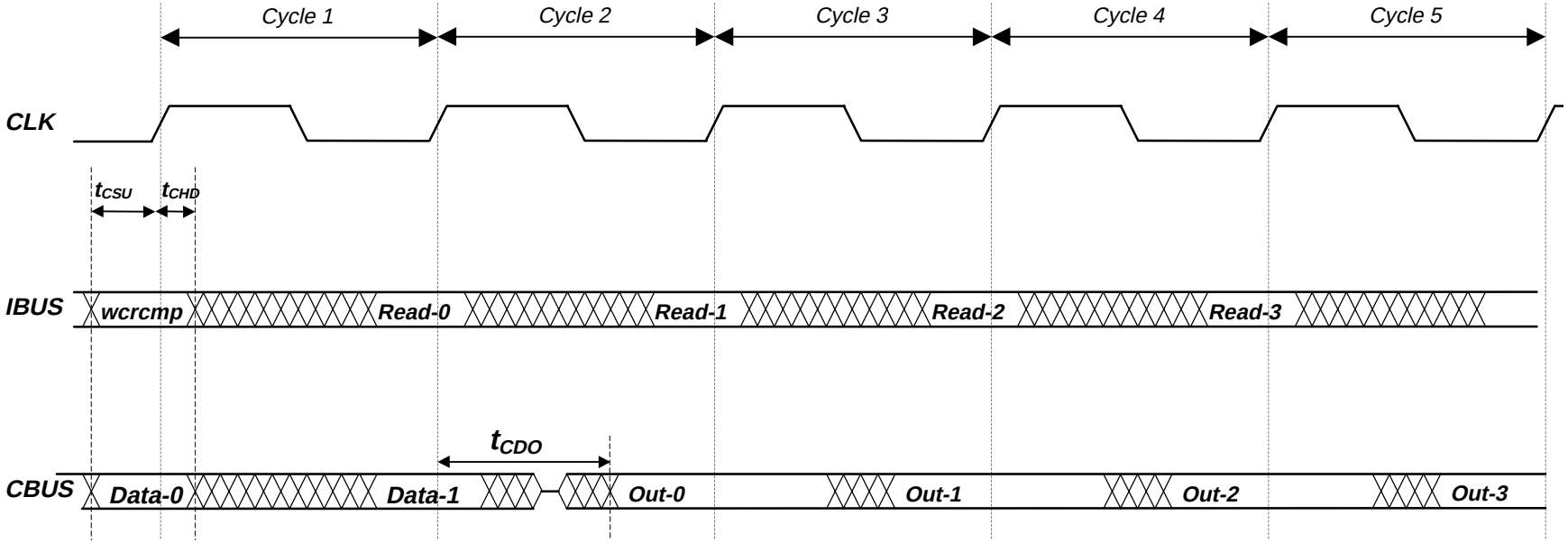
/CE = '0' during these cycles.

Memory Read-Memory Write Cycles (64-bit interface)



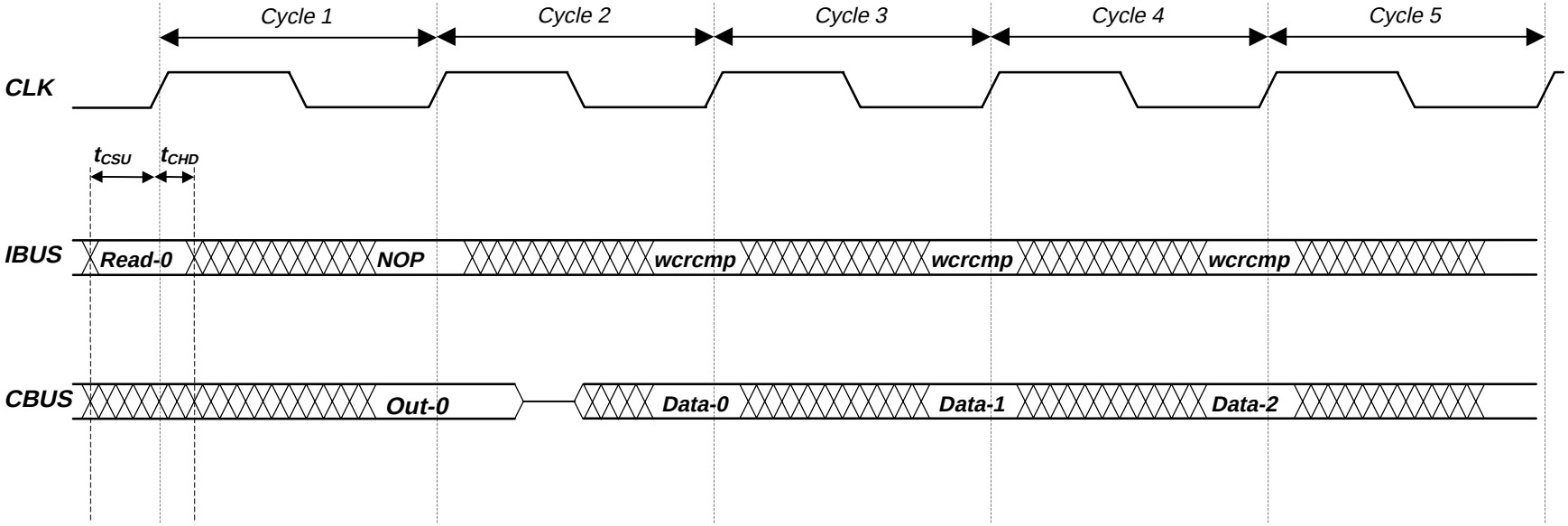
/CE = '0' during these cycles.

Compare/Memory Read Sequence



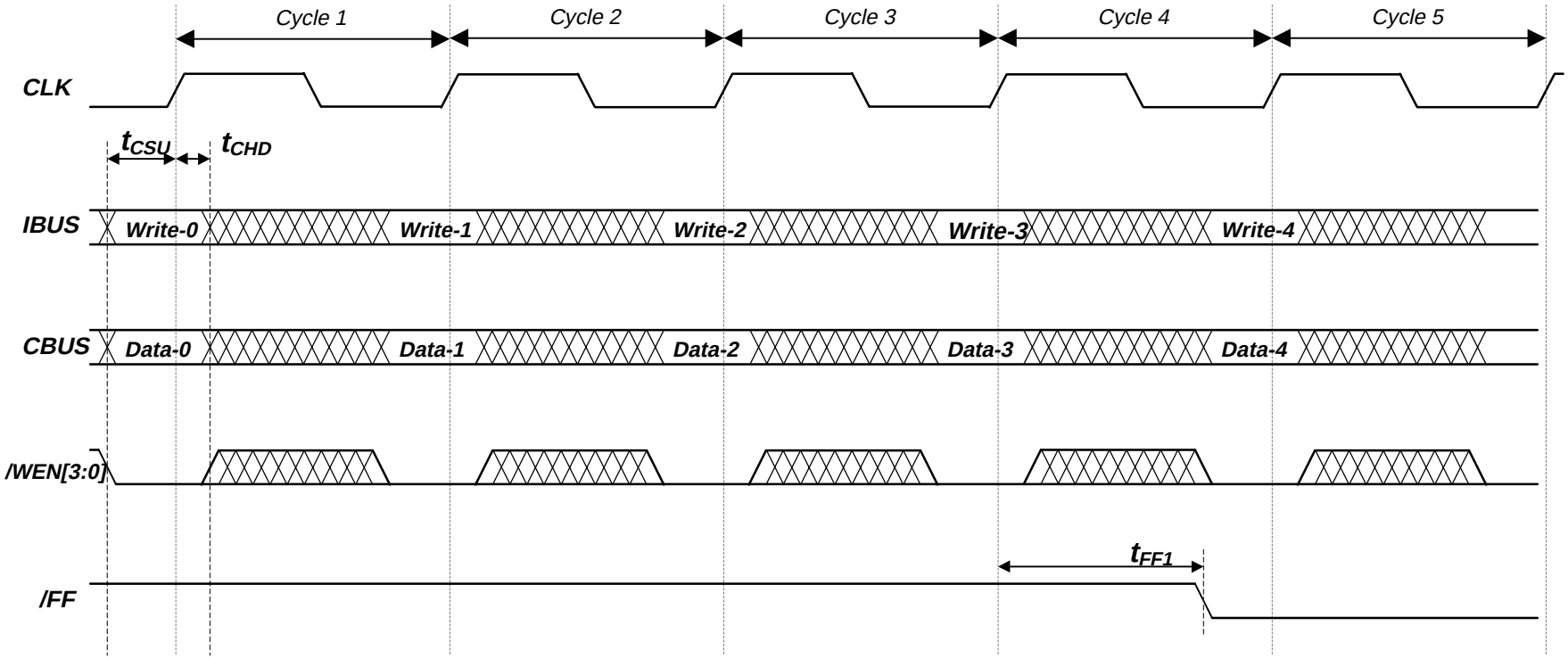
The compare instruction is issued in the 1st cycle.The instruction "Write to Comparand and Compare" is denoted as "wcrcmp". /CE = '0' during these cycles.

Memory Read/Compare Sequence (64-bit)



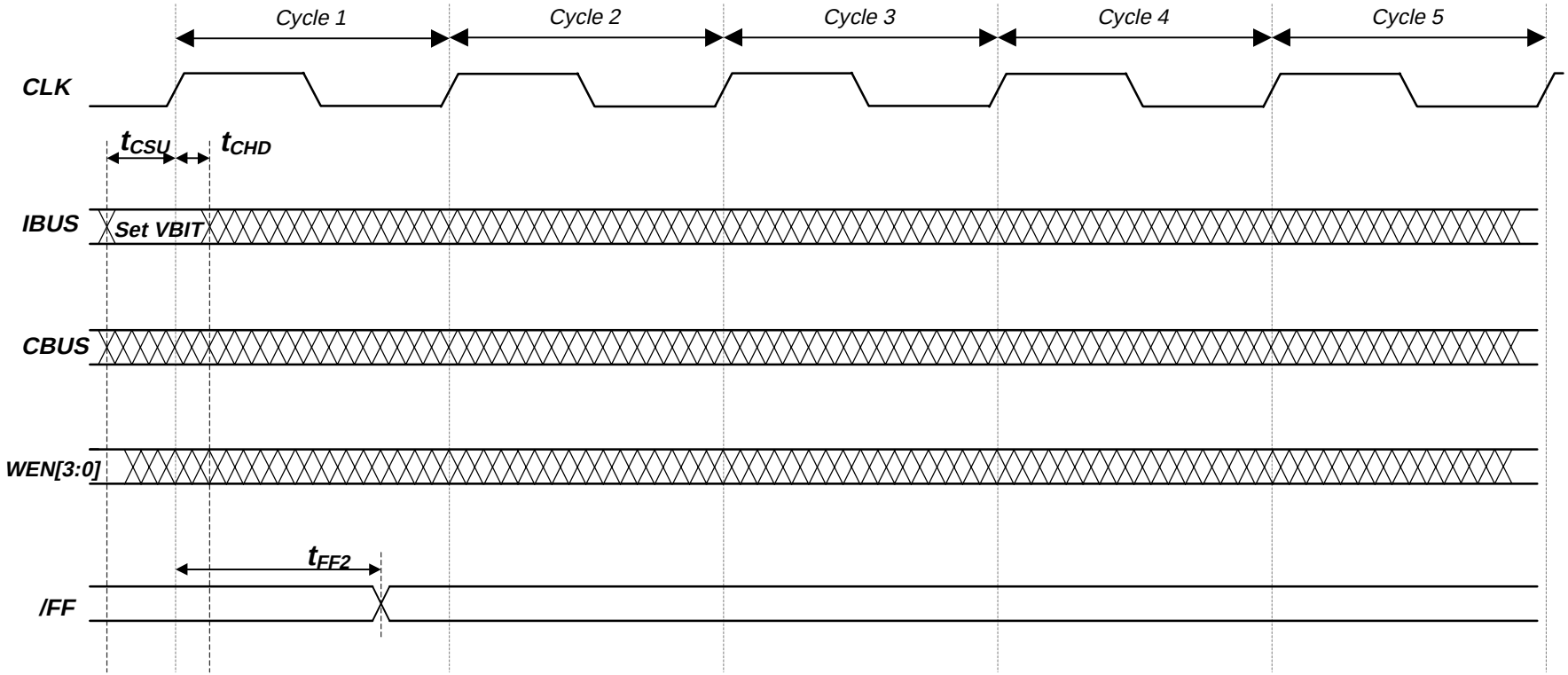
The instruction "Write to Comparand and Compare" as "wcrcmp". The /WEN[3:0] inputs are all '0'. /CE = '0' during these cycles.

Memory Write Operation and the Full Flag



The device becomes full <u>after</u> write-3 operation is completed. The Full Flag is asserted in the same cycle as shown. /CE = '0' during these cycles.

Validity Bit Operation and the Full Flag



If the device becomes full after the instruction is executed, the Full Flag is asserted; if the device was originally full and the instruction sets a location to empty, the Full Flag is de-asserted. The Full Flag assertion/Deassertion happens in the same cycle as the instruction. /CE = '0' during these cycles.

14.0 Ordering Information

Part Number	Cycle Time	Package	Comments
NLM84620R-33	33MHz	168 Pin DIMM	4K x 64
NLM84620R-25	25MHz	168 Pin DIMM	4K x 64
NLM85620R-33	33MHz	168 Pin DIMM	8K x 64
NLM85620R-25	25MHz	168 Pin DIMM	8K x 64
NLM86620R-33	33MHz	168 Pin DIMM	16K x 64
NLM86620R-25	25MHz	168 Pin DIMM	16K x 64
Please Consult Factory	33MHz	168 Pin DIMM	32K x 64
Please Consult Factory	25MHz	168 Pin DIMM	32K x 64

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Table of Contents