NUMA TECHNOLOGIES

Period to Digital (P/D) Converter
Microprocessor - Compatible

NT302

FEATURES

- **High Resolution Pulse / Period Measurement (8 ns)**
- **Suited for High Accuracy Frequency Measurement**
- **Applicable to both FM and ϕ Demodulation**
- **74 dB Dynamic Range - Wide Bandwidth 1MHz**
- **Single +5 Supply Voltage - CMOS Dissipation**
- **Directly Interfaces to Most DSPs and μPs**
- **Low Cost**
- **Buffered Data with Tri-State Outputs**
- **12 bit Resolution with 32 x 12 FIFO**
- **28 Pin Plastic Small Outline Package (SOP)**

APPLICATIONS

RF Receivers
Telecommunications
Instrumentation
Modems
Fiber Optics
Bar Code Readers

GENERAL DESCRIPTION

The NT302 Period-to-Digital (P/D) Converter is a monolithic CMOS integrated circuit primarily designed for high-resolution pulse or period measurements. The device can also be used for frequency measurement as in the case of Frequency-to-Voltage (F/V) conversions. It may be used as a standalone device or in conjunction with either a Digital Signal Processor (DSP) or a conventional μP. In addition to high-speed pulse / period and frequency measurements, it is capable of demodulating any FM or ϕ modulated signal. The device uses two internal, high speed, asynchronous counters which alternately measure the period between zero-crossing intervals of the input signal. Measurement of the zero-crossing intervals is accomplished using an external clock source as a frequency reference. The period interval of the input signal appears as a digital 12 bit parallel data value at the output of the P/D converter.

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PRODUCT DESCRIPTION

The all-CMOS construction of the NT302 Period-to-Digital (P/D) converter allows high speed operation with low power consumption. The NT302 is available as a commercial temperature range device, 0°C to +70°C, and as an industrial temperature range device, -20°C to +85°C. Both versions are available in several industry standard plastic package styles including small outline package (SOP) and quad flat pack (QFP). Operation is guaranteed over the applicable temperature range and over the supply voltage of +4.5 V to +5.5 V.

CIRCUIT DESCRIPTION

A Functional block diagram of the NT302 Period-to-Digital (P/D) converter is shown in Fig.(1). The device consists of several major function blocks, including dual High-speed asynchronous counters, gating circuitry, control logic, interface circuitry, and a 32 x 12 first-in first-out (FIFO) memory with tri-state outputs.

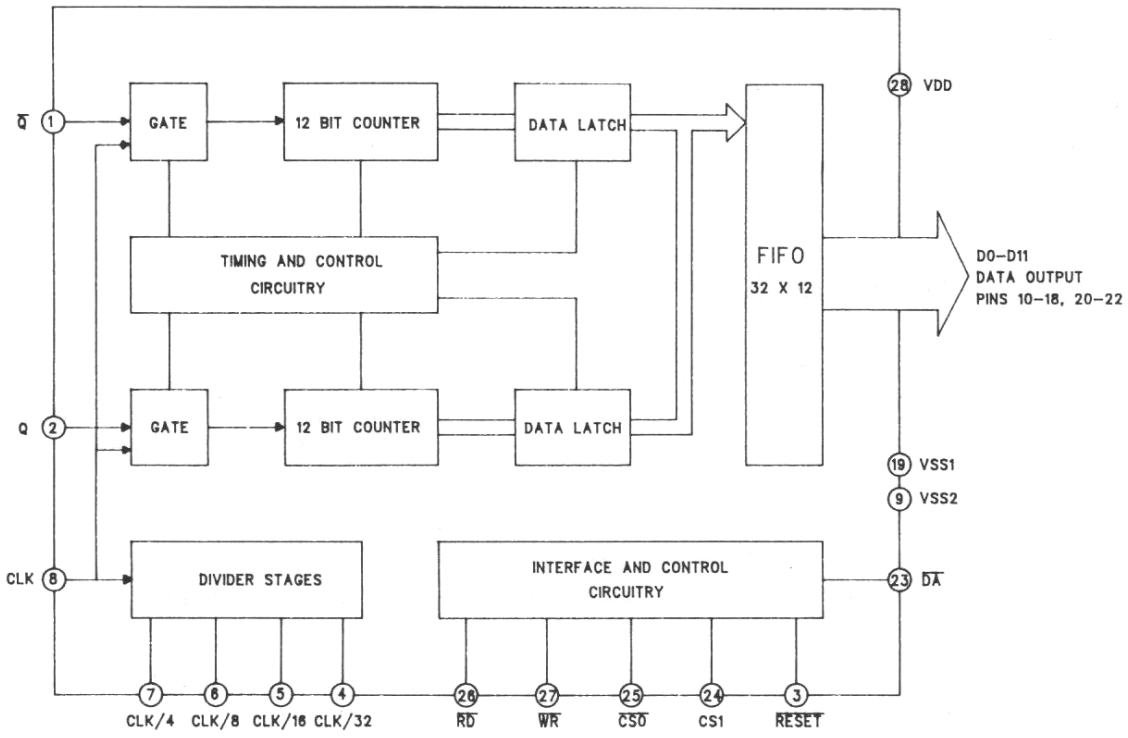


Figure (1)

CIRCUIT DESCRIPTION - Cont.

The functional block diagram shown in Figure (1) depicts the NT302 Period-to-Digital (P/D) converter. The **Q** and $\overline{\mathbf{Q}}$ CMOS compatible inputs of the NT302 are usually connected to the outputs of a comparator configured as a zero-crossing detector. In this manner, signal zero crossing information is fed into the **Q** and $\overline{\mathbf{Q}}$ inputs of the NT302. This input signal provides timing information to the internal coincidence gates in the form of a gating signal. The internal timing and control circuitry provides additional control signals for the internal counters and subsequent data latches.

During an active HIGH signal condition at either of the **Q** or $\overline{\mathbf{Q}}$ inputs, the associated input's internal counter, will advance one count for each clock cycle of the external reference clock, connected to the **(CLK)** input pin. The maximum duty cycle for either input is set by the following formulae: **Duty Cycle** $\leq 1 - 8 * t_{PW} / T$, where $T = t_{PWH} + t_{PWL}$.

Numerical data equivalent to the period measurements of each "half-cycle" is shifted in an alternating manner into the internal 32 x 12 bit asynchronous first-in first-out memory (FIFO). This internal FIFO provides buffering of the period measurement values. The interface and processor control lines of the NT302 provide the interface to an external Digital Signal Processor or a general purpose μP. Data in the form of a 12 bit binary word is read from the NT302 using these interface and control lines. This conventional memory type interface allows the Digital Signal Processor to read information from the NT302 under processor control. Data is shifted out of the internal FIFO of the Period-to-Digital (P/D) converter in a sequential manner by issuing successive reads to the data output port of the NT302. Asynchronous operation of the NT302 is accomplished by reading the DATA Output port at a rate greater than 2X the input signal frequency to the Period-to-Digital (P/D) converter.

Synchronous operation of the NT302 is accomplished by using the DATA AVAILABLE ($\overline{\mathbf{DA}}$) CMOS compatible output as an interrupt source. This interrupt may be used by the Digital Signal Processor or general purpose μP as an indication that data is available at the output of the NT302. An active LOW on the ($\overline{\mathbf{DA}}$) output indicates the availability of data at the output of the FIFO. The data output port pins of the NT302 are tri-state CMOS compatible outputs allowing the data bus to be shared by other devices.

The internal clock divider stages provide division ratios of 4, 8, 16, and 32, respectively, of the **CLK** input. The CMOS compatible divider outputs maybe used as a clock source for other devices, such as DSPs or μPs. For proper operation, care must be taken in observing output loading in order to preserve output symmetry. Output buffering is recommended for output loads of more than one CMOS or equivalent input.

APPLICATION INFORMATION

PERIOD / PULSE MEASUREMENT USING THE NT302

High-resolution pulse measurements may be made using the NT302 Period-to-Digital (P/D) converter. Resolution of the period measurement is a function of several parameters, however, the obtainable resolution is primarily related to the frequency of the external clock connected to the (**CLK**) input pin. The maximum resolution for a given pulse width maybe obtained by calculating this input clock frequency from the following formula: **CLK(MHz) = 4095 / $t_{PW\text{-}MAX}$(μsec)** with **CLK** not to exceed the maximum clock frequency (f_{MAX}) for the NT302. The minimum measurable pulse width for a given **CLK** may be calculated using the following relationship: **1 / CLK(MHz) = $t_{PW\text{-}MIN}$(μsec)** Using these relationships, one may calculate the correct clock frequency for the (**CLK**) input to the NT302. In any event, care must be taken not to allow the counter values to exceed the maximum count value of "FFFH" or the counters will ripple back through a value of "000H".

FREQUENCY MEASUREMENT USING THE NT302

High accuracy frequency measurements may be made using the NT302 Period-to-Digital (P/D) converter. Since frequency is inversely related to the period of the input signal, the NT302's period measurement capability allows it to measure the frequency of the input signal. The following equation can be used to calculate the external clock frequency for the (**CLK**) input pin. Based on the minimum input signal frequency (F_{MIN}), the correct clock frequency can be calculated by the following: **CLK = F_{MIN} * 4095**. Using this relationship the maximum resolution may be obtained for an input frequency ≥ F_{MIN}. The NT302 Period-to-Digital (P/D) converter, when used in conjunction with a DSP μP, can perform ultra-linear, wide bandwidth Frequency-to-Voltage (F/V) conversions. Unique transfer functions can be realized using a DSP μP for signal processing. If linearization of the data is required, it may be calculated or stored in the DSP μP, to provide or correct for a specific non-linear transfer function.

USING THE NT302 AS A DEMODULATOR

Frequency Modulated (FM) and or phase (ϕ) modulated signals may be recovered by the NT302, since demodulation is essentially an extension of frequency measurement. Several requirements of a frequency-to-voltage (F/V) converter when used as a demodulator include wide dynamic range, adequate frequency response, and a linear transfer function. The basic theory of operation relies on the relationship of the instantaneous frequency of the FM signal being proportional to the voltage of the modulating signal. Furthermore, the instantaneous frequency of the FM signal is inversely related to the period of the FM signal. It is in this manner, that the NT302 utilizing zero-crossing period measurement is able to demodulate.

APPLICATION INFORMATION - Cont.

INPUT CONNECTIONS

In most applications, amplification and level shifting will be required to obtain proper digital CMOS compatible signals for the NT302 Period-to-Digital (P/D) **Q** and $\overline{\mathbf{Q}}$ inputs. An external low cost comparator with complimentary CMOS compatible outputs can provide the required signal conditioning, providing zero-crossing information to the P/D converter inputs. Inputs from other sources which are CMOS compatible are acceptable as long as they meet the rise and fall time specifications of these inputs.

In most pulse measurement applications, a high-speed comparator (TL714C) or a Schmitt Trigger (74ACT14) can be used for input signal conditioning. The output signal from the signal conditioner is fed to the **Q** input of the NT302. The $\overline{\mathbf{Q}}$ input of the NT302 must be tied to ground.

A typical input circuit designed for single +5 V supply operation is shown in Fig. (2). The input signal is AC coupled via capacitor C1 to the inverting input of amplifier U2, which is configured as an inverting gain stage prior to comparator U3. A mid-point bias voltage developed by U1 is used by both the op amp and zero-crossing comparator as a low-noise reference voltage. The output of amplifier U2 is connected to the non-inverting input of comparator U3 which is configured as a zero-crossing detector. Output feedback is supplied via resistor R5 to the inverting input of comparator U3 to provide hysteresis.

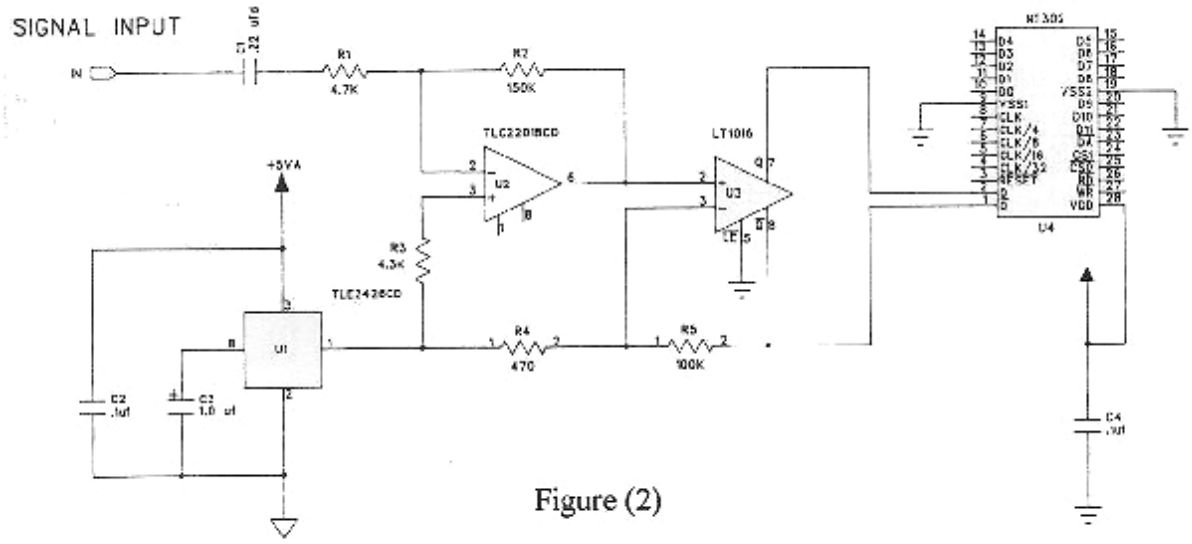


Figure (2)

INTERFACING THE NT302 TO DIGITAL SIGNAL PROCESSORS

The I/O structure of the NT302 allows direct interfacing to most DSP and general purpose microprocessor buses. Figure (3) illustrates a "no-glue" interface to the Analog Devices ADSP-21XX series of DSP microprocessors.

Consult the factory for additional information on interfacing to other DSP μPs.

NT302 TO ANALOG DEVICES ADSP-21XX

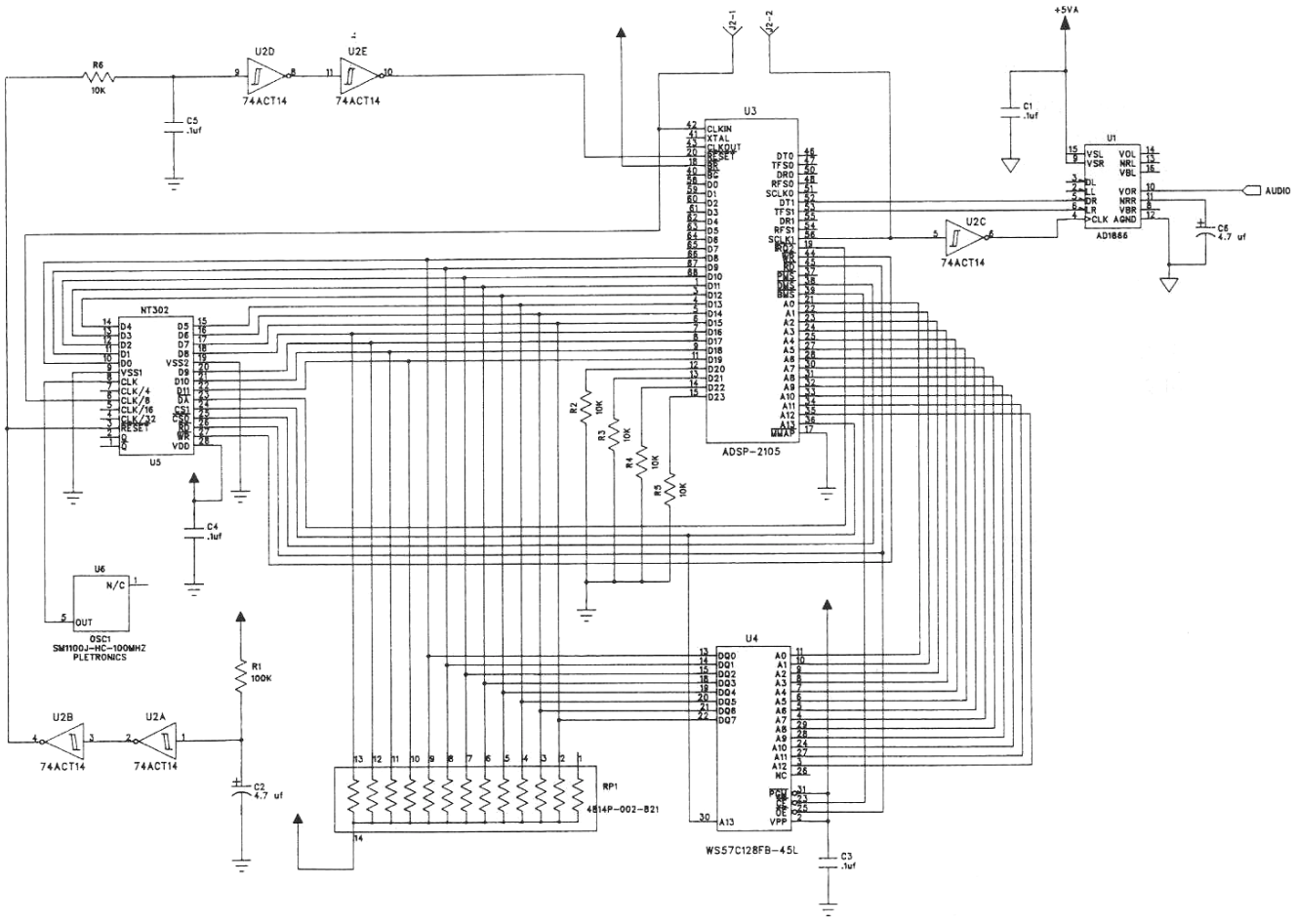


Figure (3)

PIN DESCRIPTIONS

This section summarizes the pin descriptions of the NT302 Period-to-Digital (P/D) converter by interface.

Pin Name	Type	Function
Inputs:		
Q	Input	**Q** INPUT: The CMOS compatible input, normally connected to the non-inverting output of the zero-crossing comparator. Input signal zero-crossing data is input to the Period-to-Digital (P/D) converter from the zero-crossing comparator via this input.
$\overline{\mathbf{Q}}$	Input	$\overline{\mathbf{Q}}$ INPUT: The CMOS compatible input, normally connected to the inverting output of the zero-crossing comparator. Input signal zero-crossing data is input to the Period-to-Digital (P/D) converter from the zero-crossing comparator via this input.
Clocks:		
CLK	Input	CLOCK: This CMOS compatible input is used as the reference source for the internal period measurement counters. The actual frequency used is determined by the **CLK** formulas in the applications section. The duty cycle of this input should be 50% nominally and at a frequency not to exceed the Maximum Clock Input.
CLK/4	Output	CLOCK ÷ 4: This output provides a ÷ 4 output of the **CLK** input. This output may be used as a clock source for peripheral devices such as a DSP or µP.
CLK/8	Output	CLOCK ÷ 8: This output provides a ÷ 8 output of the **CLK** input. This output may be used as a clock source for peripheral devices such as a DSP or µP.
CLK/16	Output	CLOCK ÷ 16: This output provides a ÷16 output of the **CLK** input. This output may be used as a clock source for peripheral devices such as a DSP or µP.
CLK/32	Output	CLOCK ÷ 32: This output provides a ÷ 32 output of the **CLK** input. This output may be used as a clock source for peripheral devices such as a DSP or µP.

Interrupt Request:

$\overline{\text{DA}}$	Output	DATA AVAILABLE: When LOW, this output indicates valid data is available at the output of the Period-to-Digital (P/D) converter. This output may be used as an interrupt source for a Digital Signal Processor. When used as an interrupt source, the data read from the Period-to-Digital (P/D) converter will be synchronous to the NT302's input. Upon the rising edge of **$\overline{\text{RD}}$**, the **$\overline{\text{DA}}$** output will go LOW if the FIFO is not empty, indicating data is still available. If required, handshaking with the Period-to-Digital (P/D) converter may be accomplished using the **$\overline{\text{DA}}$** signal. This may be accomplished in the following manner: The falling edge of **$\overline{\text{RD}}$**, or the fact that the **$\overline{\text{RD}}$** signal is LOW, will cause the **$\overline{\text{DA}}$** signal to go HIGH. The **$\overline{\text{RD}}$** signal should not be taken HIGH again, advancing the internal pointer to the next data, until the **$\overline{\text{DA}}$** signal has gone HIGH.

Control Interface:

$\overline{\text{RESET}}$	Input	RESET: A reset must be applied upon power up of the Period-to-Digital (P/D) converter to assure proper initialization. This causes the internal FIFO and Counters to enter a clear or empty state. The **$\overline{\text{RESET}}$** signal must be held long enough during power up to assure a proper reset. A reset condition may also be accomplished using the **$\overline{\text{WR}}$** input as described below in the pin description of **$\overline{\text{WR}}$**. When used in conjunction with a reset signal for a μP, it is recommended that the termination of the reset to the NT302 precede the termination of the reset to the μP.
$\overline{\text{WR}}$	Input	WRITE: This input, **$\overline{\text{WR}}$** in conjunction with **$\overline{\text{CS}}$**0 and **CS1,** causes the same action as **$\overline{\text{RESET}}$** with the exception that it is issued under processor control. A "dummy" write from the processor with the appropriate write duration time will perform a reset operation. The internal FIFO and Counters can be cleared "on-the-fly" in this manner.

$\overline{\text{RD}}$	Input	READ: This input, **$\overline{\text{RD}}$** in conjunction with **$\overline{\text{CS}}$**0 and **CS1**, causes the outputs **D0-D11** to change from a tri-state condition to enabled. Data is shifted out of the FIFO on the falling edge of the **$\overline{\text{RD}}$** signal**.** This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear at the outputs and the **$\overline{\text{DA}}$** signal will go LOW. If data is not present, the **$\overline{\text{DA}}$** signal will stay HIGH indicating the FIFO is empty. Upon the rising edge of **$\overline{\text{RD}}$** the **$\overline{\text{DA}}$** output will go HIGH. Asynchronous operation of the Period-to-Digital (P/D) converter may be accomplished by reading the converters FIFO at a rate higher than 2X the converters input signal rate.
$\overline{\text{CS}}$0	Input	CHIP SELECT 0: When LOW, this input specifies that control and data lines to the Period-to-Digital (P/D) converter are valid and that the operation specified by the **$\overline{\text{RD}}$**, **$\overline{\text{WR}}$**, and **CS1** inputs should be performed. When HIGH, **$\overline{\text{CS}}$**0 places the **D0-D11** data lines in a tri-state condition. This input is normally tied to a Memory Strobe from the DSP for I/O mapping purposes.
CS1	Input	CHIP SELECT 1: When HIGH, this input specifies that control and data lines to the Period-to-Digital (P/D) converter are valid and that the operation specified by the **$\overline{\text{RD}}$**, **$\overline{\text{WR}}$**, and **$\overline{\text{CS}}$**0 inputs should be performed. When LOW, **CS1** places the **D0-D11** data lines in a tri-state condition. This input is normally tied to an address line from the Digital Signal Processor for I/O mapping purposes.
Data Interface:		
D0-D11	Output	DATA OUTPUTS D0-D11: These CMOS compatible digital outputs provide the data interface to the Digital Signal Processor. **D0** being the LSB (Least Significant Bit) and **D11** being the MSB (Most Significant Bit). tri-state capabilities allows the parallel data bus to be shared with other peripheral devices such as Memory, A/Ds, etc.

Power Supply Interface:

$\mathbf{V_{DD}}$	Input	Positive supply connection input for the NT302; nominally +5.0 V for CMOS operation.
$\mathbf{V_{SS1}}$ - $\mathbf{V_{SS2}}$	Input	Ground connections for the NT302. Connect all ground pins together and to a low-impedance ground plane as close to the device as possible.

BOARD LAYOUT

Designing with high-speed CMOS digital circuits requires careful attention to detail and layout. Careful attention to layout should be observed to minimize stray inductance and capacitance effects. This attention to detail will preserve the high-speed capability of the NT302. At high clock frequencies noise is a major concern, and therefore, it is not recommended that wire wrapping be used for prototyping purposes.

SUPPLY DECOUPLING

The NT302 power supplies should be well filtered, well regulated, and free from high-frequency noise. Decoupling capacitors should be located as close as possible to all power supply pins. A 2.2 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor should provide adequate decoupling. The power supply pins of the NT302 should be decoupled directly to digital ground. An effort should be made to minimize the trace length between the capacitor leads and the respective NT302 power supply and common pins.

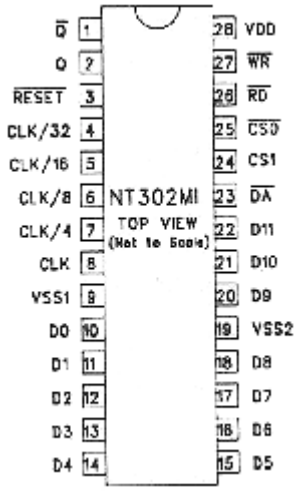
GROUNDING

While the NT302 is a digital device it can interface to an analog comparator. Therefore, a boundary must be established between the analog and digital power and ground sections. The circuit designer should attempt to locate the NT302, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground should be placed around the comparator and associated reference circuitry, while a solid digital ground should be placed around the NT302. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

If the NT302 is used with separate analog and digital ground planes, connect the $\mathbf{V_{SS1}}$ and $\mathbf{V_{SS2}}$ pins to the digital ground plane. All analog grounds, including the reference, should be tied to the analog ground plane. The digital and analog ground planes should be "summed" at one point, typically at the power supply filter capacitor. This prevents large ground loops which inductively couple noise, and allow digital currents to flow though the analog circuitry causing false data at the output of the NT302.

PIN CONFIGURATION

Plastic SOP-28 pin (450 mil)



OPERATING PRECAUTIONS

NUMA Technology's plastic molded CMOS LSI devices are designed and manufactured for trouble-free operation when used under normal operating conditions. Our products are subjected to stringent electrostatic, mechanical strength, and environmental tests for assured reliability. When working with our products the user should observe the following precautions:

(1) Use the product in the range of the rated operating voltage, operating temperature, operating input/output voltage and input/output current. If the product is used outside these operating parameters, the user may experience high failure rates.

(2) Excessive electrical noise applied to the power or input pin of the device could cause it to latch up, resulting in malfunction or damage. If this occurs, remove power, isolate the problem and turn the power on again.

(3) Do not expose the product to excessive mechanical vibration, repetitive shock, or rapid or cyclic temperature changes. These factors can cause the bond wires in the plastic package to break.

(4) Although all terminals have electrostatic protection, damage may still occur if very high electrostatic potentials are applied. Use of a conductive container or aluminum foil for packaging and transportation is recommended. (Untreated plastic containers are NOT recommended.) Use grounded soldering tools and test equipment.

TERMS and DEFINITIONS

Maximum Clock Frequency, f_{MAX}

The maximum frequency at which the logic is guaranteed to operate without errors under specified input conditions.

Hold Time, t_H:

The amount of time a signal is guaranteed to be valid (stable) after that signal has been used.

Setup time, t_{SU}:

The amount of time a signal must be stable before the signal is used.

Pulse width--Clock, t_{PW}:

The time duration of the period of the external input (**CLK**) clock frequency.

Pulse width--Reset, t_{PWR}:

The time duration of the pulse used for the $\overline{\textbf{RESET}}$ input.

Pulse width--Input High Level, t_{PWH}:

The pulse width of the input signal of either the **Q** or $\overline{\textbf{Q}}$ during an active HIGH level or logic value of "1".

Pulse width--Input Low Level, t_{PWL}:

The pulse width of the input signal of either the **Q** or $\overline{\textbf{Q}}$ during an active LOW level or logic value of "0".

High Level Input Voltage, V_{IH}:

The minimum input voltage level which defines the logic value "1".

High Level Output Voltage, V_{OH}:

The minimum output voltage level which defines the logic value "1".

Low Level Input Voltage, V_{IL}:

The minimum input voltage level which defines the logic value "0".

Low Level Output Voltage, V_{OL}:

The maximum output voltage level which defines the logic value "0".

Temperature--Ambient Operating, T_{OPR}:

The ambient operating temperature of the device.

Temperature--Storage, T_{STG}:

The maximum storage temperature range of the device.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMITS	UNITS
Power Supply Voltage	V_{DD}	V_{SS} -0.3 to 7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3 to V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS} -0.3 to V_{DD}+0.5	V
Power Dissipation	P_D		mW
Input Current	I_{DD}/I_{SS}	±40	mA
Storage Temp.	T_{STG}	-65 to 150	°C

V_{SS}-OV

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}	4.50	5.0	5.50	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Input Current (**CLK** 100 MHz)	I_{DD}		12		mA
Operating Temperature	T_{OPR}	-20		85	°C
Input Clock (**CLK**)	f_{MAX}	DC		125	MHz

V_{SS}-OV

AC CHARACTERISTICS

Test Condition

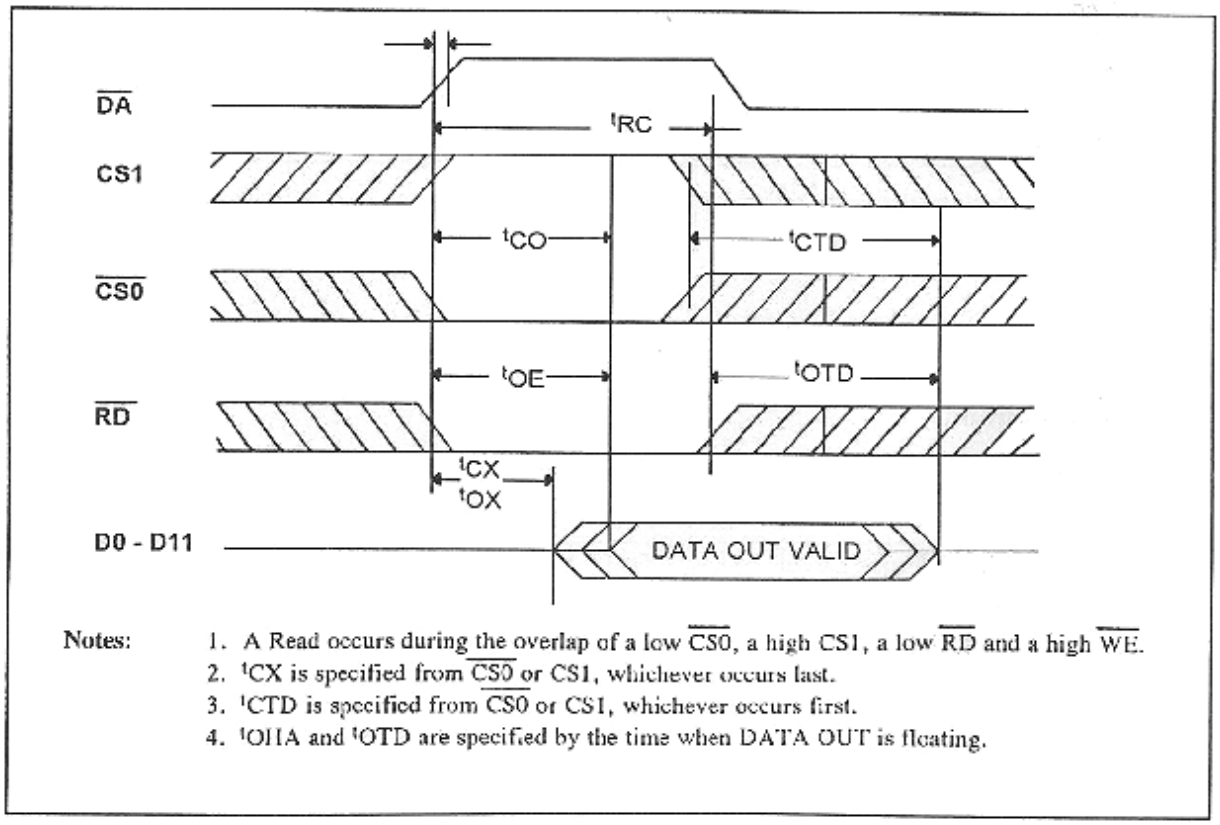
Parameter	Conditions
Input Pulse Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	CL=50 pF, 1 CMOS Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100		ns
Chip Enable Access Time	t_{CO}		100	ns
Output Enable to Output Valid	t_{OE}		50	ns
Chip Selection to Output Active	t_{CX}	10		ns
Output Enable to Output Active	t_{OX}	5		ns
Output 3-state from Output Disable	t_{OTD}	0	35	ns
Output 3-state from Chip Deselection	t_{CTD}	0	50	ns

READ CYCLE TIMING DIAGRAM



Notes:
1. A Read occurs during the overlap of a low $\overline{CS0}$, a high CS1, a low $\overline{RD}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS0}$ or CS1, whichever occurs last.
3. t_{CTD} is specified from $\overline{CS0}$ or CS1, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

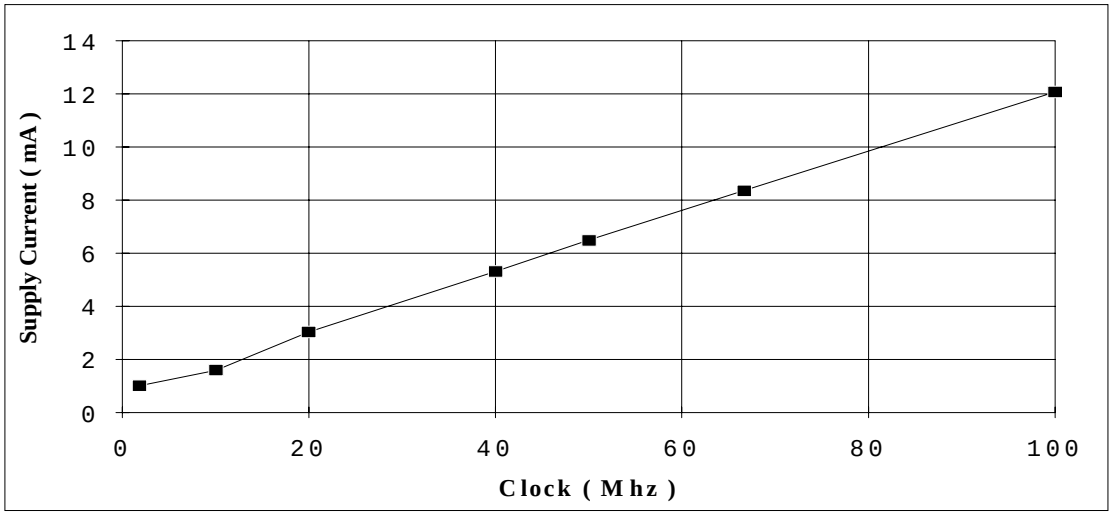
DC CHARACTERISTICS

(Unless otherwise stated, conditions are: V_{DD}=5V±10% TA=-20 to 85°C)

ITEM	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1	Static Current						
	Static Current	I_{DDS}	$V_{IN}=V_{DD}$ or V_{SS} $I_{OH}=I_{OL}$-0		7		µA
2	Input Leakage						
	Input Leakage Current	I_L	V_{DD}=MAX $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$	-1		1	µA
3	Input Characteristics						
	Input Voltage	V_{IH} 2	V_{DD}=MAX	2			V
	Input Voltage	V_{IL} 2	V_{DD}=MIN			0.08	V
4	Output Characteristics: **$\overline{DA}$,CLK/8,CLK/16,CLK/32**						
	Output Voltage	V_{OH} 2	V_{DD}=MIN I_{OH}=-3mA	V_{DD} -0.04			V
	Output Voltage	V_{OH} 2	V_{DD}-MIN I_{OL}=6mA			V_{SS} 0.04	V
5	Output Characteristics: **CLK/4, D0 - D11**						
	Output Voltage	V_{OH}3	V_{DD}=MIN I_{OH}=-6mA	V_{DD} -0.04			V
	Output Voltage	V_{OH} 3	V_{DD}=MIN I_{OL}=12mA			V_{SS} 0.04	V
6	Output Characteristics: All/Outputs						
	Off-State Leakage Current	I_{OZ}	V_{DD}=MAX $V_{OH}=V_{DD}$ or $V_{OL}=V_{SS}$	-1		1	µA

DC CHARACTERISTICS - Cont.

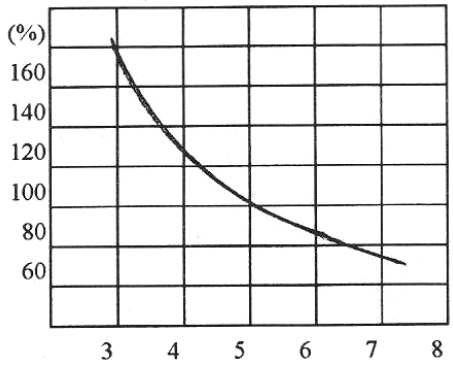
(V_{CC} = 5V, T_a = 25°C)



Typical Supply Current (I_{DD}) vs. Input Clock (CLK)

These charts indicate the effects on propagation delay with variances in supply voltage and ambient temperature respectively.

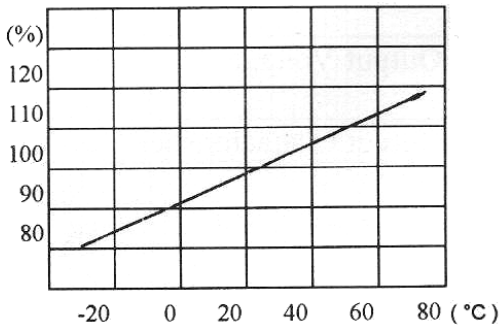
T_{pd} vs. V_{DD}



V_{DD}

Propagation Delay Degradation as a Function of Operating Voltage.

T_{pd} vs. T_{ORP}



T_{ORP}

Propagation Delay Degradation as a Function of Temperature.

ORDERING INFORMATION

Manufacturer
Device Identification

NUMA Technologies

Example

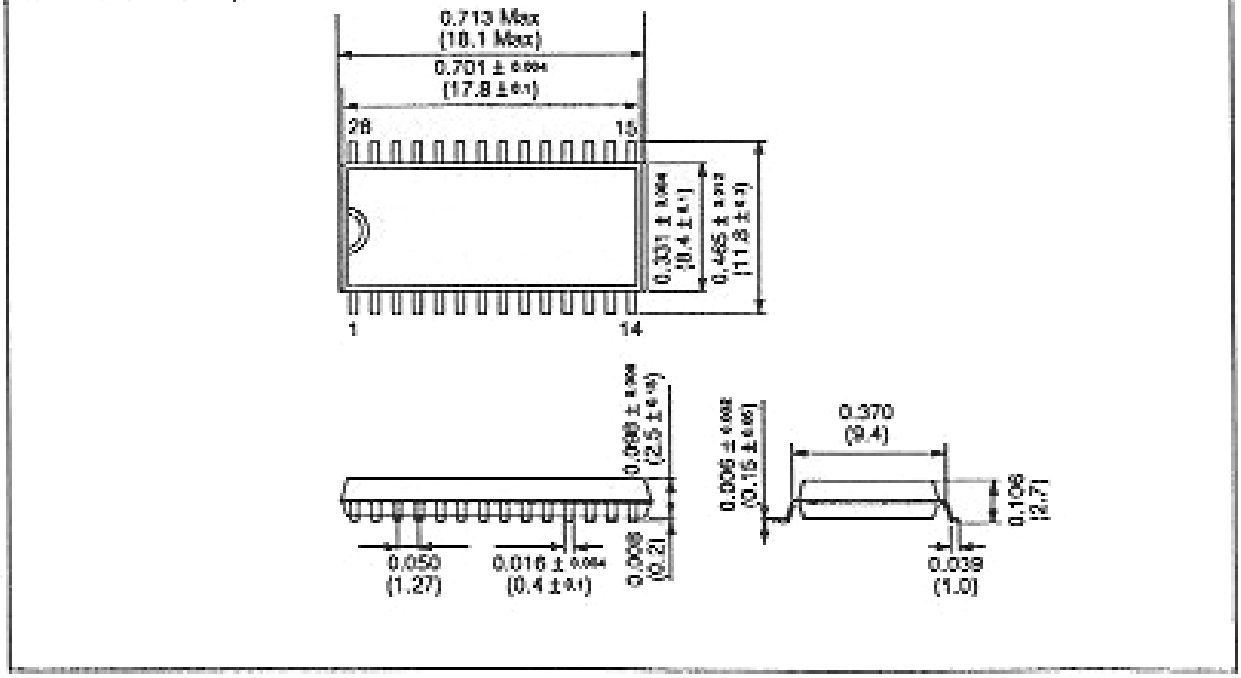
Package Type		Prefix	Device	Suffix
C	**Plastic DIP**			
D	**Die form**	**NT**	**302**	**M I**
F	**Quad Flat Package**			
H	**Ceramic DIP**			
J	**Plastic Leaded Chip Carrier**	Package		
M	**Small Outline Package**			
N	**Skinny DIP**	Temperature		
S	**Shrink DIP**			

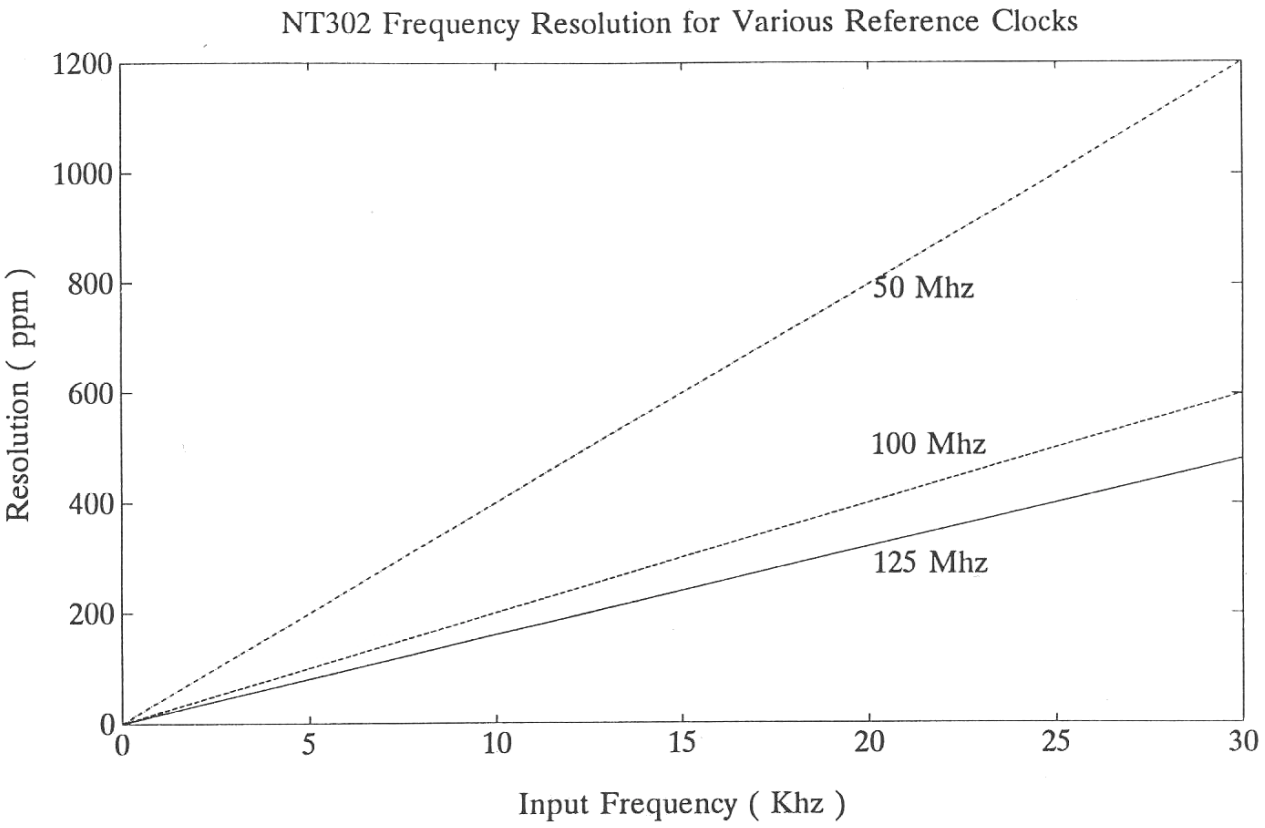
Temperature

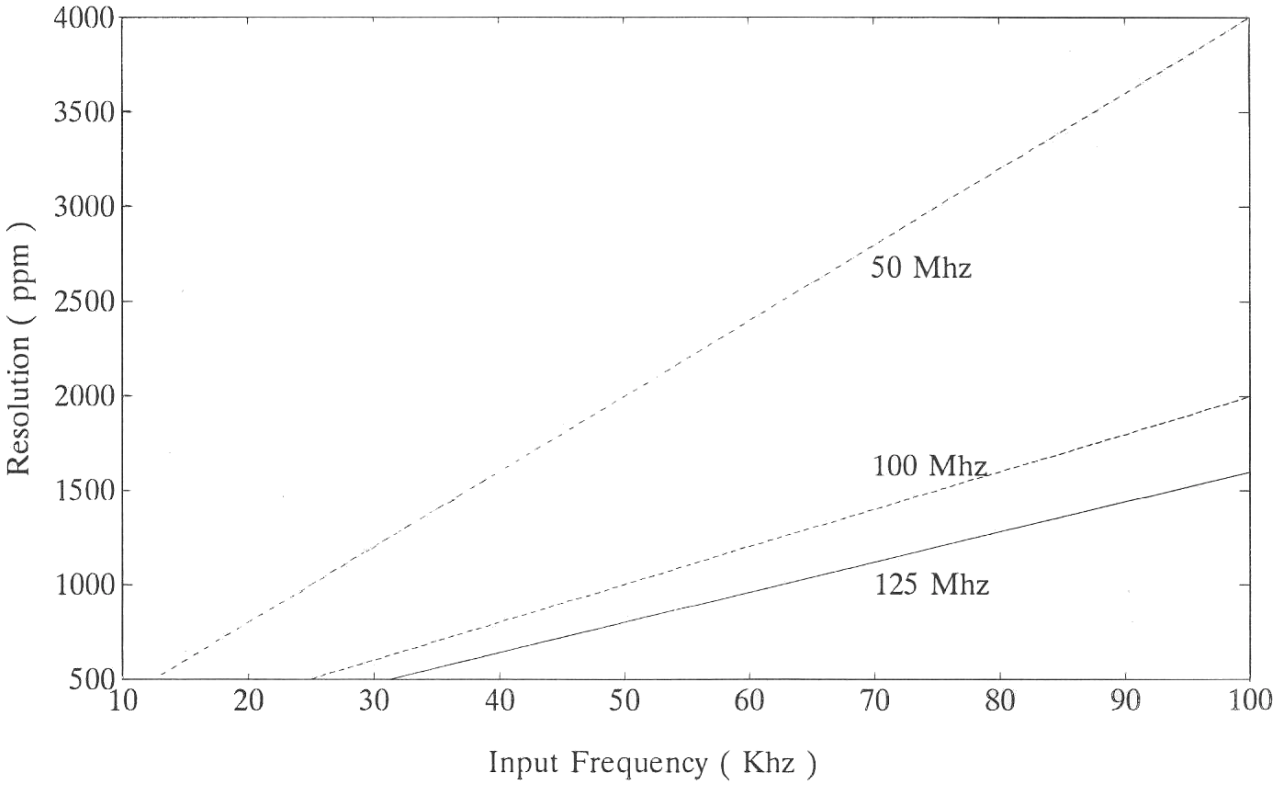
N	**Special**
C	**0°C to 70°C**
I	**-20°C to 85°C**
M	**-55°C to 125°C**
B	**-55°C to 125°C MIL Processed**
S	**Prototype Part**
K	**MIL-STM-883-5004**

Package Information

Plastic SOP2-28pin




NT302 Frequency Resolution for Various Reference Clocks
Resolution (ppm)
1200
1000
800
600
400
200
0
0
5
10
15
20
25
30
Input Frequency (Khz)
50 Mhz
100 Mhz
125 Mhz


Resolution (ppm)
4000
3500
3000
2500
2000
1500
1000
500
10
20
30
40
50
60
70
80
90
100
Input Frequency (Khz)
50 Mhz
100 Mhz
125 Mhz

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

LIFE SUPPORT DISCLAIMER

NUMA Technologies' products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of NUMA Technologies. As used herein:

1. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Products mentioned in this document are covered by U.S. patent: 5,159,281; Additional patents pending.