NTD85N02R

Power MOSFET 85 Amps, 24 Volts N-Channel DPAK

ON Semiconductor®

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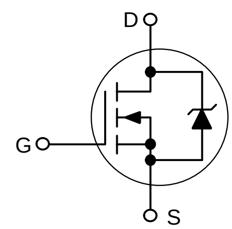
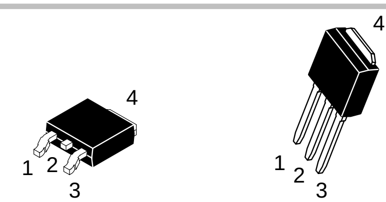
V_{DSS}	$R_{DS(ON)}$ TYP	I_D MAX
24 V	4.8 mΩ	85 A

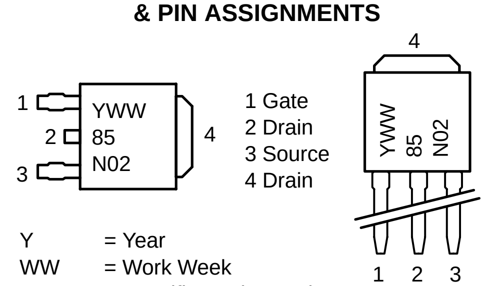
N−Channel





DPAK	Straight Lead DPAK
CASE 369AA	CASE 369D
Style 2	*Style 2*

MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
WW = Work Week
85N02R = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTD85N02R	DPAK	75 Units/Rail
NTD85N02RT4	DPAK	2500/Tape & Reel
NTD85N02R1	Straight Lead DPAK	75 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	V_{dc}
Gate−to−Source Voltage − Continuous	V_{GS}	±20	V_{dc}
Thermal Resistance − Junction−to−Case Total Power Dissipation @ T_C = 25°C Drain Current − Continuous @ T_C = 25°C, Limited by Package − Continuous @ T_A = 25°C, Limited by Wires − Single Pulse (t_p ≤ 10 μs)	$R_{\theta JC}$ P_D I_D I_D I_{DM}	1.6 78.1 85 32 96	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	$R_{\theta JA}$ P_D I_D	52 2.4 16	°C/W W A
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C	$R_{\theta JA}$ P_D I_D	100 1.25 12	°C/W W A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 30 V_{dc}, V_{GS} = 10 V_{dc}, I_L = 13 A_{pk}, L = 1 mH, R_G = 25 Ω)	E_{AS}	85	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds	T_L	260	°C

1. When surface mounted to an FR4 board using 1 inch pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) Temperature Coefficient (Positive)	(V_{GS} = 0 V_{dc}, I_D = 250 μA_{dc})	$V_{(br)DSS}$	24 −	28 20.5	− −	V_{dc} mV/°C
Zero Gate Voltage Drain Current	(V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}) (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 150°C)	I_{DSS}	− −	− −	1.5 10	μA_{dc}
Gate−Body Leakage Current	(V_{GS} = ±20 V_{dc}, V_{DS} = 0 V_{dc})	I_{GSS}	−	−	±100	nA_{dc}
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) Threshold Temperature Coefficient (Negative)	(V_{DS} = V_{GS}, I_D = 250 μA_{dc})	$V_{GS(th)}$	1.0 −	1.5 4.0	2.0 −	V_{dc} mV/°C
Static Drain−to−Source On−Resistance (Note 3)	(V_{GS} = 4.5 V_{dc}, I_D = 20 A_{dc}) (V_{GS} = 10 V_{dc}, I_D = 20 A_{dc})	$R_{DS(on)}$	− −	6.5 4.8	− 5.2	mΩ
Forward Transconductance (Note 3)	(V_{DS} = 10 V_{dc}, I_D = 15 A_{dc})	g_{FS}	−	38	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 V_{dc}, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	−	2050	−	pF
Output Capacitance		C_{oss}	−	871	−	
Transfer Capacitance		C_{rss}	−	359	−	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{GS} = 10 V_{dc}, V_{DD} = 10 V_{dc}, I_D = 30 A_{dc}, R_G = 3 Ω)	$t_{d(on)}$	−	6.3	−	ns
Rise Time		t_r	−	77	−	
Turn−Off Delay Time		$t_{d(off)}$	−	25	−	
Fall Time		t_f	−	12	−	
Gate Charge	(V_{GS} = 5 V_{dc}, I_D = 10 A_{dc}, V_{DS} = 10 V_{dc}) (Note 3)	Q_T	−	17.7	−	nC
		Q_1	−	2.6	−	
		Q_2	−	7.1	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 10 A_{dc}, V_{GS} = 0 V_{dc}) (Note 3) (I_S = 10 A_{dc}, V_{GS} = 0 V_{dc}, T_J = 125°C)	V_{SD}	− −	0.78 0.63	1.0 −	V_{dc}
Reverse Recovery Time	(I_S = 20 A_{dc}, V_{GS} = 0 V_{dc}, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	37.5	−	ns
		t_a	−	16.8	−	
		t_b	−	20.7	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.027	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

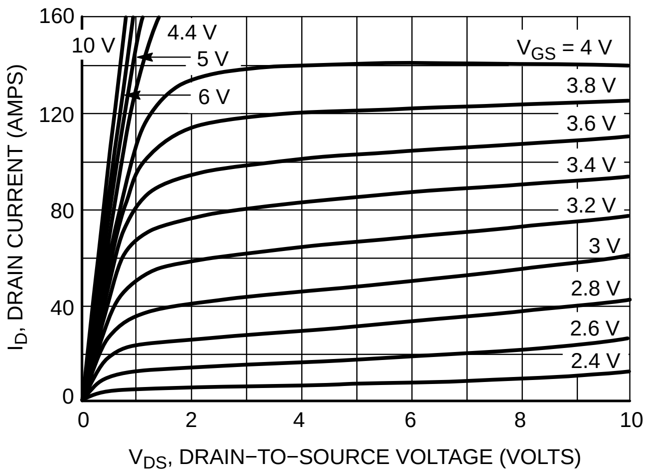


Figure 1. On−Region Characteristics

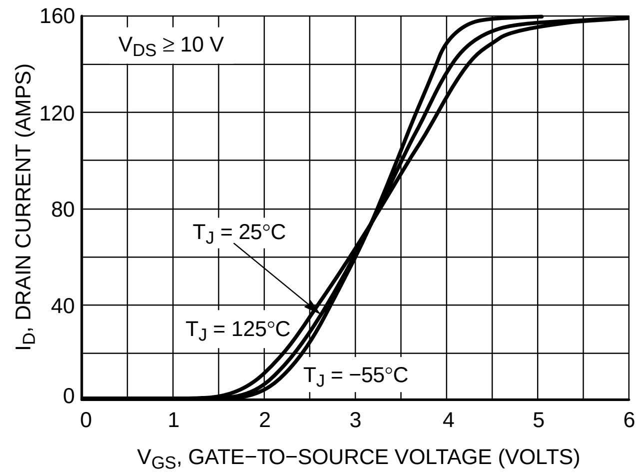


Figure 2. Transfer Characteristics

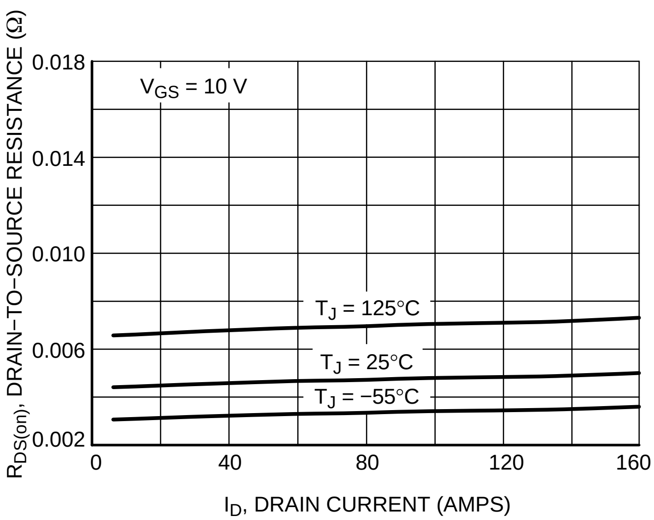


Figure 3. On−Resistance versus Drain Current and Temperature

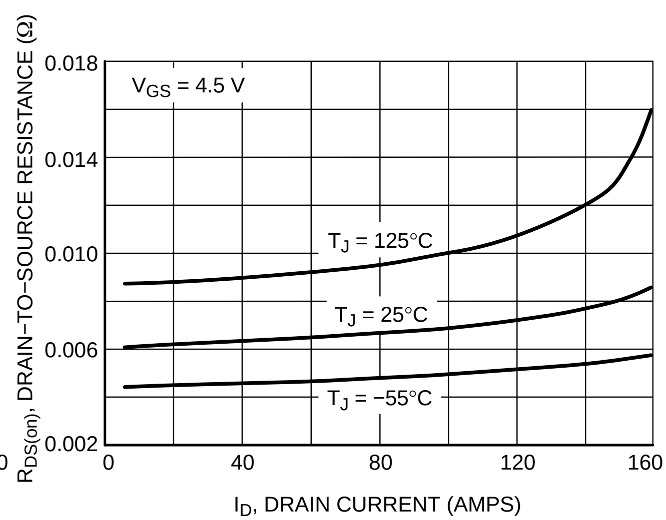


Figure 4. On−Resistance versus Drain Current and Temperature

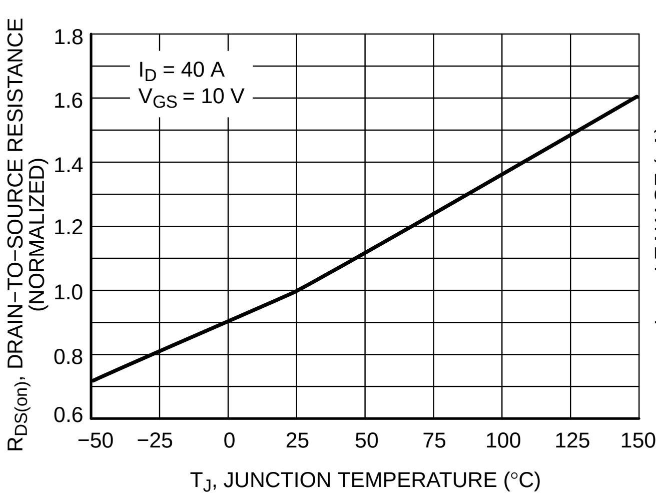


Figure 5. On−Resistance Variation with Temperature

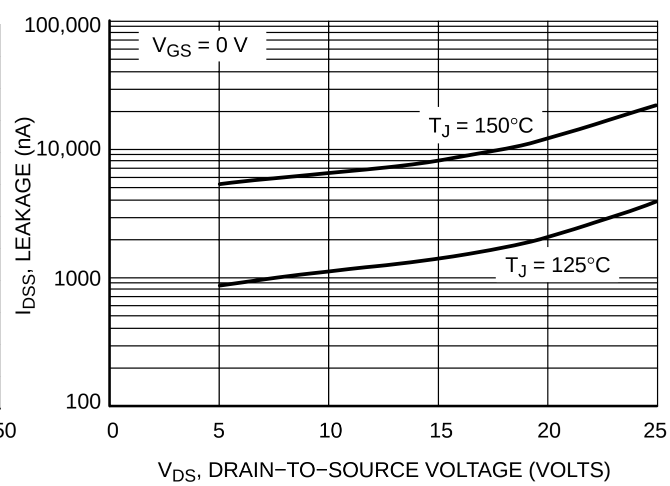


Figure 6. Drain−to−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

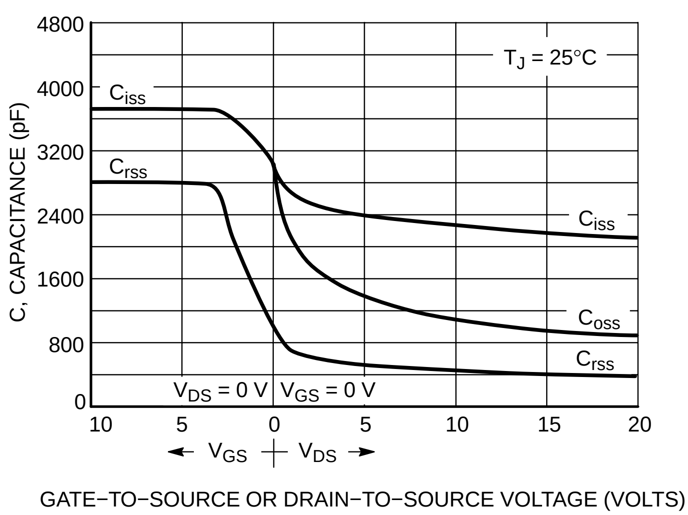


Figure 7. Capacitance Variation

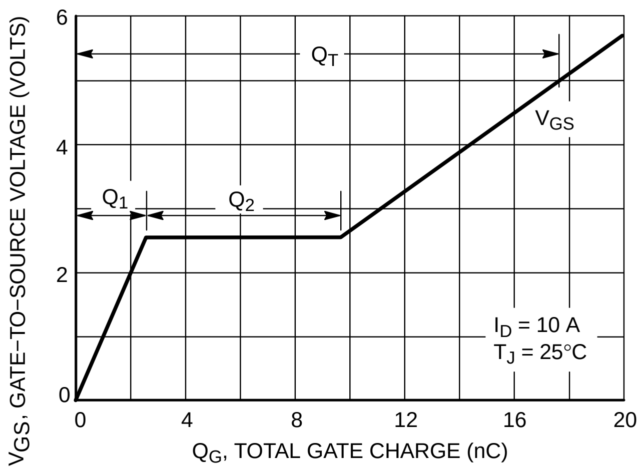


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

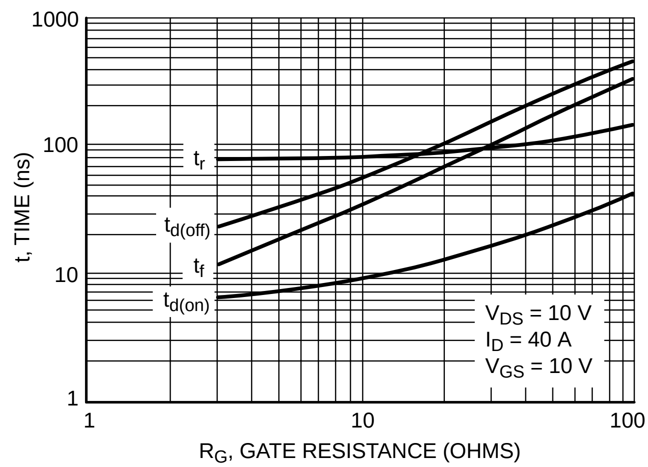


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

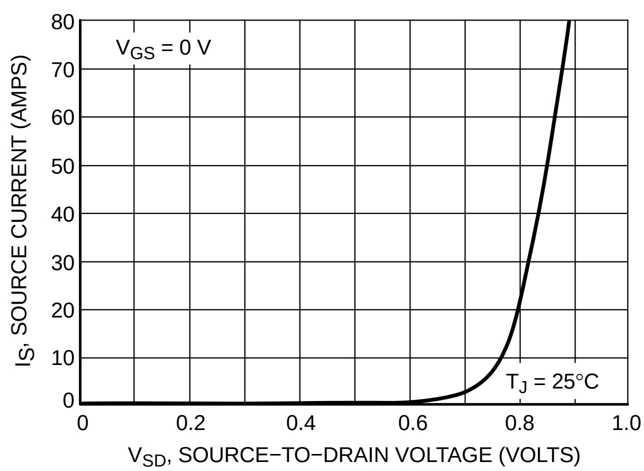


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance − General Data and Its Use."

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)}$ − T_C)/($R_{\theta JC}$).

A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

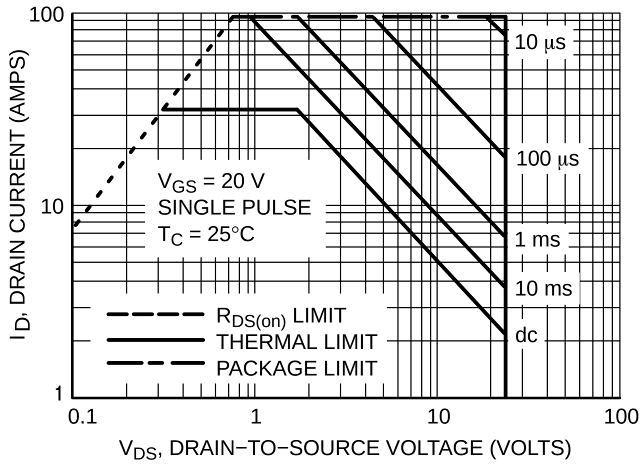


Figure 11. Maximum Rated Forward Biased Safe Operating Area

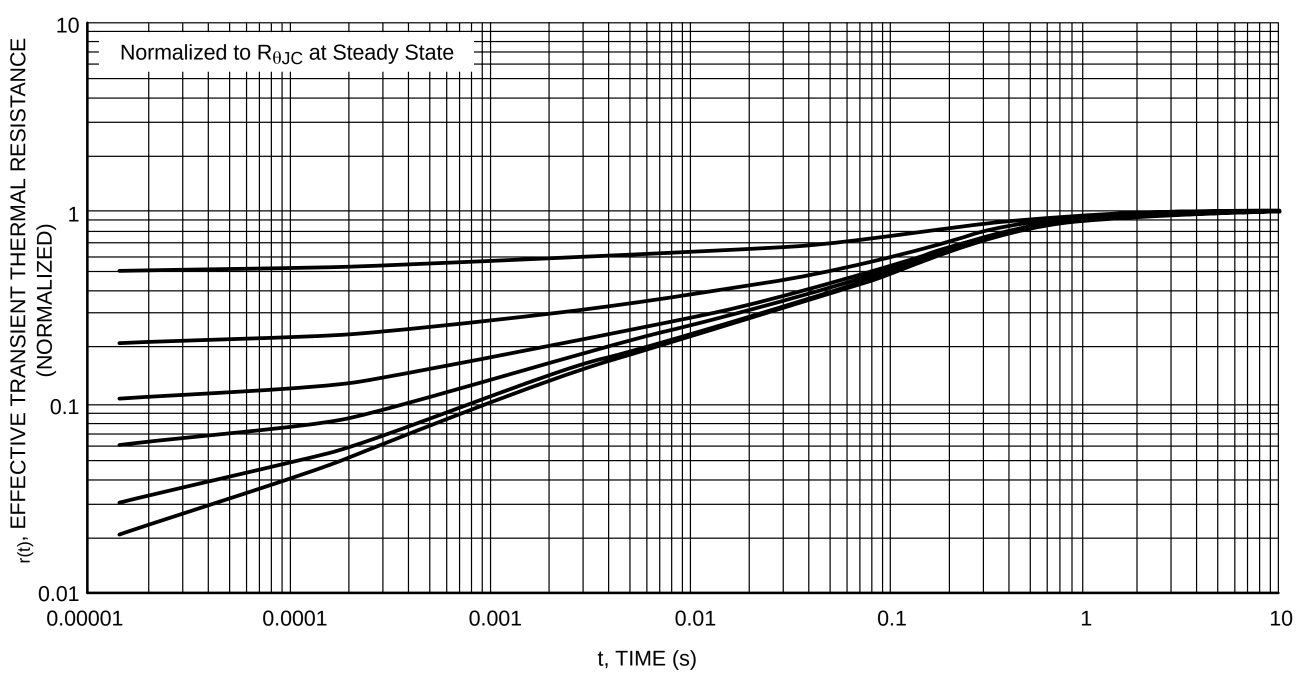


Figure 12. Thermal Response

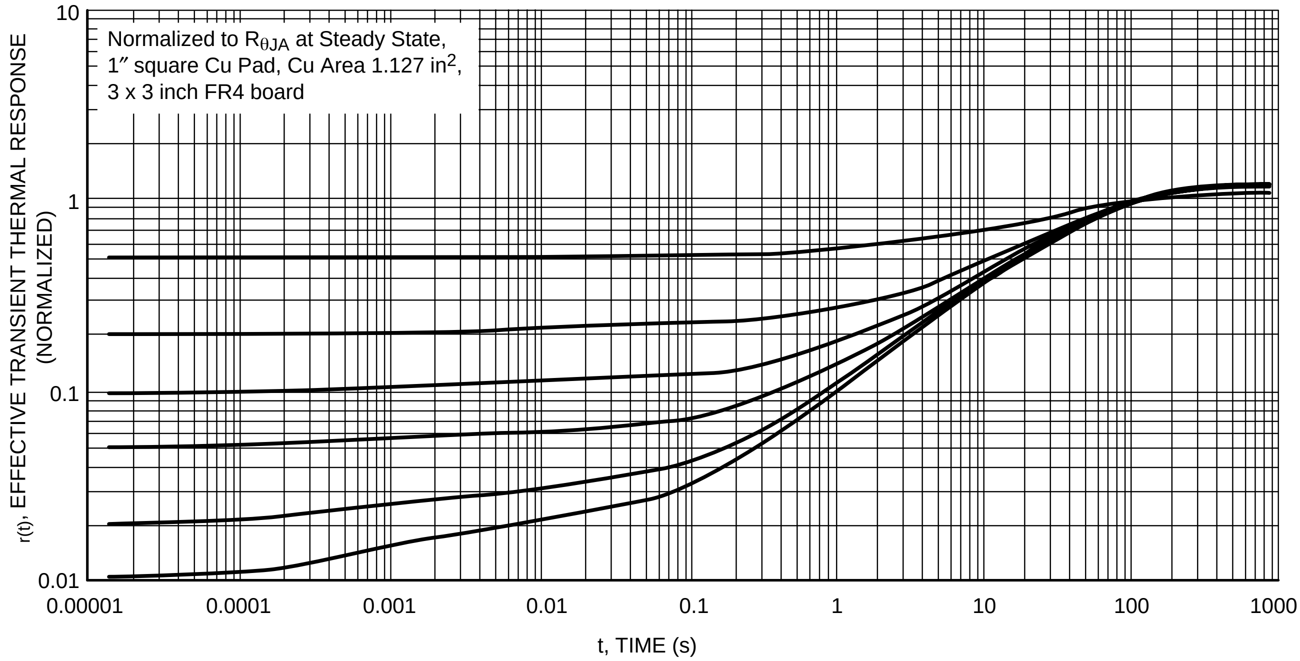
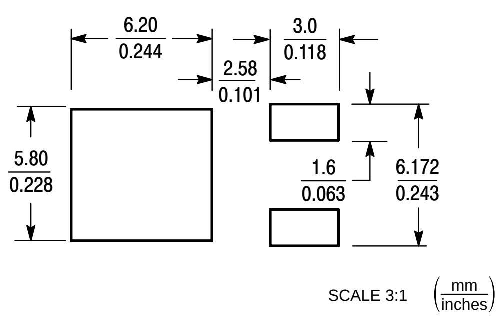


Figure 13. Thermal Response

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

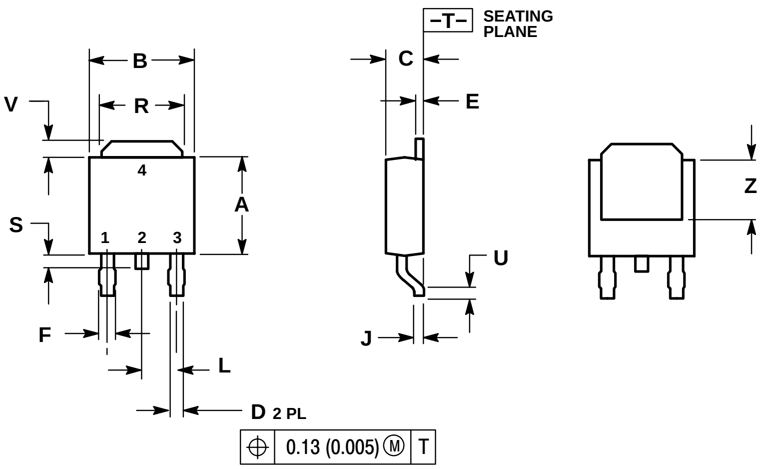
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK
CASE 369AA−01
ISSUE O

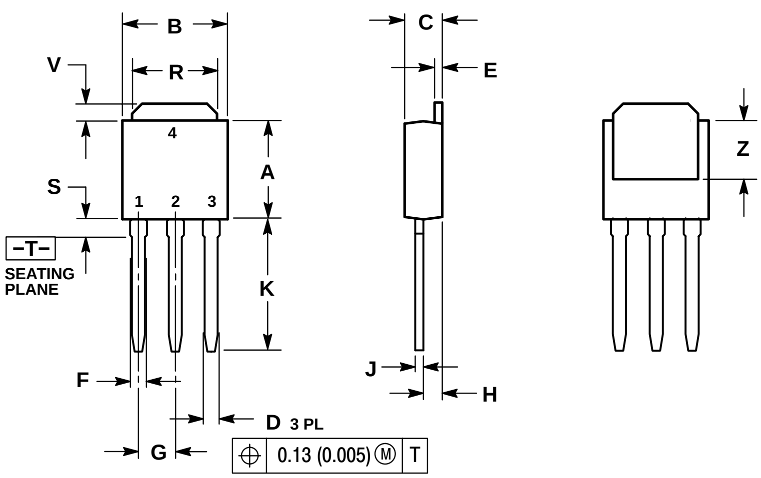


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DPAK
CASE 369D−01
ISSUE O



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C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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