PRELIMINARY

4-BIT SINGLE CHIP MICRO CONTROLLER WITH LCD DRIVER

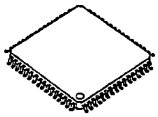
■ GENERAL DESCRIPTION

The **NJU3905** is the C-MOS 4-bit Single Chip Micro Controller consisting of ROM , RAM , I/O ports , 8-bit Serial Interfaces and LCD Driver.

It provides I/O ports for the direct control of a remote control receiver, a rotary encoder , LED driving and key scan. It also provides a serial interface for the communication with an external Micro Controller. Therefore the **NJU3905** is suitable for the front panel control of Car Audio or Home Audio.

Furthermore it provides a serial interface output to control an extension LCD Driver IC . Thus the **NJU3905** realizes to the large LCD panel driving system

■ PACKAGE OUTLINE



NJU3905F-G1

■ FEATURES

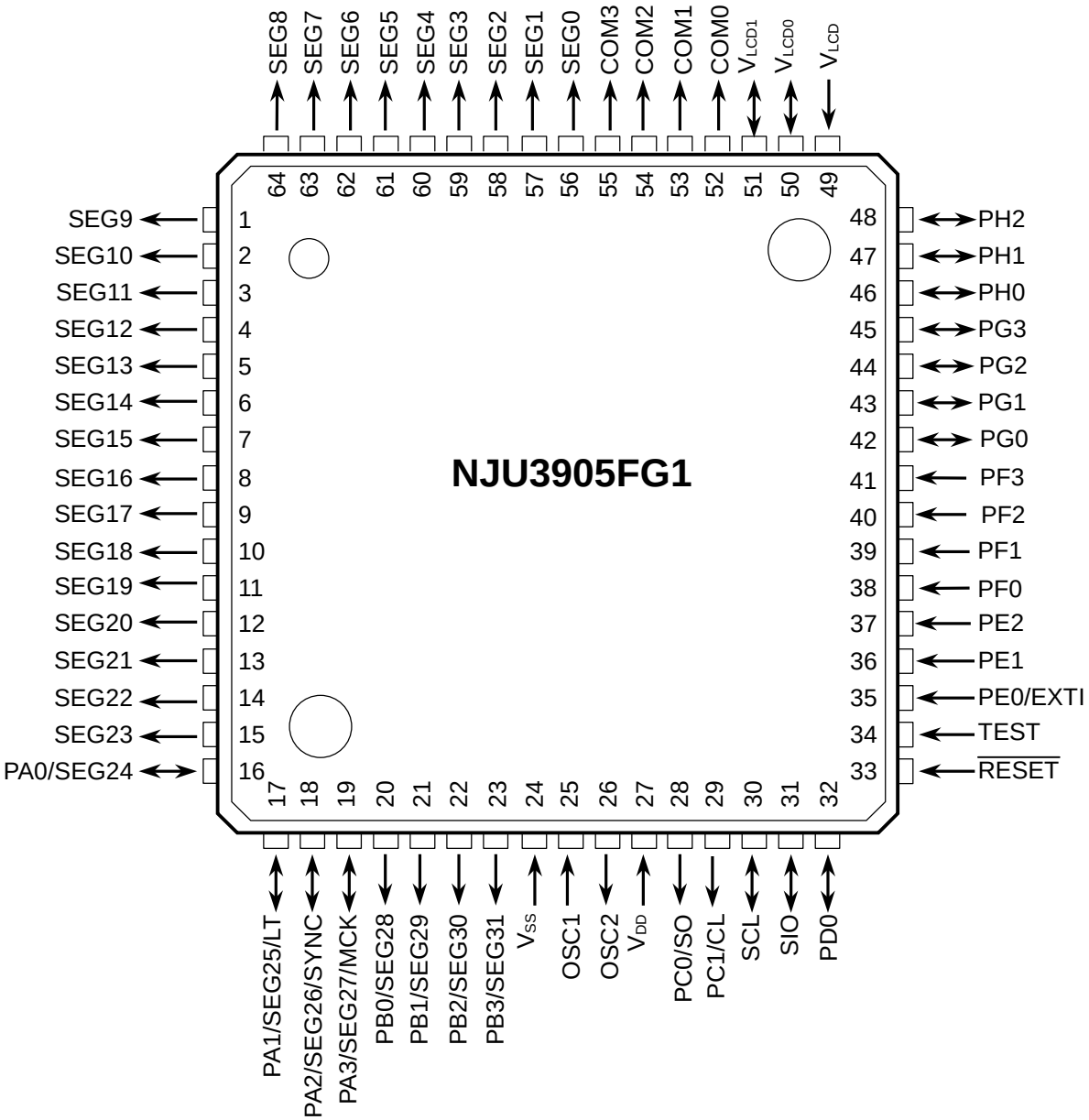
- Program ROM 8192 X 8 bits
- Data RAM 222 X 4 bits (94 X 4bits for Display)
- LCD Driver Segment Line 32 lines(MAX)
  Display Mode 1/2Duty 1/2Bias , 1/4Duty 1/3Bias
- Input / Output Port 25 lines(MAX)
  3 lines···Input / Output direction of each bit is selected by the mask option.
  5 lines···Input / Output direction of the 4-bit lines' group can be changed by the program. Additional functions by the mask option.
  External Interrupt Terminal : PE0 / EXTI
  Serial Interface Terminal : PC0 / SO, PC1 /CL
  LCD segment driving signals : PA0 / SEG24, PB0 / SEG28 to PB3 / 31
  Extension LCD Driver Interfaces or LCD segment driving signals
  : PA1 / SEG25 / LT, PA2 / SEG26 / SYNC, PA3/SEG27 / MCK
- High Output-Current terminal (4 lines)
  N-Channel FET Open Drain Type (I_{OL}) 25mA at V_{DD}=5V (PB0/SEG28 to PB3/SEG31)

Instruction Set 59 instructions

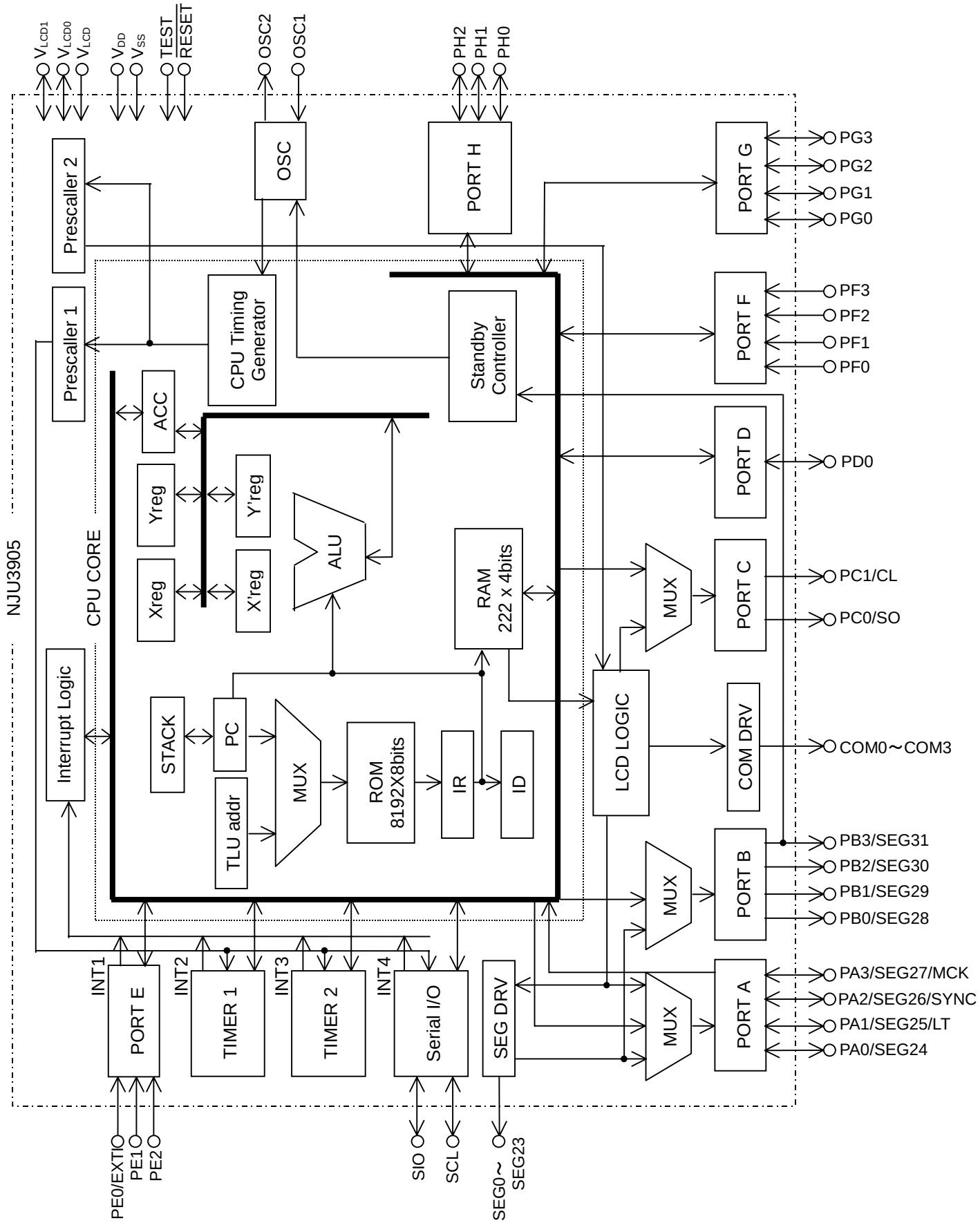
- Subroutine Nesting 8 levels
- Instruction Executing Time 6/fosc sec (1.5 μ sec at 4MHz)
- Operating Frequency Range 30kHz to 4MHz
- Internal Oscillator
  CR, or Ceramic, or X'tal oscillation and External clock input
- STANDBY function (HALT mode)
- Wide operating voltage range 2.7V to 5.5V
- 8-bit Serial Input / Output port
- Timer/Counter
  (Timer1 : 8-bit re-load type timer X 2)
- Interrupt factor 4 (external, timer1, timer2, serial Input / Output)
- LCD Extension Function
- C-MOS technology
- Package outline QFP64-G1

99/07/20

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	SYMBOL	INPUT/OUTPUT	F U N C T I O N
1 to 15 56 to 64	SEG9 to SEG23 SEG0 to SEG8	OUTPUT	LCD segment driver
52 to 55	COM0 to COM3	OUTPUT	LCD Common driver
16 17 18 19	PA0 /SEG24 PA1 /SEG25 /LT PA2 /SEG26 /SYNC PA3 /SEG27 /MCK	INPUT/OUTPUT OUTPUT INPUT/OUTPUT OUTPUT OUTPUT INPUT/OUTPUT OUTPUT OUTPUT INPUT/OUTPUT OUTPUT OUTPUT	4-bit Input / Output PORTA. Selects a function of either 1) or 2) or 3) by the mask option. 1) 4-bit Input/ Output Terminals of PORTA. Selects a terminal circuit for each port as follows by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC) •C-MOS Output Terminal (OC) 2) LCD segment driver (SEG) 3) Extension LCD Driver Interface. •Extension LCD Driver Serial Data Latch Output Terminal : LT •Extension LCD Driver Synchronizing Signal Output Terminal : SYN •Extension LCD Driver Master Clock Signal Output Terminal : MCK In case of Extension LCD Driver, Pin No.16 is assigned to input port PA0.
20 21 22 23	PB0 /SEG28 PB1 /SEG29 PB2 /SEG30 PB3 /SEG31	OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT	4-bit Output PORTB. Selects a function of either of 1) or 2) by the mask option. 1) 4-bit Input Terminals of PORTB. Selects a terminal circuit for each port as follows by the mask option. •Nch-FET Output Terminal with Pull-up Resistance (ONP) •Nch-FET Output Terminal(ON) 2) LCD segment driver (SEG)
24	V_{SS}	–	Power Source (0V)
25 26	OSC1 OSC2	INPUT OUTPUT	Internal Oscillator Terminals. Connects a device selected from the ceramic or the crystal resonator, or the resistor, to these terminals for the internal oscillator. In the external clock operation, OSC1 is the external clock input terminal and OSC2 is normally open terminal.
27	V_{DD}	–	Power Source (2.7 to 5.5V)

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
"ICP, IC,OC, SEG, LT, SYN, MCK, ONP, ON " are symbols using on MASK OPTION GENERATOR.
Refer ■ MASK OPTION

■ TERMINAL DESCRIPTION 2

No.	SYMBOL	INPUT/OUTPUT	F U N C T I O N
28 29	PC0 /SO PC1 /CL	OUTPUT OUTPUT OUTPUT OUTPUT	4-bit Output PORTC. Selects a function of either of 1) or 2) by the mask option. 1) 2-bit Output Terminals of PORTC. •C-MOS Output Terminal(ON) 2) Extension LCD Driver Interface. •Extension LCD Driver Function Serial Data Output Terminal (SO) •Extension LCD Driver Shift Clock Output Terminal (CL)
30	SCL	INOUT	Serial Interface Function. •Serial Clock Input or Output Terminal with Pull-up Resistance. (SCP) •Serial Clock Input or Output Terminal.(SC)
31	SIO	INOUT	Serial Interface Function. •Serial Data Input-Output Terminal with Pull-up Resistance. (SDP) •Serial Data Input-Output Terminal.(SD)
32	PD0	INOUT	Selects a function of either of 1) or 2) for by the mask option. 1) 1-bit Programmable Input / Output PORTD. •Input : C-MOS Input Terminal •Output: C-MOS Output Terminal Use of Pull-up resistance of the terminal is added by the mask option. (IOP / IO) 2) RESTART signal input terminal Selects a terminal circuit for each port as follows by the mask option. •Input : C-MOS Input Terminal with pull-up Resistance (RSP) •Input : C-MOS Input Terminal (RS)
33	$\overline{\text{RESET}}$	INPUT	RESET Terminal. In the “Low” level input-signal, the system is initialized.
34	TEST	INPUT	Maker Testing Terminal with Pull-down Resistance. The terminal is recommended to connect to GND.
35 36 37	PE0/EXTI PE1 PE2	INPUT INPUT INPUT	3-bit Programmable Input PORTE. Selects a terminal circuit for each port as follows by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance. (ISP) •C-MOS Schmitt Trigger Input Terminal. (IS) PE0 has a external interrupt function(EXTI). The interrupt detection edge, Rising or Falling, is fixed by the mask option.

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
“ ON, SO, CL, SCP, SC, SDP, SD, IOP, IO,RSP, RS, ISP, IS ” are symbols using on MASK OPTION GENERATOR.
Refer ■ MASK OPTION

■ TERMINAL DESCRIPTION 3

No.	SYMBOL	INPUT/OUTPUT	F U N C T I O N
38 39 40 41	PF0 PF1 PF2 PF3	INPUT INPUT INPUT INPUT	4-bit Programmable Input PORTF. Selects a terminal circuit for each port as follows by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC)
42 43 44 45	PG0 PG1 PG2 PG3	INOUT INOUT INOUT INOUT	4-bit Programmable Input / Output PORTG. This 4-bit terminal direction can be changed by the program of Input or Output. •Input : C-MOS Input Terminal •Output: C-MOS Output Terminal Use of Pull-up resistance for a terminal is added by the mask option. (IOP / IO)
46 47 48	PH0 PH1 PH2	INPUT/OUTPUT	3-bit Input / Output PORTH. Selects a terminal circuit for each port from follows by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC) •C-MOS Output Terminal (OC)
49	V_{LCD}	INPUT	Power Supply for LCD Driving.
50 51	V_{LCD0} V_{LCD1}	INOUT INOUT	Bias current Adjustment Terminal.

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
INOUT : Input or Output is changed by the program.
“ICP, IC, IOP, IO, OC ” are symbols using on MASK OPTION GENERATOR.
Refer ■ MASK OPTION

■ INTERNAL SYSTEM DESCRIPTION

The **NJU3905** is a C-MOS 4-Bit Single Chip Micro Controller consisting of Original CPU Core, Selectable Input-Output(I/O) Ports(MAX. 25 lines), Program ROM(8192 bytes), Data RAM(General-purpose area : 128 nibbles + LCD area : 94 nibbles), LCD control driver(2 or 4COM×24 SEG to 32), Extension LCD Driver interface, 8-bit Serial Interface, Dual Timer/Counter(8-bit), Interrupt Control Circuit and Oscillator Circuit.

The CPU core in the **NJU3905** is consisted of ALU(Arithmetic Logic Unit) executing the binary adding, subtracting or logical calculating, AC(Accumulator), four Registers, STACK allowing the 8-level subroutine-nesting or Interrupt operation, Program Counter indicating 8192 addresses sequentially, and Timing generator.

The **NJU3905** is applicable to the various markets because of the rich and efficient instruction set(59 instructions), wide operating voltage range(2.7V to 5.5V), low operating current, and STANDBY function reducing the power supply current.

(1) INTERNAL REGISTER

- Accumulator(AC)

  Accumulator(AC) is structured by the 4-bit register. It holds a data or a result of calculation, and executes the shift-operation (ROTATE) or the data transference between the other registers and Data Memory (RAM).

  The accumulator condition is unknown on the "RESET" operation.

- X-register(X-reg)

  X-register(X-reg) operates as the 4-bit register. Bit0 and bit1 of X-reg operates also as the RAM address pointer with Y-register.

  The X-reg condition is unknown on the "RESET" operation.

- Y-register(Y-reg)

  Y-register(Y-reg) operates as the 4-bit register or the RAM address pointer with X-reg.

  The Y-reg condition is unknown on the "RESET" operation.

- X'-register(X'-reg)

  X'-register(X'-reg) operates as the 4-bit register or a part of Program Memory(ROM) address pointer for looking data in the ROM(TRM instruction) up function.

  The X'-reg condition is unknown on the "RESET" operation.

- Y'-register(Y'-reg)

  Y'-register(Y'-reg) operates as the 4-bit register or the peripheral register number(PHYn) pointer.

  The Y'-reg condition is unknown on the "RESET" operation.

(2) INTERNAL FLAG

- RPC flag(RPC)

  RPC flag(RPC) changes the instruction table. Several instructions perform either of the dual tasks in accordance with the RPC flag condition. The RPC flag condition selects either of two couples of registers which are X- and Y- reg, or X'- and Y'-reg. X- or Y- reg is selected when the RPC flag condition is "0"(RPC=0). X'- or Y'- reg is selected when the RPC flag condition is "1"(RPC=1). The RPC flag condition is set to "1"(RPC=1) by SRPC instruction, and is set to "0"(RPC=0) by RRPC instruction.

  The RPC flag condition is set to "0" on the "RESET" operation.

- CARRY flag(CY)

  When the carry occurs after the adding calculation, the CARRY flag(CY) condition is set to "1"(CY=1), and when no carry, the CY flag condition is set to "0"(CY=0). When the borrow occurs after the subtracting calculation, the CY flag condition is set to "0"(CY=0), and when no borrow, the CY flag condition is set to "1"(CY=1). The bit-operation instruction operates the bit data rotation on the CY flag combined with the accumulator or the other register.

  The CY flag condition is set to "1"(CY=1) by SEC instruction and is set to "0"(CY=0) by CLC instruction. The CY flag condition is kept until the end of the next instruction executing cycle. The CY flag condition is unknown on the "RESET" operation.

- STATUS flag(ST)

STATUS flag(ST) is the conditional flag in accordance with the result of the instruction execution. Its condition is in accordance with follows:

1) to be same as CY flag condition.
2) to be set the condition to "0"(ST=0) when the result of the logical calculation(AND, OR, XOR, YNEA) is zero.
3) to be set the condition to "0"(ST=0) when the result of the comparison(CMP) is zero.

However, ST flag condition is always set to "1"(ST=1) except above three.

ST flag controls the branch operation. Branch instruction does not branch when ST flag condition is "0", and branches when ST flag condition is "1". ST flag condition is kept until the end of the next instruction executing cycle.

The ST flag condition is unknown on the "RESET" operation.

(3) FUNCTIONAL BLOCK

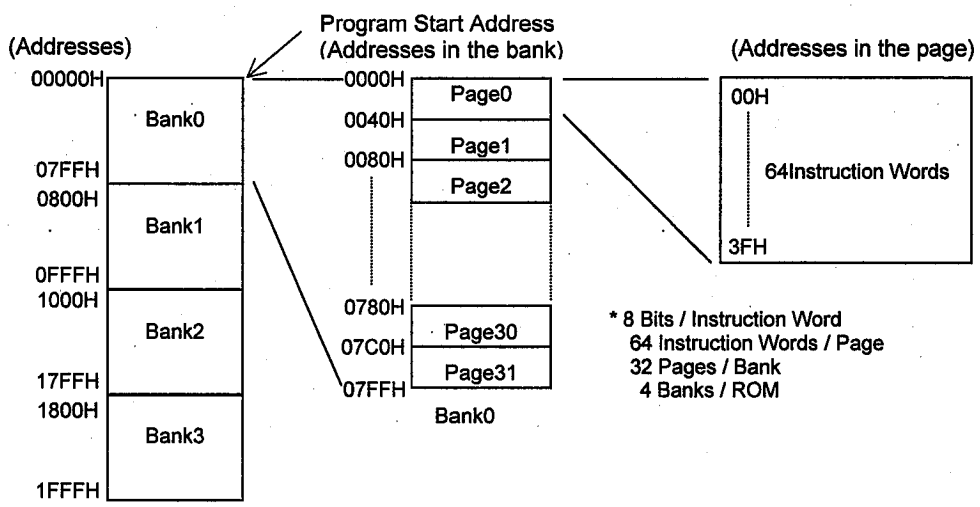
- ARITHMETIC LOGIC UNIT(ALU)

ARITHMETIC LOGIC UNIT(ALU) is a 4-bit binary paralleled calculation circuit operating binary addition, binary subtraction, comparison, logical AND, logical OR, exclusive OR, and SHIFT(Rotation). And it also can detect CARRY, BORROW or ZERO in accordance with the result of each calculation.

- PROGRAM MEMORY(ROM)

PROGRAM MEMORY(ROM) consists of 4 banks, a bank consists of 32 pages, and a page consists of 64 bytes memory capacity. Therefore the **NJU3905** prepares the 8192-byte ROM for the application program. The ROM address is indicated by the Program Counter(PC).

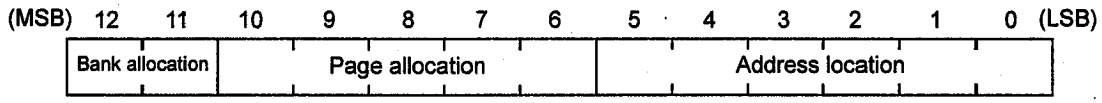
[PROGRAM MEMORY AREA]



- PROGRAM COUNTER(PC)

PROGRAM COUNTER(PC) consisted of the 13-bit binary counter stores the address for the next operating instruction in ROM. Data figures limited from b0 to b5 on the PC indicate the address in a page, and data figures limited from b6 to b10 on the PC indicate the page in a bank, and data figures limited from b11 to b12 on PC indicates a bank in ROM. Although the ROM address can be indicated 8192 addresses continuously, the target address of JMP instruction is restricted by Paging structure in ROM. The target address of JPL or CALL instruction is restricted by Banking structure in ROM.

The PC condition is set to "0" on the "RESET" operation.



JMP instruction can branch to the optional address in the page. The target address is indicated by the data figures limited from b0 to b5(6 bits) on PC as shown in above. The paging structure can reduce the program size in ROM and the JMP instruction execution time against JPL instruction because JMP instruction is consisted of one byte(8 bits) length. JPL and CALL instructions can branch to the optional address without considering the paging structure, because they consist of two bytes(16 bits) length including the 11 bits of PC. But JPL and CALL instructions can not branch between the banks in ROM.

The memory bank register(PHY15) on the peripheral register table0 selects a bank in ROM. When the branch target address is not found in the bank, the memory bank register requires to change the bank number.

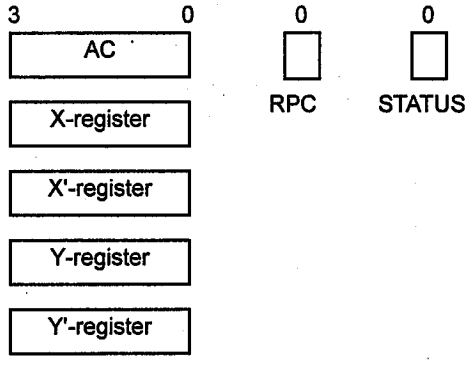
- STACK

STACK consists of three types of registers which are the 8 by 13 bits, the 5 by 4 bits, and the 2 by 1 bit registers. The registers of STACK hold the data of PC automatically when the interrupt routine or the subroutine is called. The 5 by 4 bits registers of STACK hold the data of the internal registers automatically when the interrupt operation is executed. The 2 by 1 bit registers of STACK hold the data of the internal flag automatically when the interrupt operation is executed. In the return (RET or RETI) operation, PC, the internal registers, and the internal flags registers get the held data from STACK automatically.

[For branch(CALL) and interrupt operation]

STACK POINTER	12 ... 0
000	PC
001	PC
010	PC
011	PC
100	PC
101	PC
110	PC
111	PC

[For interrupt operation]



- STACK POINTER(SP)

STACK POINTER(SP) consists of the 3 bits binary counter. SP indicates the number of next operating position in the STACK. It counts one up(increment) after the subroutine call(CALL) or the interrupt operation, and it counts one down(decrement) after the return(RET or RETI) operation.

Data storing operation to STACK after that SP overflowed (over than 7) or underflowed(under than 0), breaks the former held data in STACK. Therefore the subroutine nesting level must be cautioned in the application program.

SP condition is set to "0" on "RESET" operation.

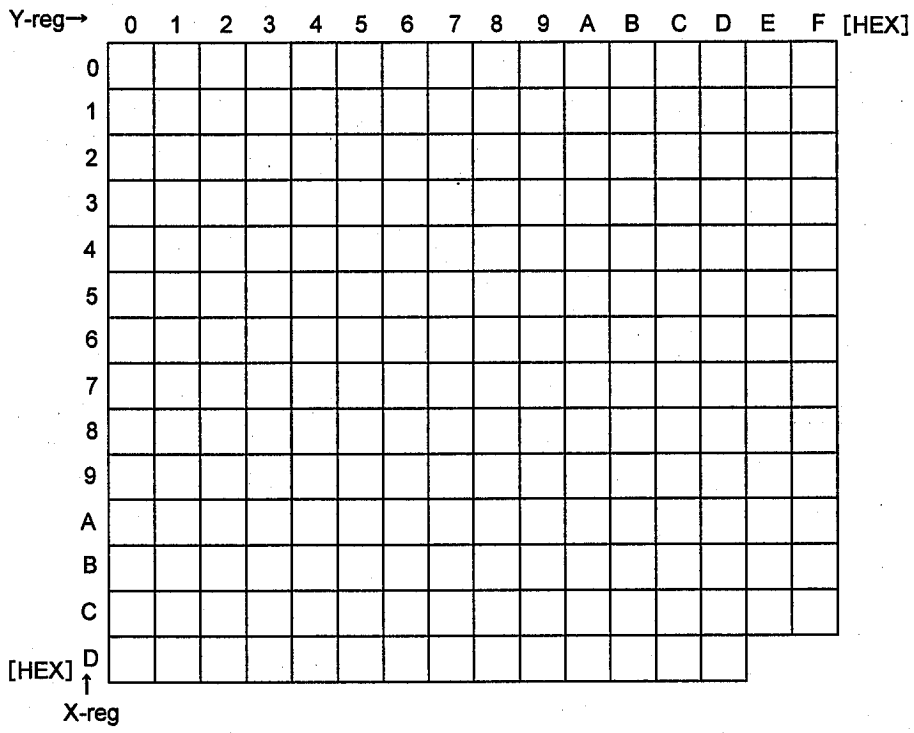
- DATA MEMORY(RAM)

DATA MEMORY(RAM) is formed with the 4-bit length a word. The **NJU3905** provides 222 words(888 bits) RAM. The data formed with the 4-bit length a word can be read/written from/to RAM, and the data formed with the 1-bit length in a word can be set, reset, or tested by the bit-operation instruction.

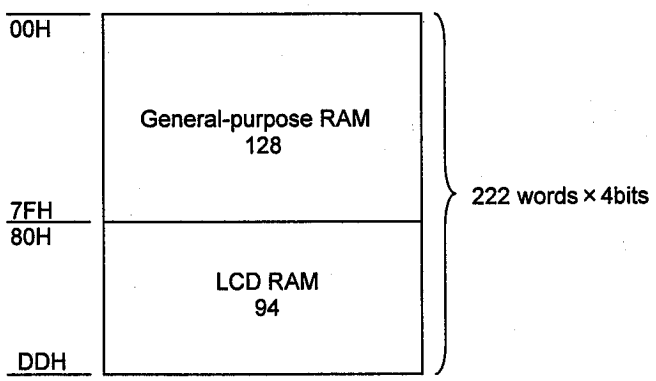
The RAM address is indicated indirectly by X-reg and Y-reg.

The RAM consists of General-purpose RAM(00H~7FH) and LCD RAM(80H~DDH). The area of LCD RAM can be also diverted to General-purpose RAM.

[RAM ADDRESS MAP]



Note) The RAM mast not use DEH to FFH



- PERIPHERAL REGISTERs(PH)

PERIPHERAL REGISTERs(PH) controlling I/O Ports or the ROM address are selected by the data in Y'-reg.

Two Peripheral Register tables called as table0 and table1 in the **NJU3905** consist of 32 registers totally.

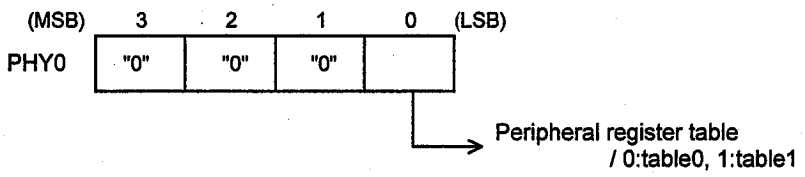
The Peripheral Register assigned for each I/O Port can get the signal data from the external application by reading operation, or can output the signal data to the external application by writing operation in accordance with the type of input or output selected by the mask option. Although the data can be read from the Peripheral Register assigned as the Output, it sometimes takes the incorrect data of the Output Port.

《Peripheral Register Table Change》

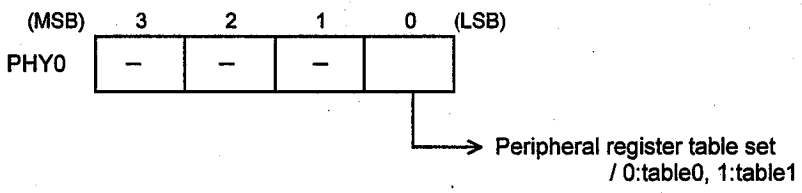
When LSB(b0) of the peripheral register table change register(PHY0) is written "0", the table0 is selected. When LSB of PHY0 is written "1", the table1 is selected.

The table0 is selected on "RESET" operation.

[Reading from the Peripheral Register Table Change Register (PHY0)]



[Writing to the Peripheral Register Table Change Register (PHY0)]



[PERIPHERAL REGISTER TABLE0]

Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read ※1	Data in Reset
0H	PHY0 (00H)	Peripheral Register Table Change Register	1	W R	0
1H	PHY1 (01H)	Serial Input/Output Control Register	3	W R	0
2H	PHY2 (02H)	Serial Input/Output Shift Register	8	W R	0
3H	PHY3 (03H)	Timer1/Pre-scaler Control Register	4	W R	0
4H	PHY4 (04H)	Initial Value Register1 / Timer Counter1	8	W R	0
5H	PHY5 (05H)	Timer2 Control Register	3	W R	0
6H	PHY6 (06H)	Initial Value Register2 / Timer Counter2	8	W R	0
7H	PHY7 (07H)	LCD Control Register	3	W R	0 ※3
8H	PHY8 (08H)	Interrupt Control Register	4	WR	0
9H	PHY9 (09H)				
AH	PHY10(0AH)				
BH	PHY11(0BH)				
CH	PHY12(0CH)				
DH	PHY13(0DH)	ROM Addressing Register "Low-bit"	4	W R	unknown
EH	PHY14(0EH)	ROM Addressing Register "Hi-bit"	1	W R	unknown
FH	PHY15(0FH)	Memory Bank Register	2	W R	0 ※2

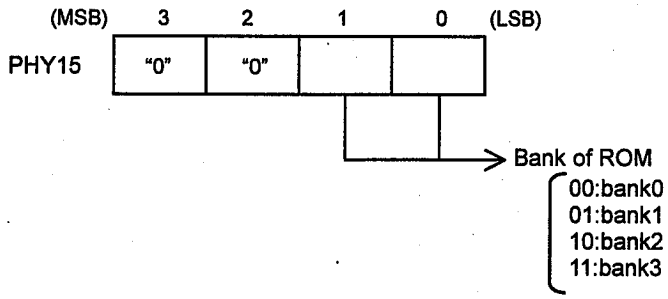
[PERIPHERAL REGISTER TABLE1]

Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read ※1	Data in Reset
0H	PHY0 (00H)	Peripheral Register Table Change Register	1	W R	0
1H	PHY17(11H)	PORTA Output or PORTA Input	4	W/R	0 ※3
2H	PHY18(12H)	PORTB Output	4	W R	0 ※4
3H	PHY19(13H)	PORTC Output	2	W R	0 ※5
4H	PHY20(14H)	PORTD Output or PORTD Input	1	W/R	0
5H	PHY21(15H)	PORTE Input	3	R	0
6H	PHY22(16H)	PORTF Input	4	R	0
7H	PHY23(17H)	PORTG Output or PORTG Input	4	W/R	0
8H	PHY24(18H)	PORTH Output or PORTH Input	3	W/R	0
9H	PHY25(19H)	Programmable Input/Output Port Control Register (PD0)	1	W R	0
AH	PHY26(1AH)	Programmable Input/Output Port Control Register (PG0~PG3)	4	W R	0
BH	PHY27(1BH)				
CH	PHY28(1CH)				
DH	PHY29(1DH)				
EH	PHY30(1EH)				
FH	PHY31(1FH)				

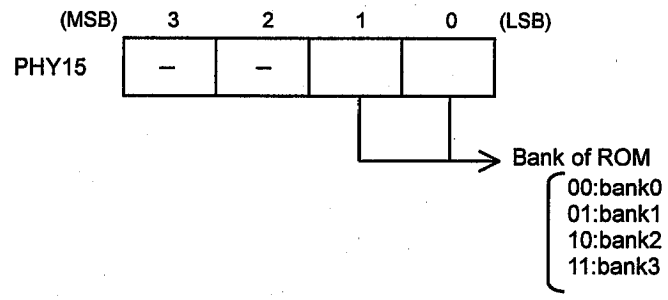
※1
- W : Write only
- R : Read only
- WR : Read and Write
- W / R : Fixed as Read or Write by the mask option

※2 Memory Bank Register(PHY15) selects the Bank0 in ROM when lower 2-bit of PHY15 is written "00", and selects the Bank1 when lower 2-bit of PHY15 is written "01", and selects the Bank2 when lower 2-bit of PHY15 is written "10",and selects the Bank3 when lower 2-bit of PHY15 is written "11".
The Bank0 is selected on "RESET" operation.

[Reading from the Memory Bank Register (PHY15)]

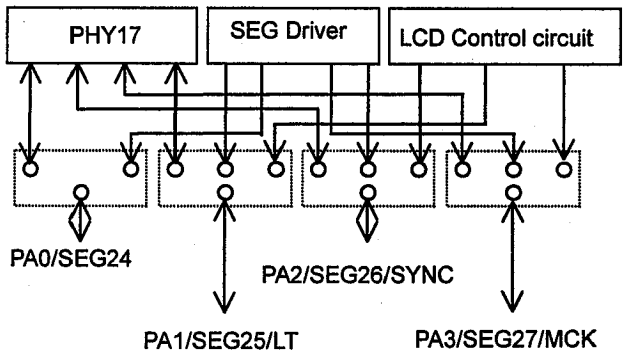


[Writing to Memory Bank Register (PHY15)]

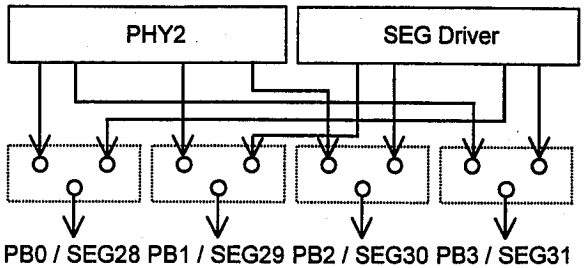


Note) Bank0 Address : 0000H to 07FFH
Bank1 Address : 0800H to 0FFFH
Bank2 Address : 1000H to 17FFH
Bank3 Address : 1800H to 1FFFH

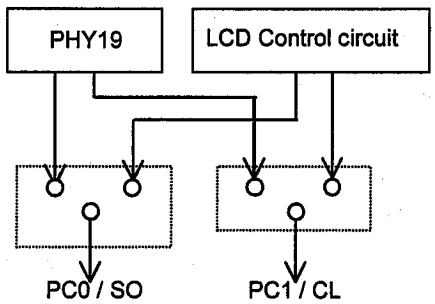
※3 Wiring of terminals
The mask option selects a terminal type from PA0/SEG24, PA1/SEG25/LT, PA2/SEG26/SYNC, PA3/SEG27/MCK as shown in right.



※4 Wiring of terminals
The mask option selects a terminal type from PB0 / SEG28, PB1 / SEG29, PB2 / SEG30, PB3 / SEG31 as shown in right.



※5 Wiring of terminals
The mask option selects a terminal type from PC0 /SO, PC1 / CL as shown in right



● ROM ADDRESSING REGISTER(PHY13, PHY14)

ROM Addressing Register (PHY13. PHY14) indicates the address of ROM with Accumulator and X'-reg for the data transference operation (TRM) from ROM to RAM.

The PHY13 and PHY14 condition are unknown on "RESET" operation. The lower a bit(b0) in PHY14 is used as the ROM ADDRESSING and higher 3 bits(b1,b2,b3) are not used.

[ROM ADDRESSING]

no used			A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0
PHY14				PHY13				X'				AC			

■ INPUT OUTPUT PORT

The **NJU3905** provides 14 Input-Output lines and 11 dual-function lines for the interface to an external application circuit. All lines are assigned to each Peripheral Register.

[PORT FUNCTION TABLE]

PORT NAME	FUNCTION	INPUT/OUTPUT
PA0～PA3	Input / Output port or SEG or LCD Extension Driver Interface	Input / Output selectable ports by the mask option.
PB0～PB3	Output or SEG	Output
PC0, PC1	Output or SO or CL	Output
PD0	Input / Output port	Programmable Input / Output PORT In case of terminal set up restart function, PD0 is assigned as input port.
PE0～PE2,	Input port	Input
PF0～PF3	Input port	Input
PG0～PG3	Input / Output port	Programmable Input / Output PORT(4-bit)
PH0～PH2	Input / Output port	Input / Output selectable ports by the mask option.

Note) Pull-up resistance is selected by the mask option.(refer ■INPUT OUTPUT TERMINAL TYPE)

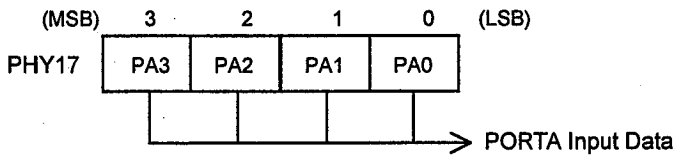
When the terminal is selected as the output by the mask option, the data reading from the assigned peripheral register can monitor the condition of the output terminal. When the terminal is selected as the N-channel FET open-drain output without pull-up resistance, the monitored condition of the output is always set to "H" level. And the condition of the unassigned bit as the output in the peripheral register is always set to "L" level.

(1) INPUT OUTPUT PORT

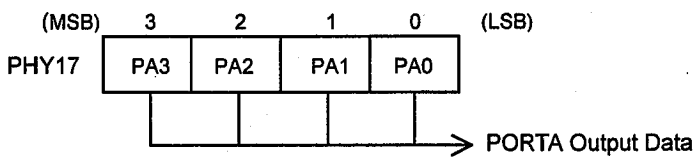
- PORTA(PA0 to PA3)

PORTA is a 4-bit input-output PORT. It operates also as the LCD segment driving signal output terminals (SEG24 to SEG27) or LCD Extension Drive terminals(LT, SYNC, MCK) by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTA register (PHY17). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY17.

[READING PORTA INPUT DATA (PHY17)]



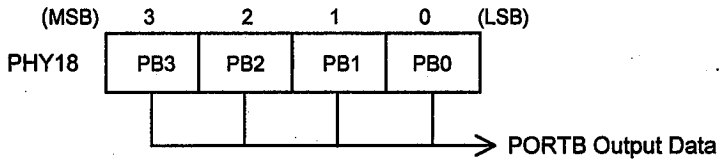
[WRITING PORTA OUTPUT DATA (PHY17)]



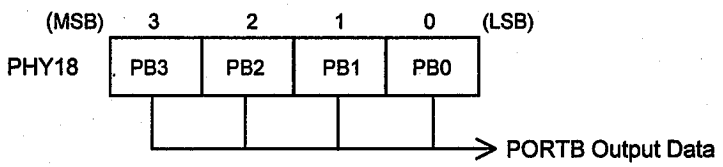
- PORTB(PB0 to PB3)

PORTB is a 4-bit output PORT. It operates also as the LCD segment driving signal output terminals (SEG28 to SEG31) by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTB register (PHY18).

[READING PORTB OUTPUT DATA (PHY18)]



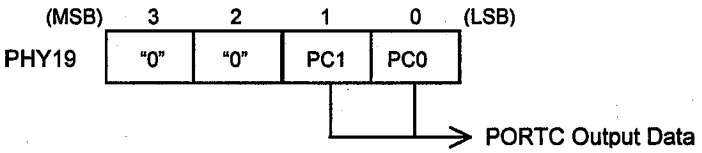
[WRITING PORTB OUTPUT DATA (PHY18)]



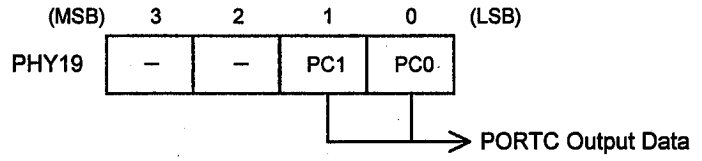
- PORTC(PC0, PC1)

PORTC is a 2-bit Output PORT. It operates also as SO and CL terminals of the 8-bit serial interface by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTC register (PHY19).

[READING PORTB OUTPUT DATA (PHY19)]



[WRITING PORTB OUTPUT DATA (PHY19)]



- PORTD (PD0)

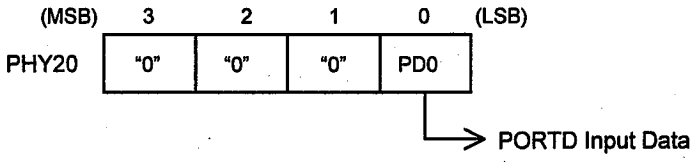
PORTD is a 1-bit programmable input-output PORT. It is set as the output when the second bit (b1) of the programmable input/output control register (PHY25) is set to "1", and it is set as the input when "b1" of PHY25 is set to "0". When the PORT is set as the output, the 1-bit signal is output through the output terminals by writing data into the peripheral register assigned for PORTD (PHY20). PHY20 as the output register should be written the output data before the PORTD is set as the output by PHY25, because the conditions of the output terminal is unknown while the output data is not written in PHY20. When this PORT is set as the input, the 1-bit external signal are gotten directly through the input terminals by reading data from PHY20. PHY20 can be written or read without regard to the input or output.

PORTD is set as the input by "0" into PHY25 on the "RESET" operation.

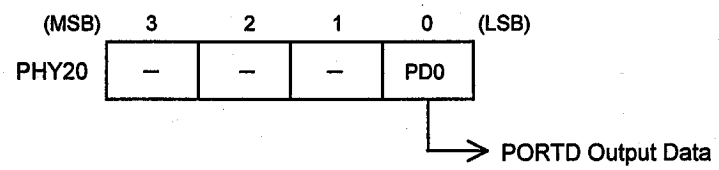
PD0 terminal performs the extra function as the re-start signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PD0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program. (refer ■STANDBY FUNCTION)

In case of the re-start signal input terminal, PH0 is set to Input terminal.

[READING PORTD INPUT DATA (PHY20)]



[WRITING PORTD OUTPUT DATA (PHY20)]

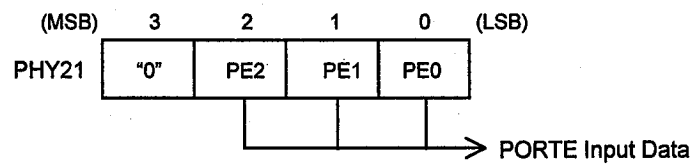


- PORTE (PE0 to PE2)

PORTE is a 3-bit input PORT. When the PORTE is set as the input PORT, the three external signals are gotten directly from the input terminals by reading data from PHY21. PE0 operates also as EXTI input terminal for the external interrupt signal input by the mask option.

Use of Rising edge type or Falling edge for a terminal is in accordance with the mask option.

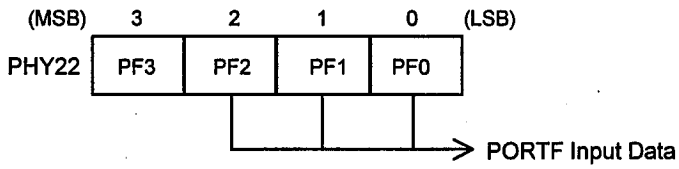
[READING PORTE INPUT DATA (PHY21)]



- PORTF (PF0 to PF3)

PORTE is a 4-bit input PORT. When the PORTF is set as the input PORT, the four external signals are gotten directly from the input terminals by reading data from PHY22.

[READING PORTF INPUT DATA (PHY22)]

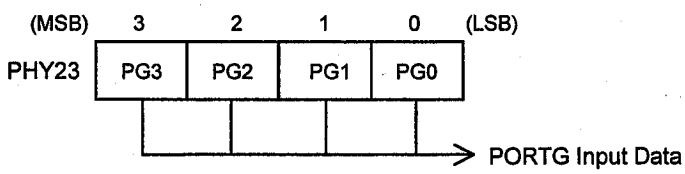


- PORTG (PG0 to PG3)

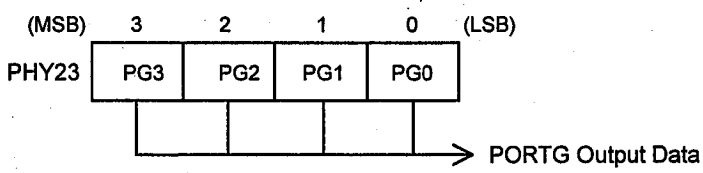
PORTG is a 4-bit programmable input-output PORT. The input or the output is selected for each bit by the programmable input/output control register (PHY26). It is set to "1" as the output, and is set to "0" as the input. When the PORT is set as the output, the 4-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTG (PHY23). PHY23 as the output register should be written the output data before the PORTG is set as the output by PHY26, because the conditions of the output terminals are unknown while the output data is not written in PHY23. When this PORT is set as the input, the 4-bit external signals are gotten directly through the input terminals by reading data from PHY23. PHY23 can be written or read without regard to the input or output. When the terminal is selected as the N-channel FET open-drain output without pull-up resistance, the monitored condition of the output is always set to "H" level.

PORTG is set as the input by "0" into PHY26 on the "RESET" operation.

[READING PORTG INPUT DATA (PHY23)]



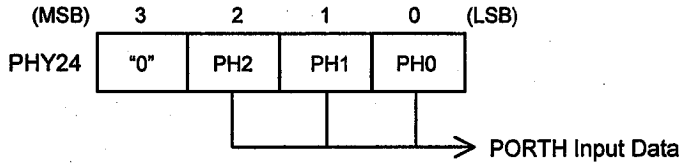
[WRITING PORTG OUTPUT DATA (PHY23)]



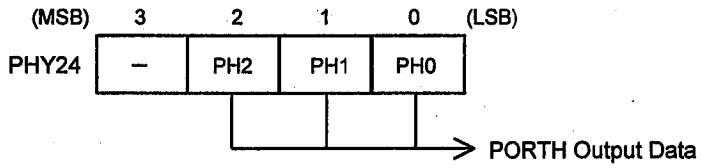
- PORTH (PH0 to PH2)

PORTH is a 3-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data into the PORTH register (PHY24). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY24.

[READING PORTH INPUT DATA (PHY24)]



[WRITING PORTH OUTPUT DATA (PHY24)]

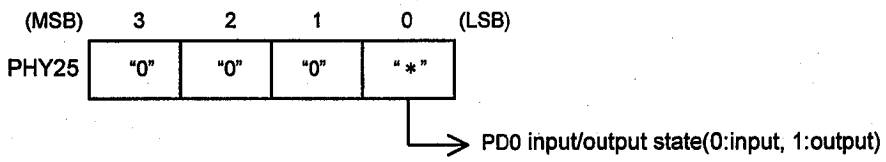


(2) PROGRAMMABLE INPUT/OUTPUT PORT CONTROL REGISTER (PHY25, PHY26)

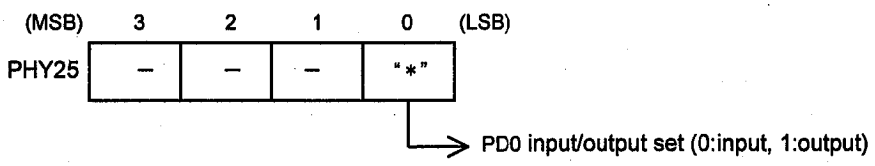
Programmable Input / Output Port Control Registers(PHY25, 26) are peripheral registers to set the direction of programmable input/output PORTs(PORTD and PORTG). PORTD is set as the output when PHY25 is set to "1". PORTD are set as the input when PHY25 is set to "0". PORTG are set as the output when b1 of PHY26 is set to "1". PORTB are set as the input when PHY26 is set to "0".

PORTD and PORTG are set as the input in accordance with the state of PHY25 and PHY26 which is set to "0" on the "RESET" operation.

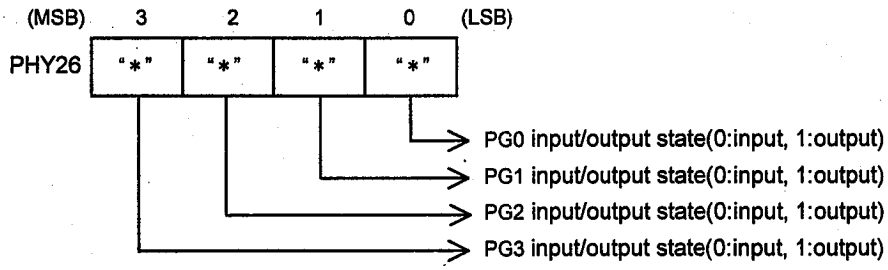
[READING from Programmable Input / Output Port Control Register (PHY25)]



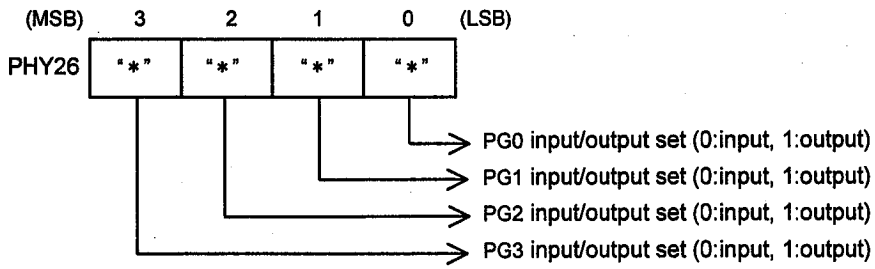
[WRITING to Programmable Input / Output Port Control Register (PHY25)]



[READING from Programmable Input / Output Port Control Register (PHY26)]



[WRITING to Programmable Input / Output Port Control Register (PHY26)]



(3) PROGRAMMABLE INPUT/OUTPUT PORT OPERATION EXAMPLE

- The output operation

PG0 and PG1 of PORTG output "H", and PG2 and PG3 of PORTG output "L".

```
        .
        .
SRPC            ;
LDI     Y, 0    ;   Peripheral table is
LDI     A, %0001;   set to the table1
TAP             ;
LDI     Y, 7    ;PHY23(PORTG Register) is pointed
LDI     A, %0011;"0011"(BIN) is stored into Accumulator
TAP             ;The data in Accumulator is transmitted to PHY23
LDI     Y, 10   ;PHY26 is pointed                          PORTG is
LDI     A, %1111;"1111"(BIN) is stored into Accumulator    set to the output
TAP             ;The data in Accumulator is transmitted to PHY26
        .
        .
```

- The input operation example

Accumulator gets the input data from PORTG.

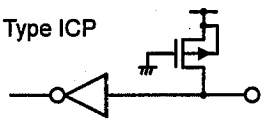
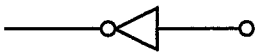
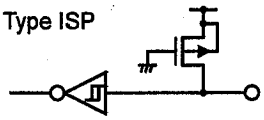
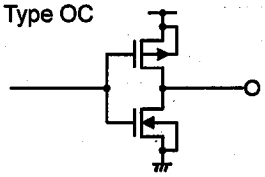
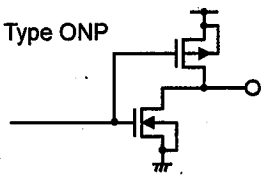
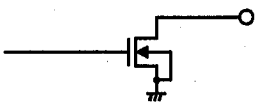
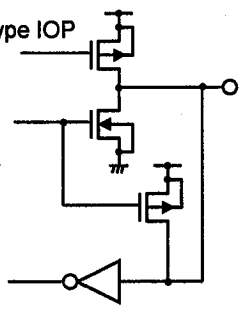
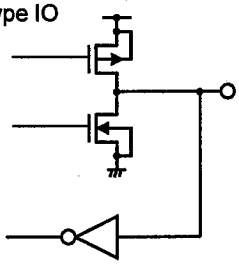
```
        .
        .
SRPC            ;
LDI     Y, 0    ;   Peripheral table is
LDI     A, %0001;   set to the table1
TAP             ;
LDI     Y, 10   ;PHY26 is pointed                          PORTG is
LDI     A, %0000;"0000" is stored into Accumulator         set to the input
TAP             ;The data in Accumulator is transferred to PHY26
LDI     Y, 7    ;PHY23(PORTG Register) is pointed
TPA             ;The input data from PHY23 is transferred to Accumulator
        .
        .
```

The signal from PG0 terminal is stored into the LSB of Accumulator, the signal from PG1 terminal is stored into the b1 of Accumulator, the signal from PG2 terminal is stored into the b2 of Accumulator, and the signal from PG3 terminal is stored into the b3 of Accumulator.

■ INPUT OUTPUT TERMINAL TYPE

Each terminal of PORT A, B, C, D, E, F, G and H can select a terminal type from the follows by the mask option which is the same mask of the program coding into ROM and the others. But PORT A selects the input or output terminal type, PORT B and C select only the output terminal, and PORT D selects only the input terminal.

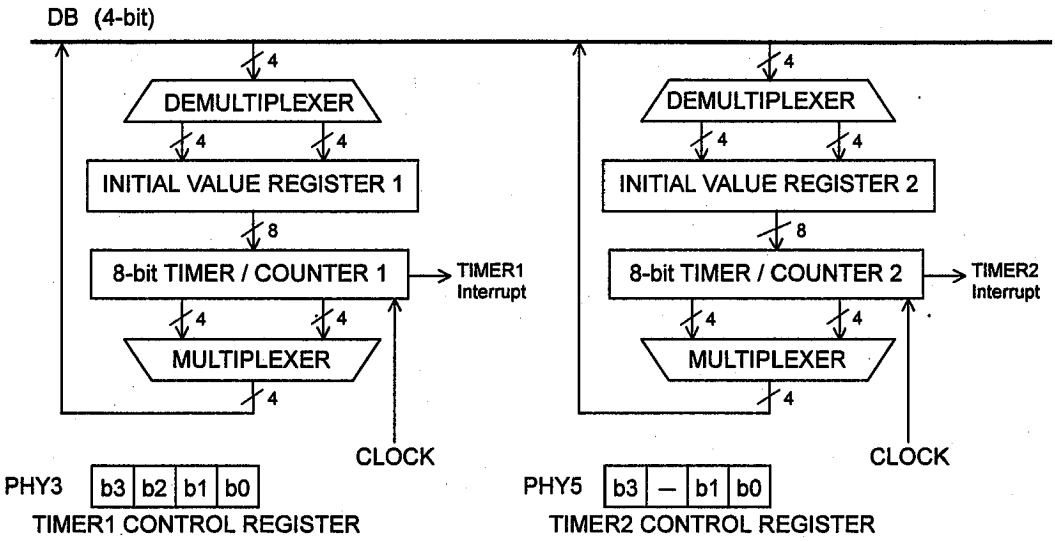
[INPUT OUTPUT TERMINAL TYPES]

	Types	With Pull-up	Without Pull-up	Terminals
Input Terminal	CMOS	Type ICP 	Type IC 	PA0~PA3, PF0~PF3, PH0~PH2
	Schmitt Trigger	Type ISP 	Type IS 	PE0/EXTI, PE1, PE2
Output Terminal	CMOS		Type OC 	PA0~PA3, PC0, PC1, PH0~PH2
	N-Channel Open Drain	Type ONP 	Type ON 	PB0~PB3
Programmable Input Output	CMOS	Type IOP 	Type IO 	PD0, PG0~PG3

■ TIMER

The **NJU3905** provides a couple of Programmable Timer / Counter(Timer1, Timer2) consisting of the 8-bit binary counter.

[Structure of Timer / Counter]



Timer1 count clock and Timer2 count clock are supplied from internal prescaler1. Timer1 control register(PHY3) can stop for clock supply to internal prescaler1. The initial value of the counter can be set the optional value by the program which instructs to write the data(a value of the time-interval or the event-count) into the Initial Value Register(Timer1 or Timer2 is set the each value independently). In enabling the timer1 interrupt, when the Timer1 counter counts from "FF" to "00" (overflow), the timer1 interrupt request occurs and the internal interrupt process starts the own operation. In enabling the timer2 interrupt, when the Timer2 counter counts from "FF" to "00" (overflow), the timer2 interrupt request occurs and the internal interrupt process starts the own operation.

In the repeat mode of the Timer operation, when the counter overflows, the initial value is loaded into the counter automatically and the counter continues the count from the loaded initial value(Auto re-load function: See the repeat mode of the Timer operation timing chart). In the single mode of the Timer operation, when the counter overflows, the count is stopped (See the single mode of the Timer operation timing chart). For starting the count operation again, the start bit (LSB) of the Timer1 or Timer2 Control Register must be set to "1". The latest initial value is set into the counter and the counter starts the count.

In enabling the interrupt operation, when the counter overflows, the Timer / Counter overflow flag is set to "1" and the internal interrupt process starts to the own operation. In disabling the timer interrupt, the Timer / Counter overflow flag is not set. The Timer / Counter overflow flag is initialized by the Timer Start or the Reset signal.

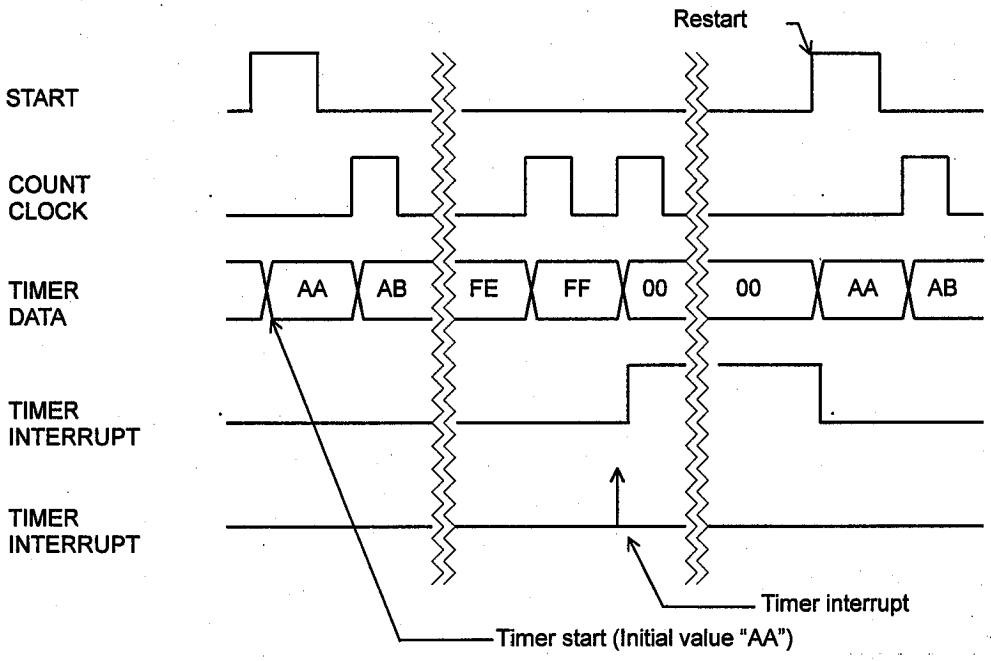
The internal clock into the counter is the divided clock from the internal prescaler. The frequency of the clock can be selected by the mask option from follows which are the dividing numbers based on the inverse of the 1-instruction executing period($1/f_{OSC}$ x 6).

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

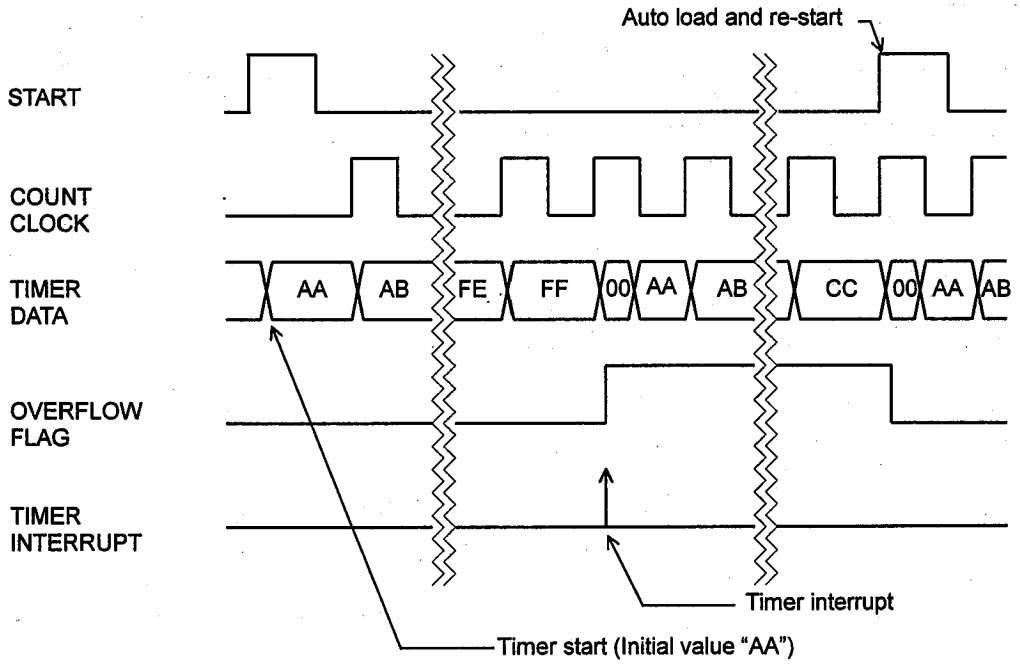
When the bit2(b2) of the Timer1 / Prescaler Control Register is set to "1", the pre-scaler generating the internal count clock is stopped the operation. As the result, Timer / Counter stops the count operation.

In the external clock operation of Timer2, the external clock must be input to CNTI terminal. The Timer2 Control Register selects either the internal clock operation or the external clock operation.

[THE SINGLE MODE OF THE TIMER OPERATION TIMING] (The initial value is set to "AAH")

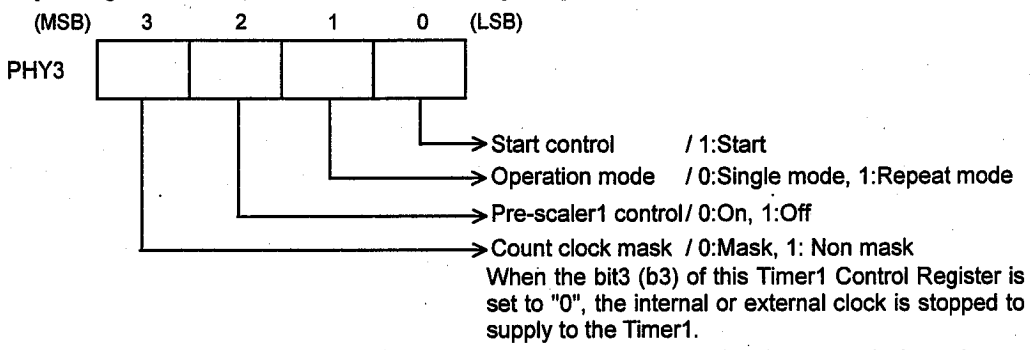


[THE REPEAT MODE OF THE TIMER OPERATION TIMING] (The initial value is set to "AAH")



- Timer1 / Pre-scaler Control Register { PHY3 ; (Y'=3, Peripheral register table 0) }

[Writing to the Timer1 / Pre-scaler Control Register]



When the bit3 (b3) of this Timer1 Control Register is set to "0", the internal or external clock is stopped to supply to the Timer1.

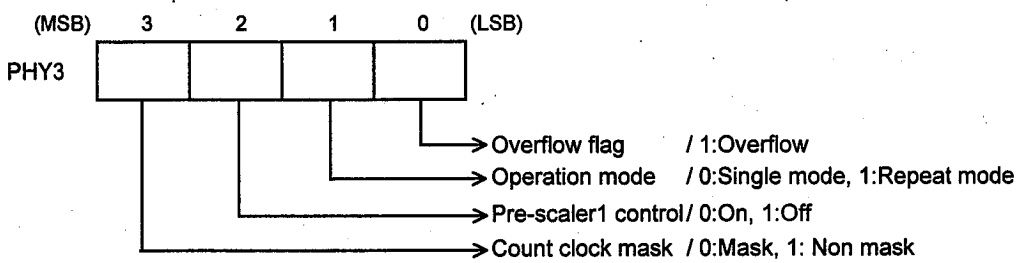
EX.) An example of the start procedure in the single mode and releasing the count clock mask.

```
        :
        :
SRPC            ;
LDI     Y, 3    ;PHY3(Timer1/Pre-scaler Control Register) is pointed.
LDI     A, %1000;"1000"(BIN) is stored to accumulator          ] Single mode, releasing the count
TAP             ;Data is transferred from accumulator to PHY3 ] clock mask Pre-scaler is enable.
LDI     A, %1001;"1001"(BIN) is stored to accumulator          ]
TAP             ;Data is transferred from accumulator to PHY3 ] The count is started.
        :
        :
```

Remarks) When the pre-scaler1 generating the count clock is stopped the operation, Timer is also stopped. But the data in the counter is kept. Therefore Timer can continue to count from the kept condition of the counter when the pre-scaler1 is started the operation again. However, the clocks from the pre-scaler1 are delivered to Serial I/O, therefore the pre-scaler1 requires careful operation, especially stop or start.

When the pre-scaler1 is started the operation again after it was stopped, it is reset and start to count from "zero".

[Reading from the Timer1 / Pre-scaler Control Register]

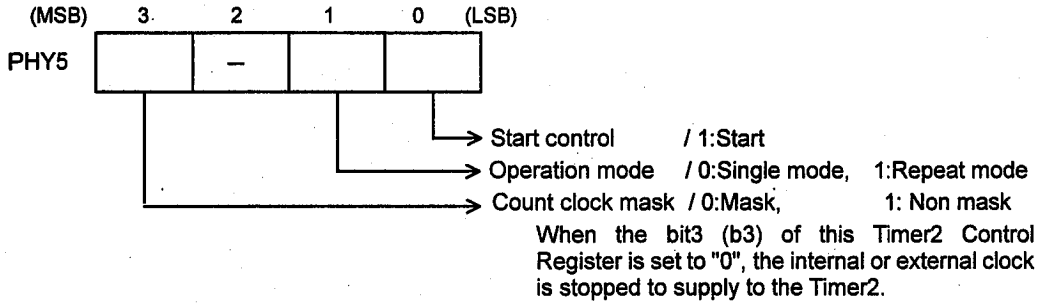


EX.) An example of the overflow in the single mode and releasing the count clock mask.(The data of the Timer1 / Pre-scaler Control Register is "1001"(BIN).)

```
        :
        :
SRPC            ;
LDI     Y, 3    ;PHY3(Timer1/Pre-scaler Control Register) is pointed.
TPA             ;"1001"(BIN) of PHY3 is transferred to accumulator.
        :
        :
```

- Timer2 Control Register { PHY5 ; (Y'=5, Peripheral register table 0) }

[Writing to the Timer2 Control Register]

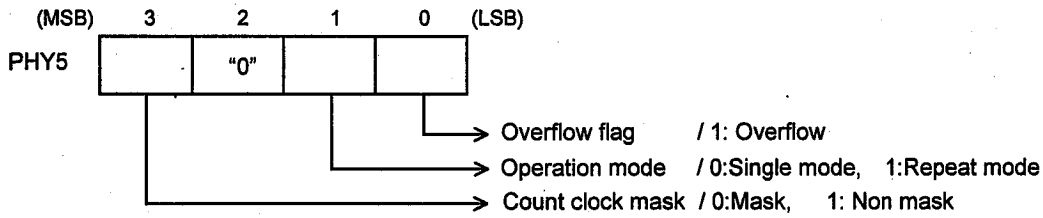


EX.) An example of the start procedure for the repeat mode and releasing the count clock mask.

```
        :
        :
SRPC            ;
LDI     Y, 5    ; PHY5(Timer2 Control Register) is pointed.
LDI     A, %1110; "1110"(BIN) is stored to accumulator          ] Repeat mode,
TAP             ; Data is transferred from accumulator to PHY5  ] releasing the count clock mask.
LDI     A, %1111; "1111"(BIN) is stored to accumulator          ]
TAP             ; Data is transferred from accumulator to PHY5  ] The count is started.
        :
        :
```

Remarks) In the Timer2 operation, when the count clock mask bit(b3) of the Timer2 Control Register is set to "0", the Timer2 is stopped to count and it holds the latest data of the 8-bit counter2. When the b3 is set to "0", the Timer2 starts to count from the hold data of the 8-bit counter2.

[Reading from the Timer1 / Pre-scaler Control Register]



EX.) An example of the Timer2 starting information as the Single mode and the released clock mask. (The data of Timer2 Control Register is "1001"(BIN).)

```
        :
        :
SRPC            ;
LDI     Y, 5    ;PHY5(Timer2 Control Register) is pointed
TPA             ;Data is transferred "1001"(BIN) of PHY5 to accumulator
        :
        :
```

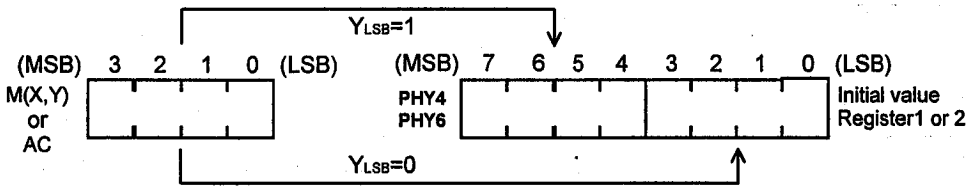
- Initial Value Register / Timer Counter

Initial Value Register1 / Timer Counter1 { PHY4; (Y'=4, Peripheral register table 0) }
Initial Value Register2 / Timer Counter2 { PHY6; (Y'=6, Peripheral register table 0) }

The Initial Value Register consisted of a 8-bit register sets the initial value to the counter, or gets the counted value from the counter.

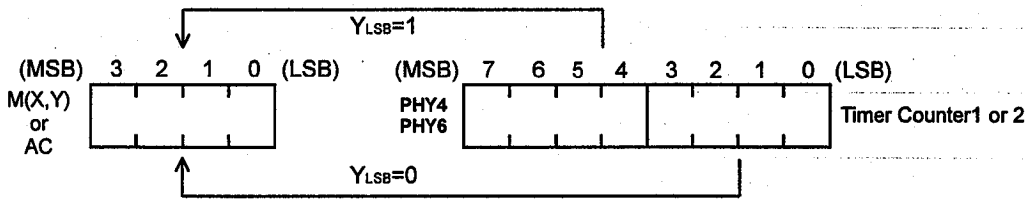
[Writing to the Initial Value Register 1 or 2]

When a data in RAM or Accumulator is transferred to the Initial Value Register1, the data is loaded into the higher 4-bit(b7 - b4) or lower(b3 - b0) of the Initial Value Register1 in accordance with the condition of LSB of Y-register.



[Reading from the Timer Counter1]

When a current data in the Timer Counter1 is transferred into RAM or Accumulator, the data is gotten from higher 4-bit(b7 - b4) or lower(b3 - b0) of the Timer Counter1 or Timer Counter2 in accordance with the condition of LSB of Y-register.

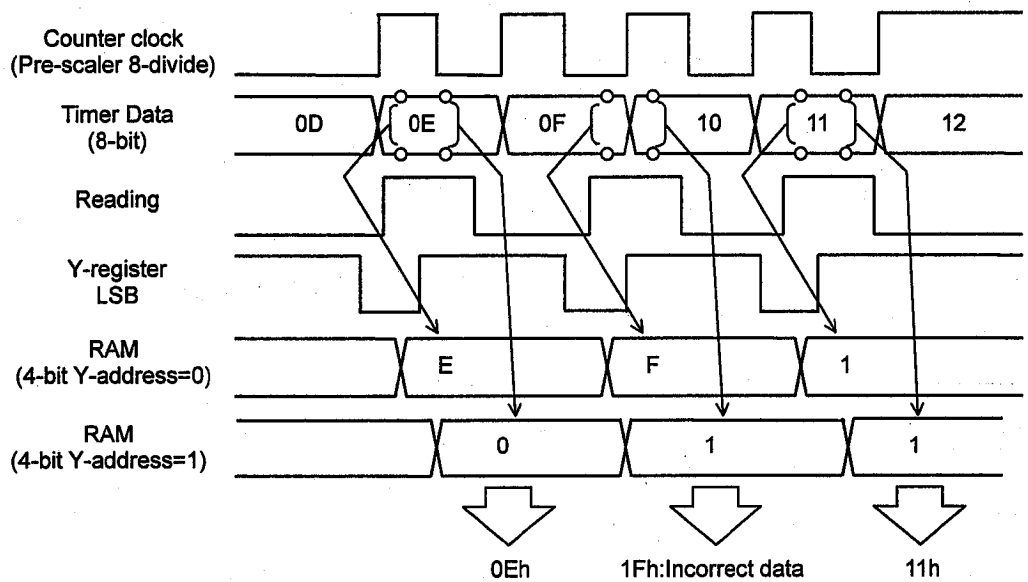


[Reading data from 8-bit Timer Counter1 to RAM]

Though the data of the Timer and Counter can be read in the count operation, the read data is sometimes incorrect when the clock inputs to the counter during the reading operation.

When the 8-bit counter data is read in count operation as shown in the following timing chart (An example of data reading from the counter to RAM), Timer often counts up between the first 4-bit data reading and the second. In case of the following chart, though the timer data is "0Fh" when the lower 4-bit data is gotten, it is "10h" when the higher 4-bit data is gotten. Therefore the final data becomes to be "1Fh".

[An example of data reading from Timer Counter1 to RAM]

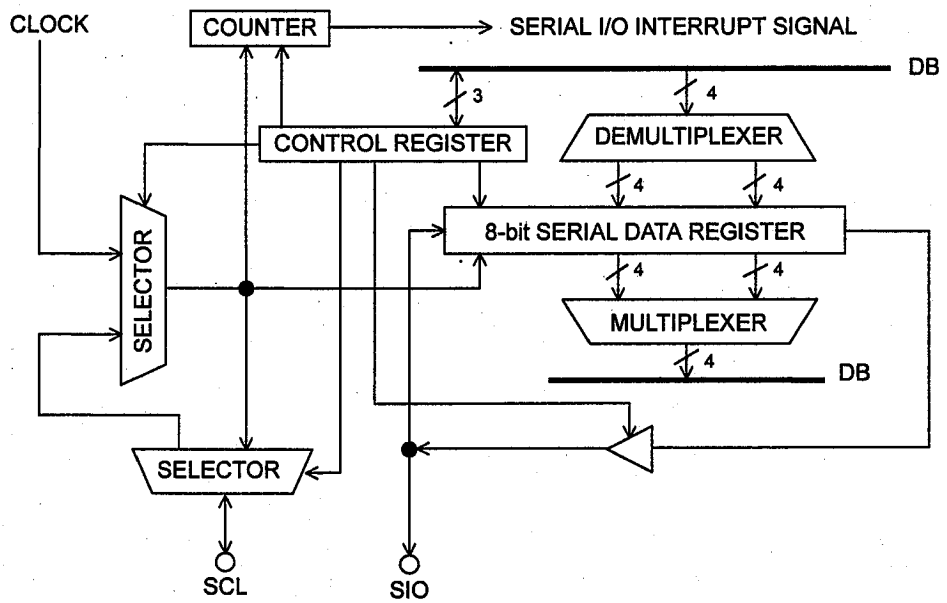


There are some other cases to read the incorrect data from the 8-bit counter during the count operation.

■ SERIAL INPUT OUTPUT

SERIAL INPUT OUTPUT consists of the sift registers to convert from 8-bit parallel data to serial data, the 3-bit serial clock counter, and the 3-bit serial control register. It operates as the 8-bit serial input or output. The external or internal clock is selected for the shift clock in accordance with the Serial Input / Output control register.

[Block diagram of the SERIAL INPUT OUTPUT]



The serial input or output operation starts when the LSB of the Serial Input / Output control register (PHY1) is set "1". In the external clock operation, the serial input or output operation waits to start until the external clock comes in.

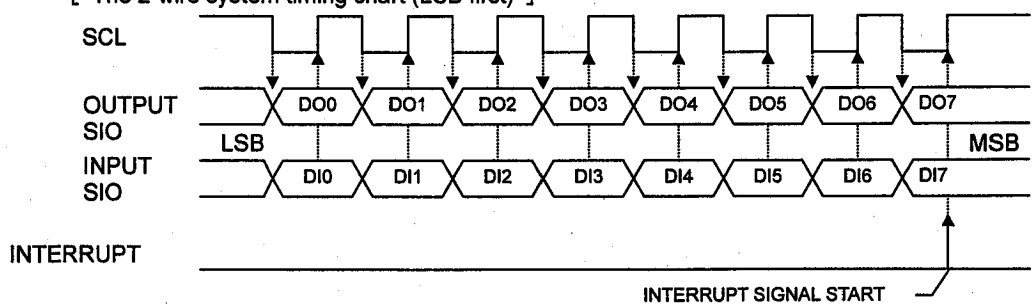
When the serial shift register (PHY2) is set the data in advance, the data is output (transmitted) through the SIO terminal. The SIO terminal can be changed as a transmitter or a receiver in accordance with the bit3(b3) of PHY1. The data order, MSB or LSB first, is selected by the mask option.

Serial Input Output operates as the 2-wire system with SIO and SCL.

The data synchronized with the falling edge of the SCL clock is transmitted through the SIO terminal. The data synchronized with the rising edge of the SCL clock is received through the SIO terminal.

※ In case of the data transmission through the SIO terminal, the SIO terminal must be set the output by the condition of the bit3(b3) in Serial Input / Output control register (PHY1) set "1" .
Incase of the data receiving through the SIO terminal , the SIO terminal must be set the input terminal by the condition of the b3 on PHY1 set "0".

[The 2-wire system timing chart (LSB first)]



In case of the external clock operation, the external clock is inputted as the Serial Clock (SCL) to the SCL terminal as shown in the 2-wire system timing chart. The signal condition into the SCL terminal must be kept as "HIGH" until the external clock come in. In the communication, when the CLK with the noise or other redundant signals from the outside of **NJU3905** input to the CLK terminal, Serial Input Output operates incorrectly. The maximum frequency of the SCL is 500kHz.

In case of the internal clock operation, the SCL outputs through the SCL terminal as shown in the 2-wire system timing chart. The internal interrupt signal occurs when the 3-bit counter has counted the SCL clock up to 8 times that means 1-byte serial data communication end. The internal clock as the SCL is divided clock in the internal pre-scaler, and the frequency of the clock can be selected by the mask option from follows which are dividing numbers based on the inverse of the 1-instruction executing period(6/ f_{osc}).

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

Remarks 1) When the bit2 (b2) of Timer1 / Pre-scaler control register (PHY3) is set "1", the pre-scaler generating the internal serial clock is stopped and the internal serial clock also stopped. Accordingly, Serial Input Output does not operate.

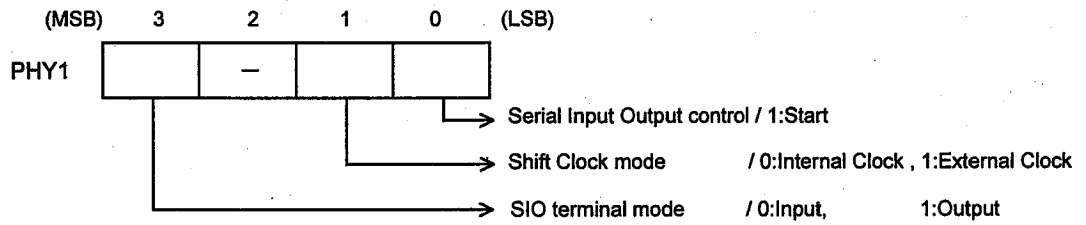
Remarks 2) If the writing operation is operated to the Serial Input / Output shift register (PHY2) or the Serial Input / Output control register during the transmission or the reception operation, the 3-bit counter is reset and the serial data transmission or reception is stopped. Therefore the writing operation to the above registers must not be operated during the transmission and the reception operation.

Remarks 3) When the external clock is selected as the shift clock, a voltage level of the SCL terminal is made "HIGH" during the transmission and reception are stopping.

- SERIAL INPUT / OUTPUT CONTROL REGISTER {PHY1;(Y' = 1)}

When the data of bit1 (b1) and bit3 (b3) of the Serial Input / Output control register are changed, the operation must be perform before starting the serial transmission or reception. (See the following sample program) In change the condition of b1 and b3 on PHY1 and setting the LSB of PHY1 to start the communication are operated at the same time, Serial Input Output operation dose not operate correctly.

[Writing to the Serial Input / Output Control Register]

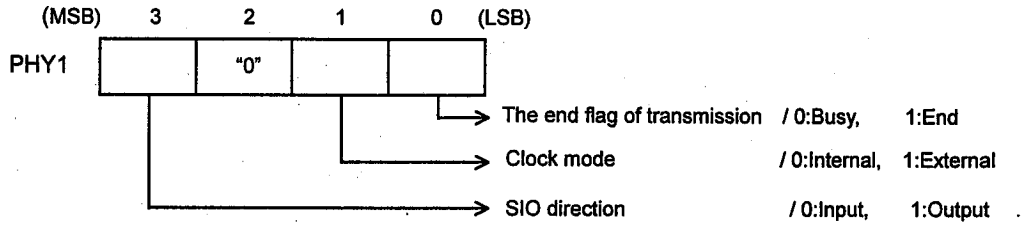


EX.) An example of the start procedure in the serial data communication, the external clock operation and the SIO terminal setting as the input.

```
        :
        :
SRPC            ;
LDI     Y, 1    ;PHY1(Serial Input / Output control register) is set
LDI     A, %0010 ; "0010"(BIN) is stored to accumulator          ┐ External clock,
TAP              ; Data is transferred from accumulator to PHY1  ┘ Input mode
LDI     A, %0011 ; "0011"(BIN) is stored to accumulator          ┐
TAP              ; Data is transferred from accumulator to PHY1  ┘ Transmission Starts
        :
        :
```

Remarks 4) In case of the external clock operation at the both of the transmission and reception mode, inputting the external clock must wait while the 2-instruction execution period after that LSB of Serial Input / Output control register is set "1" (START).
(one instruction execution period = 1/ f_{osc} × 6)
If the external clock is input within the 2-instruction execution period, the Serial Input / Output shift register can not recognize the first SCL. The number of the shift operation is decreased a time, 8 times to 7.

[Reading from the Serial Input / Output Control Register]



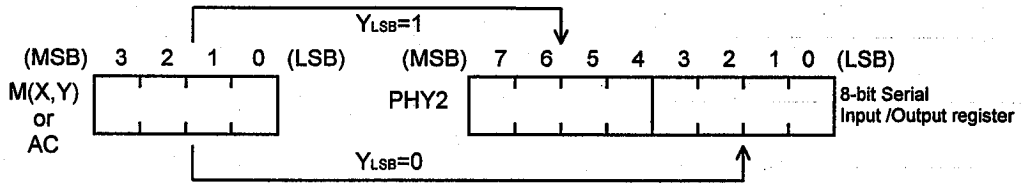
Remarks 5) The end flag of transmission is set "1" when the serial data (8bits) transmission operation is ended. It is cleared by setting the serial data transmission start signal in the Serial Input / Output control register.

- SERIAL INPUT / OUTPUT SHIFT REGISTER {PHY2;(Y' =2)}

The Serial Input / Output Shift register consisted of a 8-bit register operates to set the transmission data or get the reception data.

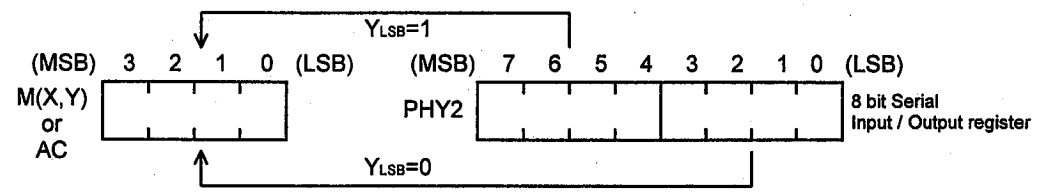
[Writing to the Serial Input / Output Shift Register]

The data in RAM or Accumulator is transferred to the Serial Input / Output Shift register, and it is loaded into lower 4-bit (b0 to b3) or higher (b4 to b7) in PHY2 in accordance with the condition of LSB of Y-register.



[Reading from the Serial Input / Output Shift Register]

The Serial Input data is transferred to RAM or Accumulator, it is loaded from lower 4-bit (b0 to b3) or higher (b4 to b7) of PHY2 in accordance with the condition of LSB of Y-register.



An example of the serial data reception program

In the internal clock operation, SIO terminal is set as the input and the serial input data is transferred to RAM.

```
                :
                :
                :
; -----    Interrupt process    -----
          ORG    $40          ; Interrupt vector address of FULL or EMPTY
SINT      SRPC                ;
          LDI    Y, 1         ; The Serial Input / Output control register is set
          TPA                 ;
          TBA    0            ; The end flag of transmission is tested
          JMP    SIO_OK       ;
          JMP    SINT_E       ;
;
SIO_OK    LDI    Y, 2         ; The Serial Input / Output shift register is set
          RRPC                ; RAM to store the serial input data is set
          LDI    X, SIO_DAT.X ; RAM address, X=0
          LDI    Y, SIO_DAT.Y ; RAM address, Y=0
          TPMICY              ; The serial input data is transferred to RAM (lower 4-bit)
                              ; and Y-register is incremented
          TPMICY              ; The serial input data is transferred to RAM (higher 4-bit)
                              ; and Y-register is incremented
;
SINT_E    RETI                ; End of the interrupt process
;
; -----  Serial data inputting process  -----
SIO_IN    SRPC                ;
          LDI    Y, 0         ; The peripheral register table is set
          CLA                 ;
          TAP                 ;
;
          LDI    Y, 1         ; The Serial Input / Output control register is set
          LDI    A, %0000     ; The internal clock operation is set and the SIO
                              ; terminal is set as the input
          TAP                 ;
          LDI    A, %0001     ; The serial data reception is started
          TAP                 ;                                        ;
;
                :
                :
                :
          WSEG                ; The RAM area is set
SIO_DAT   DS     2            ; The area to store the serial input data is secured
```

An example of the serial data transmitting program

In the internal clock operation, the SIO terminal is set as the output and the data in RAM is transmitted.

```
                :
                :
                :
; -----   Interrupt process   -----
          ORG     $40           ; Interrupt vector address of FULL or EMPTY
SINT      SRPC                  ;
          LDI     Y, 1          ; The Serial Input / Output control register is set
          TPA                   ;
          TBA     0             ; The end flag of transmission is tested
          JMP     SIO_OK        ;
          JMP     SINT_E        ;
;
SIO_OK    RRPC                  ; End of the interrupt process
          LDI     X, SIO_FLG.X  ;
          LDI     Y, SIO_FLG.Y  ;
          LDI     A, 1          ;
          TAM                   ;
;
SINT_E    RETI                  ; The peripheral register table is set
;
; -----   Serial data transmitting process   -----
SIO_OUT   SRPC                  ;
          LDI     Y, 0          ; The peripheral register table is set
          CLA                   ;
          TAP                   ;
;
          LDI     Y, 2          ; The Serial Input / Output shift register is set
;
          RRPC                  ; RAM to store the serial output data is set
          LDI     X, SIO_DAT.X  ; RAM address,  X=0
          LDI     Y, SIO_DAT.Y  ; RAM  address, Y=1
          TMPICY                ; The data in RAM is transferred to the Serial Input / Output shift
                                ; register (lower 4-bit) and Y-register is incremented
          TMPICY                ; The data in RAM is transferred to the Serial Input / Output shift
                                ; register (higher 4-bit) and Y-register is incremented
;
          SRPC                  ;
          LDI     Y, 1          ; The Serial Input /Output control register is set
          LDI     A, %1000      ; The internal clock operation and the transmission mode are set
          TAP                   ;
          LDI     A, %1001      ; The serial data transmitting operation is started
          TAP                   ;
;
                :
                :
                :
          WSEG                  ; The RAM area
SIO_DAT   DS      2             ; The end flag of transmission
SIO_FLG   DS      1             ; The area to store the serial output data
```

■ INTERRUPT

NJU3905 prepares four kinds of the interrupt. The interrupt "enable" or "disable" is controlled by the program. The interrupt operates as single process and no multiple. However, when new interrupt request occurs during the other interrupt process, the request is kept, and then the new interrupt process starts after the prior interrupt process. The priority order of the interrupts that the first is (1) External interrupt-1, the second is (2) internal interrupt-1, the third is (3) internal interrupt-2, and the fourth is (4) Internal interrupt-3 as shown in follow.

When the interrupt request flag is set by the own factor, the interrupt enabled by the interrupt control register (PHY8) stores the data of Program Counter, Accumulator, X-reg, X'-reg, Y-reg, Y'-reg, PRC, and STATUS into the STACK register, and sets the interrupt vector address into Program Counter, and then the interrupt process is started. The return from the interrupt process by "RETI" instruction resets the corresponded interrupt request flag, and regains the held data from STACK, and then the operation before the interrupt process is started continuously. When the interrupt control register disables the interrupt process, the interrupt request flag is not set.

[THE PRIORITY ORDER OF FOUR INTERRUPTS]

Order	Interrupt			Vector Address(H:HEX)
(1)	External interrupt-1			10H
(2)	Internal interrupt-1	Timer/Counter-1	Overflow	20H
(3)	Internal interrupt-2	Timer/Counter-2	Overflow	30H
(4)	Internal interrupt-3	Serial shift register	Full/ Empty	40H

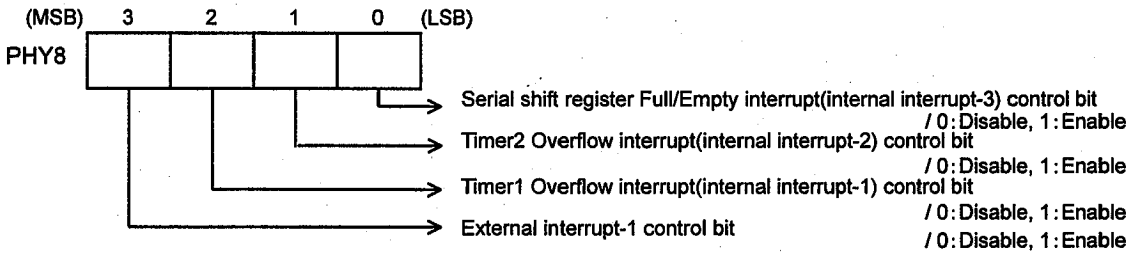
The External Interrupt-1 can get interruption request by the edge of external signal interrupt input terminal(EXTI). A edge direction of external interrupt signal can be selected by mask option. The External Interrupt takes precedence over another interrupts. The external interrupt-1 request flag is reset by "RETI" instruction. When the external interrupt-1 occurs during the standby mode by "HLT" instruction, the External interrupt-1 request signal is latched and its interrupt process is started after that the standby mode is released.

The Internal interrupt enable by PHY8 is started the interrupt process when the internal interrupt request flag is set.

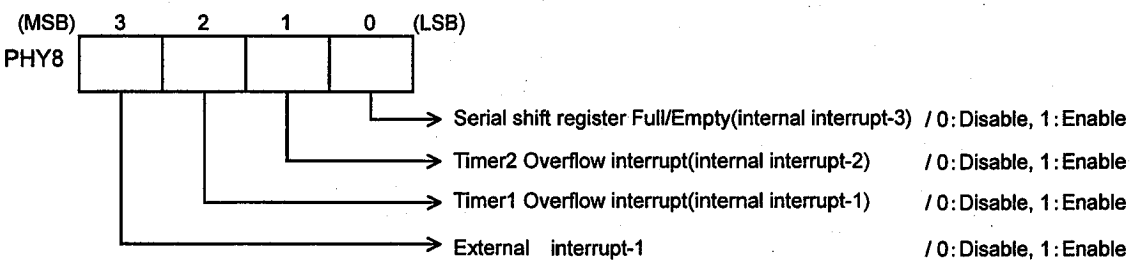
The Timer1 and the Timer2 interrupt request flags are independent of the overflow flag, and they are reset by "RETI" instruction, (TIMER)START signal of the Timer control register, or RESET signal from the external circuit. Serial Input Output interrupt request flag is set synchronizing with the transmission end flag when its interrupt is enabled by PHY8. And the flag is reset by the "RETI" instruction or the RESET signal from the external circuit.

- INTERRUPT CONTROL REGISTER {PHY8;(Y' =8)}

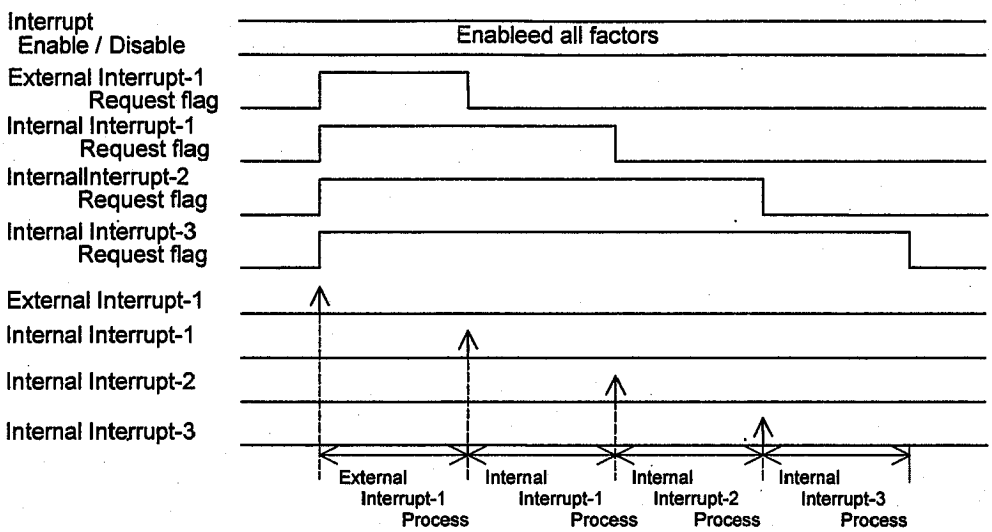
[Writing to the Interrupt Control Register]



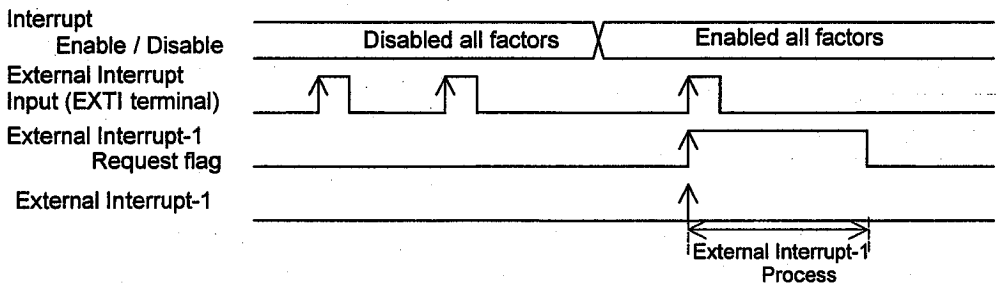
[Reading from the Interrupt Control Register]



[Enable all factors (b0 to b3 of PHY8 were set "1")]

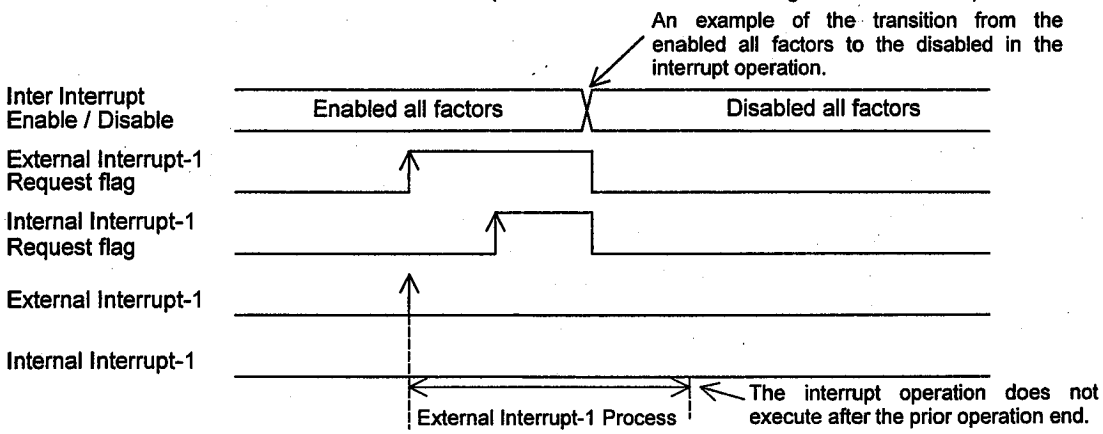


[From the all factors enabled to the disabled (b0 to b3 of PHY8 are changed from "1" to "0")]



※ The internal interrupt is also ignored while it is disabled.

[From the all factors enabled to the disable (b0 to b3 of PHY8 are changed from "1" to "0")]



※ When the interrupt is enabled, the latest interrupt request occurred during the prior other interrupt process starts its interrupt process after the prior interrupt operation. However, when the interrupt is disable during the prior interrupt process as shown in above timing chart, the latest interrupt request dose not start. But the prior interrupt process is completed.

■ INCORPORATED LCD DRIVER

The features of the Incorporated LCD Driver are shown as follows.

- The common signal outputs: 4 or 2 lines. / The segment signal outputs: 32 lines (MAX.).
- The Display mode: 1/2 Duty(1/2Bias) or 1/4 Duty(1/3 Bias). (mask option)
- On Chip Bleeder resistance for LCD Bias
- Display ON / OFF, Power Save ON / OFF, and Transmission Start of the display data for extension LCD driver can be controlled by program.
- LCD Segment Driver can be extended by connecting another LCD Driver IC. The interface for the extension LCD segment driver.

(1) General Description of Incorporated LCD Driver

The Incorporated LCD driver is consisted of the RAM for display, Timing controller, Common Driver, and Segment Driver. The **NJU3905** can drive panel which is consisted of 4 commons and 32 segments (MAX.) the LCD directory. And it provides the Interface for the Extension LCD Driver by mask option setting. The **NJU3905** with extension LCD driver can drive the 4 commons and 94 segments LCD panel.

In case of driving with the Extension LCD Driver, segment driver output terminals of **NJU3905** are reduced to 24 lines from **NJU3905**.

(2) Clock Generator for the Incorporated LCD Driver

The flame frequency of LCD Driver is supplied from the output of the Internal pre-scaler2 and one of frequency is selected from following frequencies by mask option. It is divided using inversion of 1-instruction $\{1/f_{OSC} \times 6\}$.

1/64, 1/128, 1/256, 1/384, 1/512, 1/768, 1/1024, 1/1536, 1/2048, 1/3072, 1/4096, 1/6144, 1/8192

[Relations between Master Clock and LCD Flame Frequency]

Examples of Selecting the LCD driver Flame Frequency are shown .

Master Clock of NJU3905	Flame Frequency of Incorporated LCD Driver Divided Frequency in the Pre-scaler2					
	1/64	1/1024	1/2048	1/4096	1/6144	1/8192
4MHz						81.4Hz
3MHz					81.4Hz	
2MHz				81.4Hz		
1MHz			81.4Hz			
455kHz		74.1Hz				
32.768kHz	85.3Hz					

(3) Select Duty

The 1/2Duty(1/2Bias) of LCD panel driving or 1/4Duty(1/3Bias) is selected by mask option.

Due to the bleeder resisters between each V_{LCD} and V_{SS}, the V_{LCD} driving Voltage shown in [Output Voltage Level at 1/2 Duty or 1/4Duty] are output from LCD driving Voltage(V_{LCD}) source terminals, V_{LCD0} and V_{LCD1}. But capacitors should be connected to them for V_{LCD} stable operation.

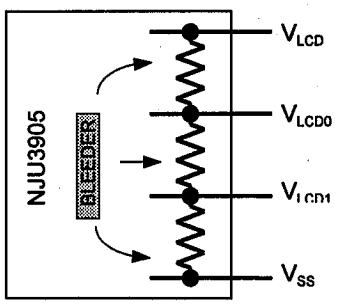
The LCD driving Voltage (V_{LCD}) can be adjusted by the external resisters or others.

[Output Voltage Level at 1/2Duty or 1/4Duty]

	1/2Duty	1/4Duty
V_{LCD}	V_{LCD}	V_{LCD}
V_{LCD0}	(1/2)·V_{LCD}	(2/3)·V_{LCD}
$V_{LCD}1$		(1/3)·V_{LCD}
V_{SS}	V_{SS}	V_{SS}

V_{LCD}=2.7~5.5V

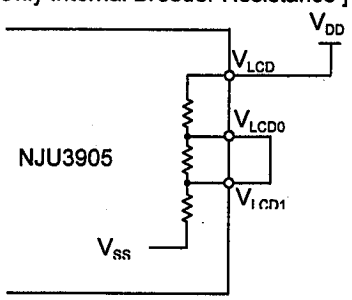
[The circuit of Bleeder]



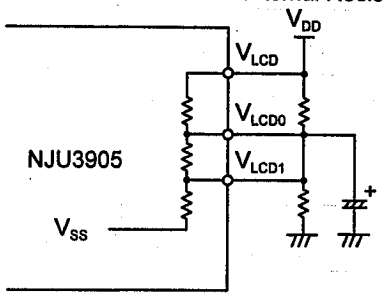
• LCD Voltage Circuit Examples

1/2Duty,1/2Bias

[Only Internal Breeder Resistance]

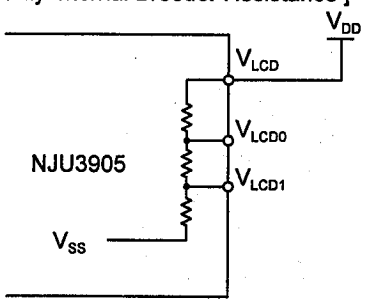


[Internal Breeder Resistance with external Resistance]

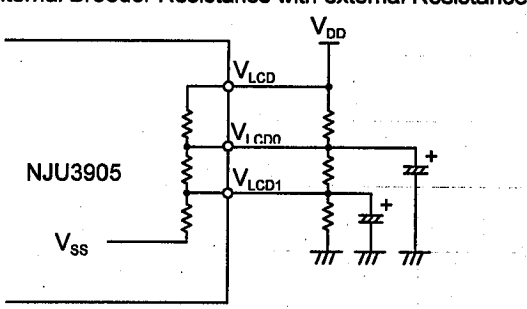


1/4Duty,1/3Bias

[Only Internal Breeder Resistance]

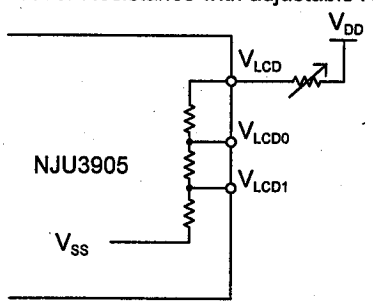


[Internal Breeder Resistance with external Resistance]



1/4Duty,1/3Bias

[Internal Breeder Resistance with adjustable Resistance]



(4) LCD Control Register (PHY7)

The LCD Driver is controlled by the LCD Control Register (PHY7) which is consisted of the Display Control Bit(b0), the Power Save Control Bit(b1), and the Data Transfer for the extension LCD driver Control Bit(b2). The data in the extension LCD driver RAM area is transferred to the Extension LCD Driver, when **NJU3905** drives a LCD panel with it.

This data transfer must be programmed to operate after the Extension LCD Driver is reset or at the renewal of the data in extension LCD driver RAM area.

The speed of this data transfer depends on the Master Clock only, and dose not depend on the Flame Frequency.

- Display ON / OFF Control (b0)
- Power Save ON / OFF Control (b1)

Relations between the command of Display ON / OFF Control and Power Save ON / OFF Control setting and the Display Condition are shown on the table of [Input Command and Display].

At Power Save ON, the internal condition of **NJU3905** is shown as follows.

① The current consumption of the Incorporated LCD Driver become nearly 0 μA.
② Driving the LCD is stopped and the Output Level of segment and common become V_{SS}
③ The Display Data and Operating Mode before **NJU3905** is made Power Save Mode is held.

[Input Command and Display]

Input Command (Peripheral Register PHY7)		LCD Panel
b1	b0	
0	0	Display ON
0	1	Display OFF
1	*	Power Save ON

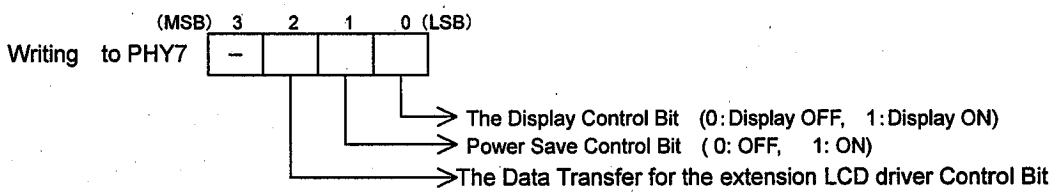
* : don't care

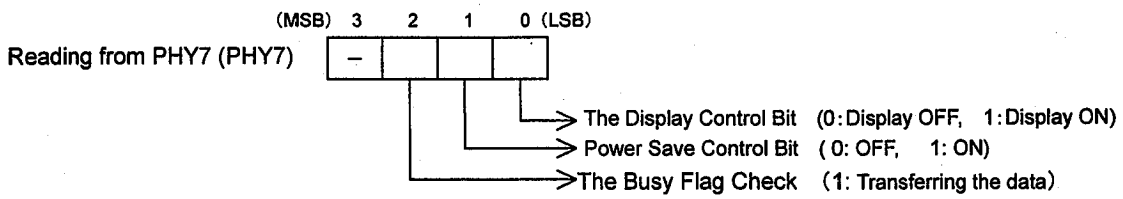
- Transferring the data for the extension LCD driver Start Control (writing to b2) :
  Transferring the data for the extension LCD driver is started by writing "1" to b2.
  Writing "0" to b2" is not needed.

- Busy Flag Check (reading from b2) :
  The Data Transfer for the extension LCD driver Control Bit(b2) is made to set "1" during transferring the data. During this time, b2 can not be written.

Note) At reset, b0 is set "0" (Display OFF) and b1 is set "0" (Power Save OFF).

[LCD Control Register (PHY7)]



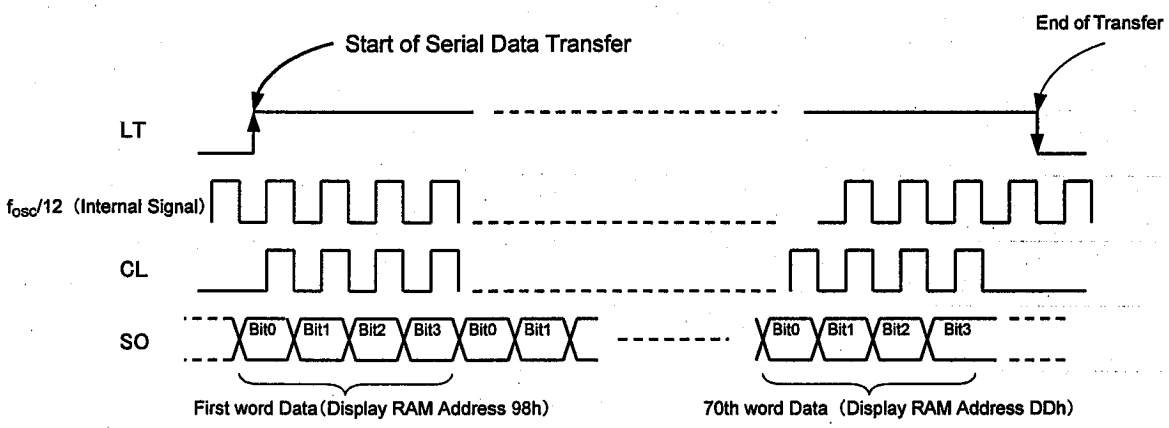


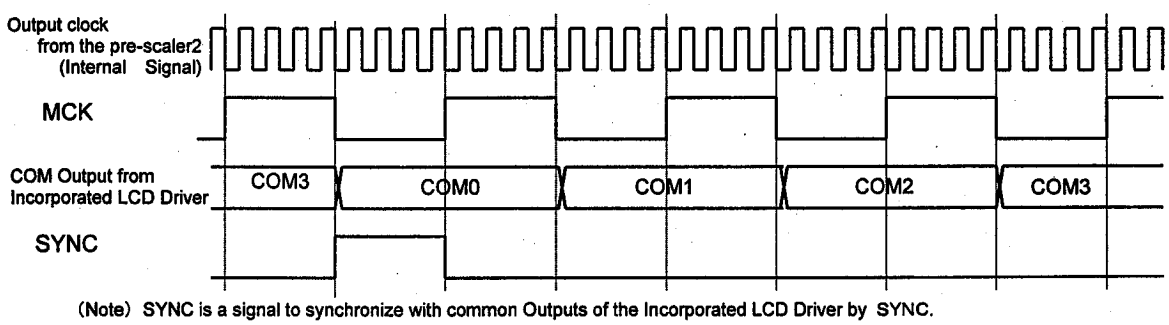
(5) INTERFACE FUNCTION FOR EXTENSION LCD DRIVER

NJU3905 provides LT, SYNC, MCK, SO, and CL signals of the interface for the Extension LCD Driver. Those signals are in shown in fellow in busy of data transfer

Interface Signal	Functions and Operating Conditions
LT	Serial Data Latch Signal While the Serial Data is transferred, high level is output. Low level is output from end of transfer to start of next transfer.
SYNC	Synchronization signal to the extension LCD driver (refer [Serial Interface Output for the Extension LCD Driver Timing Chart])
MCK	Master Clock to the extension LCD driver (The frequency of MCK is four times against the flame frequency.
SO	Serial Data to the extension LCD driver The data in the display RAM (address: 98H~DDH) are output in order from b0 to b3. A transfer data is 70 words.(4bit × 70= 280bit : A word is consisted of b0, b1, b2, and b3.)
CL	Data shift Clock to the extension LCD driver It is output when the LT terminal is high. It is not output when the terminal is low . Number of shift clock is 280 (4 × 70) clocks.

[Serial Interface Output to the Extension LCD Driver Timing Chart]





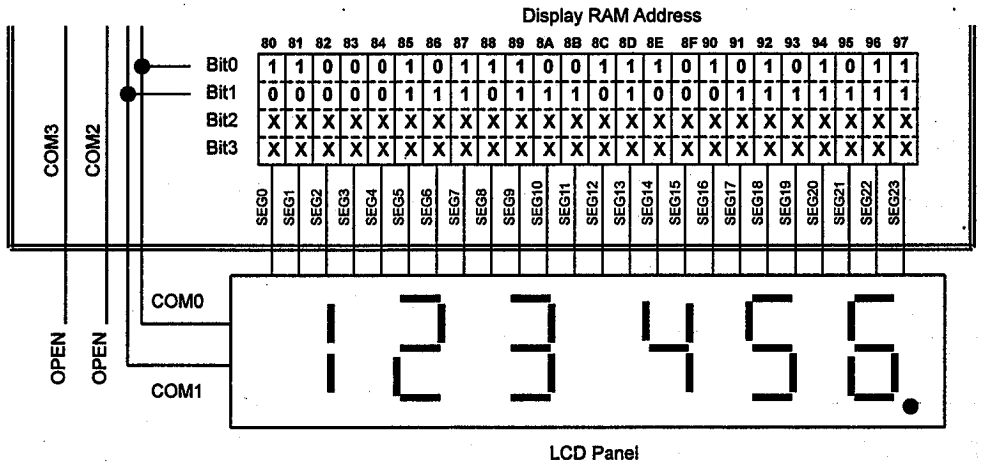
(Note) SYNC is a signal to synchronize with common Outputs of the Incorporated LCD Driver by SYNC. When COM0 and MCL are "low", SYNC is "high" .

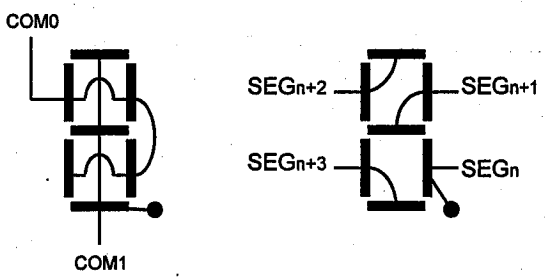
(6) Display Data and Display Data RAM

Relations between the Display Data and the Display Data RAM address is shown in [The example of LCD Display Image]. LCD Display is indicated when a RAM Data is set "1" and Display Control is ON .

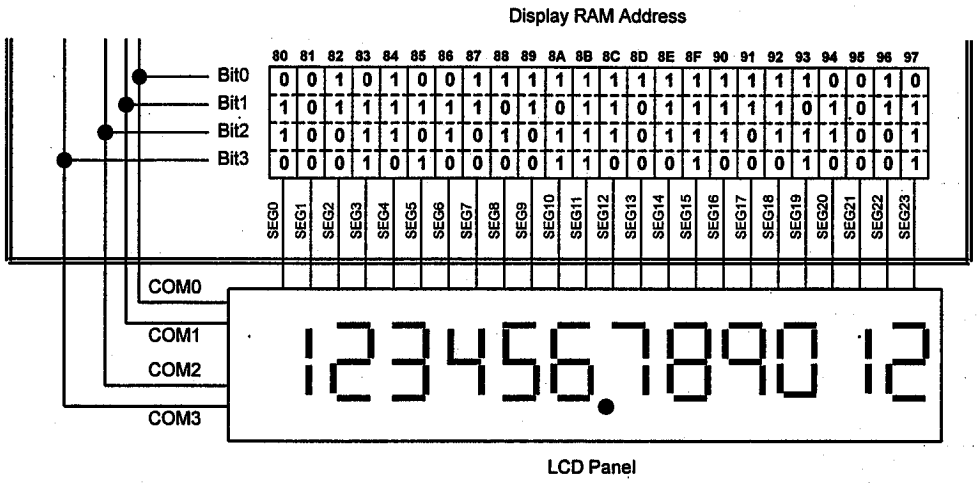
[The Example of LCD Display Image]

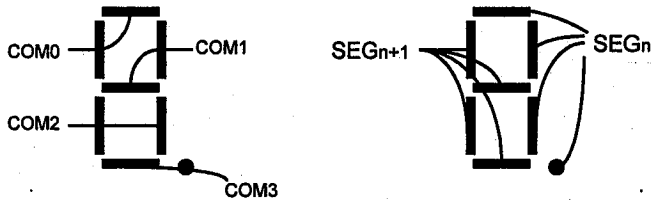
- 1/2Duty(1/2Bias)





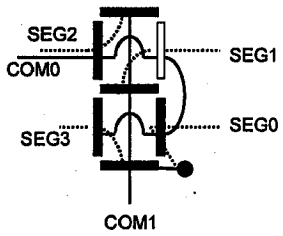
• 1/4Duty(1/3Bias)



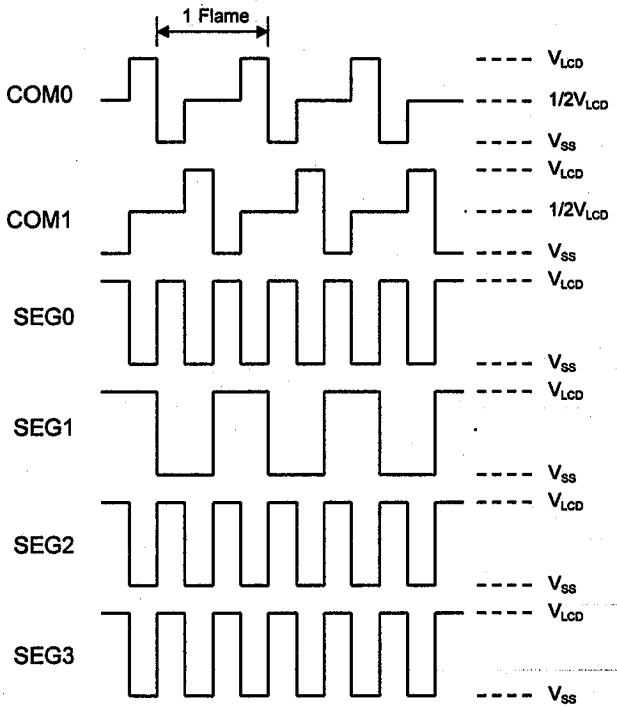


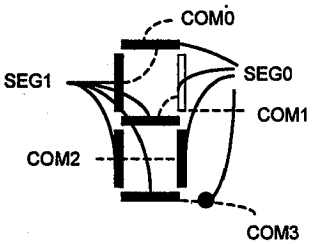
[The Example of LCD Driving Waveform]

1/2duty(1/2bias)



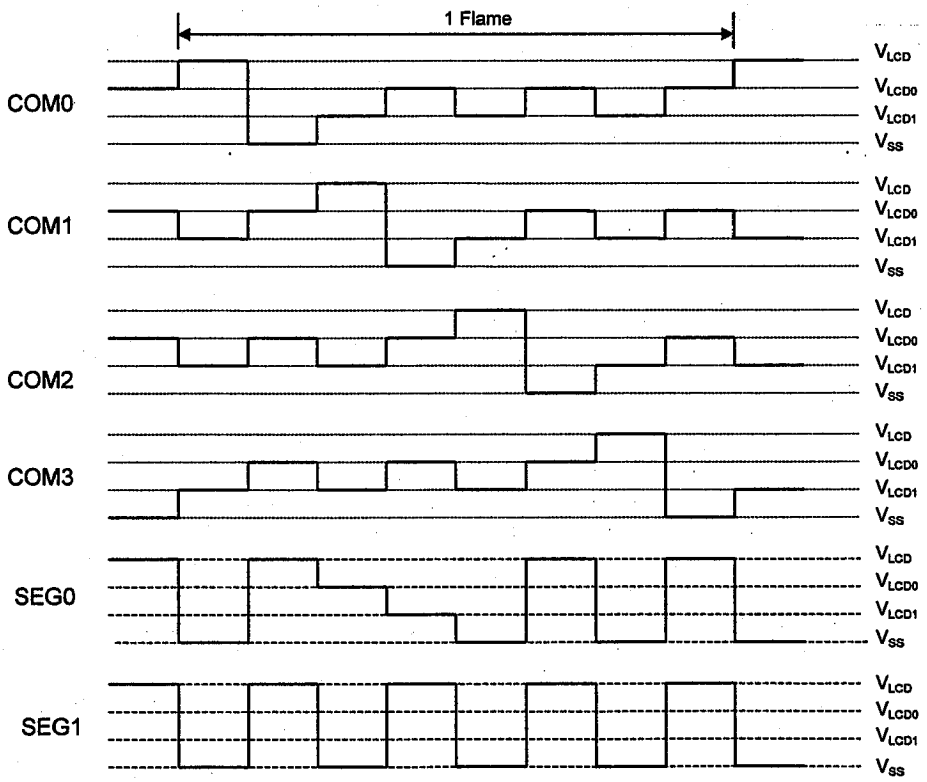
1/2Duty(1/2Bias)





1/4Duty(1/3Bias)

1/4duty(1/3bias)



■ STANDBY FUNCTION

STANDBY FUNCTION halts the IC operation and reduces the current consumption.

The STANDBY function starts by the HLT instruction. After the HLT instruction execution cycle, the internal oscillator operation is stopped and all of the operation is halted. In case of the external clock operation, the clock is stopped automatically delivering into the internal system by the internal circuit, and all operation is halted as same as the internal oscillator operation. This is STANDBY mode.

In the STANDBY mode, the operating current can be reduced. Though the clock into the internal system is stopped and all of the operation is halted, all condition of Program Counter, Registers, and data in RAM are kept certainly.

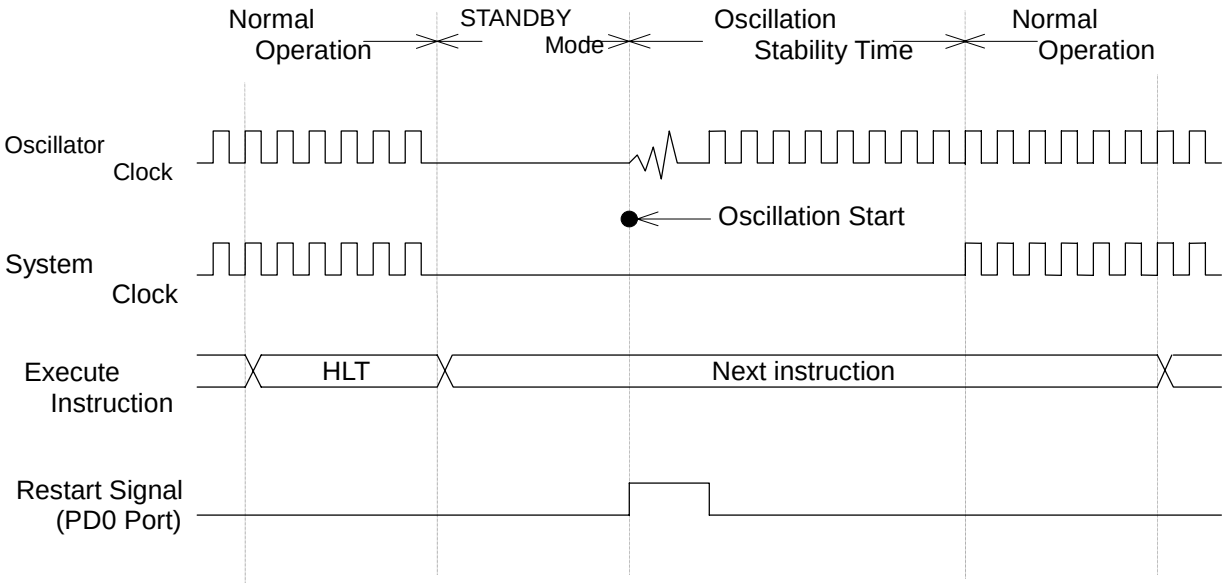
Two ways to release from the STANDBY mode are prepared. One way is the reset operation that when the reset signal is inputted to RESET terminal, the operation starts from the initial condition. The other way is the re-start operation that when the re-start signal is inputted to PD0 terminal, the operation starts from the kept Program Counter location which is the program address after the final operation. In case of the re-start signal operation, if the rising signal, low to high, is input to PD0 terminal, the internal oscillator circuit starts at first. After the stabilized clock from the internal oscillator was counted eight times, the clock is started delivering into the internal system. Then NJU3905 starts to operate from the kept Program Counter location with all of the kept conditions.

In case of the external clock operation, the external clock must be started to supply to the OSC1 terminal before the STANDBY mode is released. The external clock is recommended to stop supplying to the OSC1 terminal for reducing the power consumption during the STANDBY mode.

At way of the re-start signal inputted to PD0 terminal, this terminal must be selected re-start function by mask option.

Note） In order to avoid abnormal displaying, the standby function starting after LCD Driver become Power-Save is recommended.

[STANDBY MODE TIMING CHART]



*1 Selecting PD0 as re-start input terminal only enables **NJU3905** to release from the standby mode by re-start signal inputted to PD.
At reset operation, **NJU3905** becomes operating from initial condition.

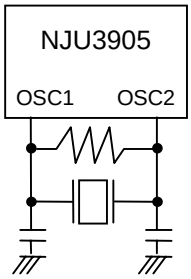
■ CLOCK GENERATION

The system clock is generated in the internal oscillator circuit with the external crystal or ceramic resonator , or the resistor connected to OSC1 and OSC2 terminals. Furthermore , the NJU3905 can operate by the external clock to the OSC1 terminal for the system clock. In the external clock operation, the OSC2 terminal must be opened.

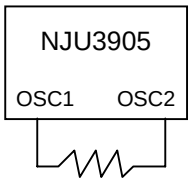
The typical application examples for each oscillator circuit are shown in follows. However a Crystal or a Ceramic operation requires the considered evaluation, because the oscillator operates in accordance with the characteristics of each component.

[OSCILLATOR APPLICATION EXAMPLES]

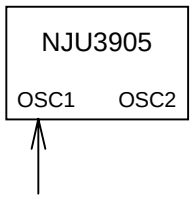
1) X'tal/Ceramic oscillation



2) CR oscillation



3) External clock input

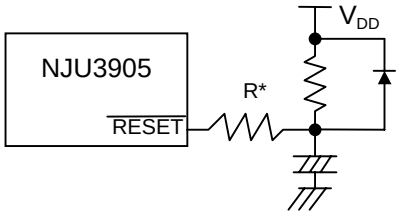


■ RESET OPERATION

All of the internal circuits are initialized by inputting the low level signal to the RESET terminal.

A circuit example for Power ON Reset Operation with a resistor, a capacitor, and a diode is shown in follow. Power On Reset Operation requires to keep the low level of the input signal to RESET terminal until the stabilized oscillation of the internal oscillator. Therefore the constants on the reset circuit must be decided in accordance with the characteristics of the clock generator circuit.

[An example of Power On Reset circuit]



R* : A resister is RESET terminal protector. It is required depending on the condition of an application.

■ PRESCALER

NJU3905 has two Prescalers. The pre-scaler1 can supply the clock to Timer1, Timer2 and Serial Interface. a frequency of the pre-scaler1 can be selected in 12 kinds shown in follows by mask option.

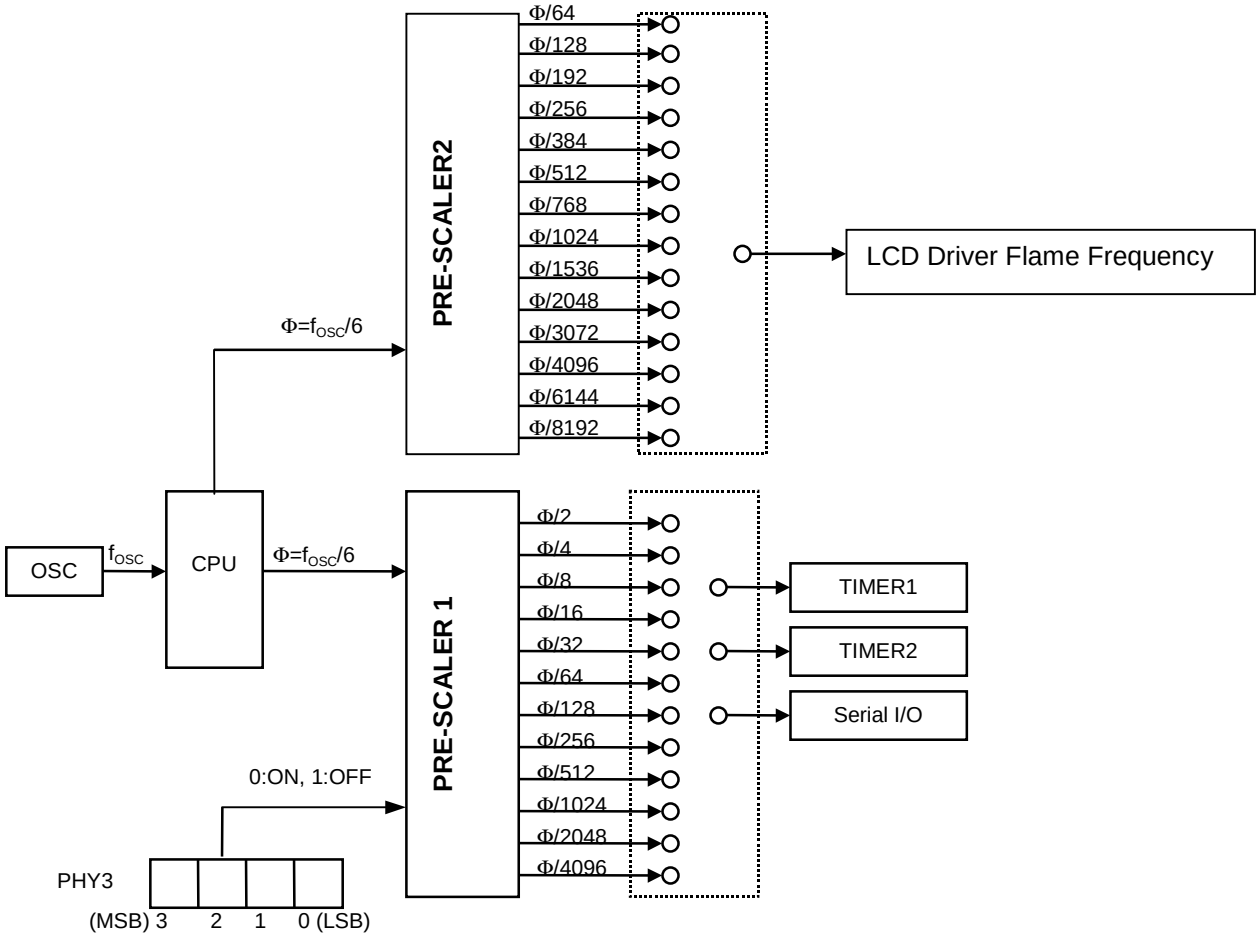
1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

When the bit2(b2) of Timer1 control register (PHY3) is set “1”, the pre-scaler1 operation is stopped, but output clock is also stopped to Timer1, Timer2 and serial interface . When the b2 of PHY3 is set “0”, the Prescaler operation is started to count from “0”.

The Pre-scaler2 can supply the clock of LCD Driver Flame Frequency. A frequency of the Pre-scaler2 can be selected in 14 kinds shown in follows by mask option.

1/64, 1/128, 1/192, 1/256, 1/384, 1/512, 1/768, 1/1024, 1/1536, 1/2048, 1/3072, 1/4096, 1/6144, 1/8192

[AROUND THE PRE-SCALER BLOCK DIAGRAM]



EX.) The output frequency of Prescaler at f_{OSC}=4MHz (Φ=4MHz / 6).

PreScaler Divider	Φ/2	Φ/4	Φ/8	Φ/16	Φ/32	Φ/64	Φ/128	Φ/256	Φ/384
Output Frequency	333.33 kHz	166.67 kHz	83.33 kHz	41.67 kHz	20.83 kHz	10.42 kHz	5.21 kHz	2.60 kHz	1.74 kHz
PreScaler Divider	Φ/512	Φ/768	Φ/1024	Φ/1536	Φ/2048	Φ/3072	Φ/4096	Φ/6144	Φ/8192
Output Frequency	1.30 kHz	868 Hz	651 Hz	434 Hz	326 Hz	217 Hz	163 Hz	108.5 Hz	81.4 Hz

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	-0.3 ~ V_{DD}	V
Operating Temperature	T_{opr}	-40 ~ +85	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 1−1 (V_{DD}=2.7~5.5V, V_{SS}=0V, Ta= -40~85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	2.7		5.5	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz X'tal Oscillation in Reset		2.0	4.0	mA	*3
	I_{DD2}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz Ceramic Oscillation in Reset		2.0	4.0	mA	*3
	I_{DD3}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz CR Oscillation in Reset		1.9	3.8	mA	*3
	I_{DD4}	V_{DD} V_{DD}=5V,Standby Mode			4.0	μA	*3
High-Level Input Voltage	V_{IH1}	PA0/SEG24/LT ~ PA3/SEG27/MCK, PD0, PF0~PF3, PG0~PG3, PH0~PH2, SCL	0.7V_{DD}		V_{DD}	V	*1
	V_{IH2}	PE0/EXTI~PE2, $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-1.0		V_{DD}	V	
Low-Level Input Voltage	V_{IL1}	PA0/SEG24 ~ PA3/SEG27/MCK, PD0, PF0~PF3, PG0~PG3, PH0~PH2, SCL	0		0.3V_{DD}	V	*1
	V_{IL2}	PE0/EXTI~PE2, $\overline{\text{RESET}}$	0		0.2V_{DD}	V	*1
	V_{IL3}	OSC1	0		1.0	V	

*1 Input / Output port is set as an Input terminal.
*2 Input / Output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 1–2 (V_{DD}=2.7~5.5V, V_{SS}=0V, Ta= -40~85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	I_{IH}	V_{DD}=5.5V, V_{IN}=5.5V PA0/SEG24 ~PA3/SEG27/MCK, PD0, PE0/EXTI~PE2, PF0~PF3,PG0~PG3, PH0~PH2, SCL, RESET			10	μA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=5.5V, V_{IN}=0V Without Pull-up Resister PA0/SEG24 ~PA3/SEG27/MCK, PD0, PE0/EXTI~PE2, PF0~PF3,PG0~PG3, PH0~PH2, SCL, RESET			-10	μA	*1
	I_{IL2}	V_{DD}=5.5V, V_{IN}=0V With Pull-up Resister PA0/SEG24 ~PA3/SEG27/MCK, PD0, PE0/EXTI~PE2, PF0～PF3,PG0~PG3, PH0~PH2, SCL			-100	μA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-100μA PA0/SEG24 ~PA3/SEG27/MCK, PC0/SO, PC1/CL, PD0, PG0~PG3, PH0~PH2, SCL	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=400mA PA0/SEG24 ~PA3/SEG27/MCK, PC0/SO, PC1/CL, PD0, PG0~PG3, PH0~PH2, SCL			0.5	V	*2
	V_{OL2}	I_{OL2}=25mA PB0/SEG28~PB3/SEG31			1.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=5.5V, V_{OH}=5.5V PB0/SEG28~PB3/SEG31			10	μA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz		10	20	pF	

*1 Input / Output port is set as an Input terminal.
*2 Input / Output port is set as an Output terminal.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 2 INCORPORATED LCD DRIVER (V_{DD}=2.7~5.5V, V_{SS}=0V, Ta= -40~85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{LCD}	V_{LCD}	2.7		5.5	V	
	V_{LCD0}	V_{LCD0}	$0.4V_{DD}$		V_{DD}	V	*1
	V_{LCD1}	V_{LCD1}	V_{SS}		$0.6V_{DD}$	V	*1
Bleeder Resister	R_b	V_{LCD} –V_{SS} =5V, 1/2bias		20	30	kΩ	
		V_{LCD} –V_{SS} =5V, 1/3bias		30	45	kΩ	
Common Output Impedance	R_{com1}	COM0~COM3	–	5	25	kΩ	*2
Segment Output Impedance	R_{seg1}	SEG0~SEG31	–	10	50	kΩ	*2

*1 LCD driving voltage is adjusted by external circuit.
(Necessary condition : $V_{LCD} \geqq V_{LCD0} \geqq V_{LCD1} \geqq V_{SS}$)

*2 When Voltage (0.1V) is applied between LCD driver an output terminal (SEG/COM) and an supply Voltage terminal (V_{LCD0}, V_{LCD1}) , value of resistance is appeared.

■ ELECTRICAL CHARACTERISTICS

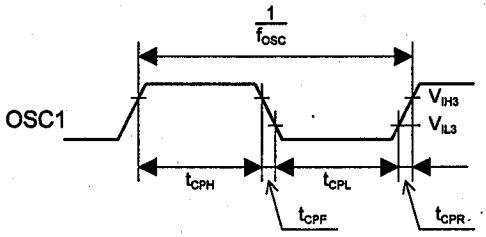
AC CHARACTERISTICS 1

(V_{DD}=2.7~5.5V, V_{SS}=0V, Ta= -40~85°C)

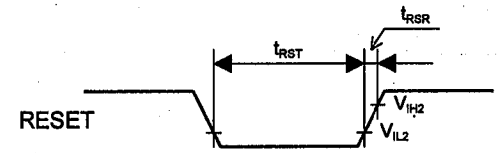
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	NOTE
Operating Frequency	f_{OSC}	X'tal Resonator	0.03		4.0	MHz
		Ceramic Resonator	0.03		4.0	
		External Resister Oscillation	0.03		2.0	
		External Clock	0.03		4.0	
Instruction Cycle Time	t_C			$6/f_{OSC}$		sec
External Clock	t_{CPH} t_{CPL}		125		16600	nsec
External Clock Rise Time Fall Time	t_{CPR} t_{CPF}				20	nsec
RESET Low-Level Width	t_{RST}		$12/f_{OSC}$			sec
RESET Rise Time	t_{RSR}				20	msec
Port Input Level Width	t_{PIN}		$6/f_{OSC}$			sec
Restart Signal Rise Time	t_{STR}	PD0 terminal			200	nsec
External Interrupt Signal Rise Time Fall Time	t_{EXR} t_{EXF}	PE0/EXTI terminal			200	nsec

■ AC CHARACTERISTICS 1 TIMING CHART

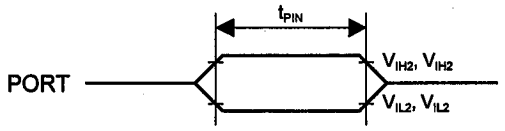
EXTERNAL CLOCK



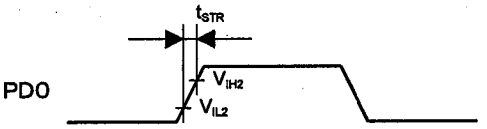
RESET INPUT



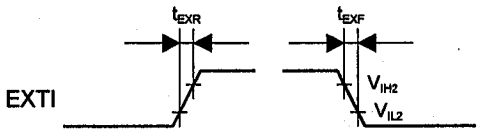
PORT INPUT



RESTART



EXTERNAL INTERRUPT



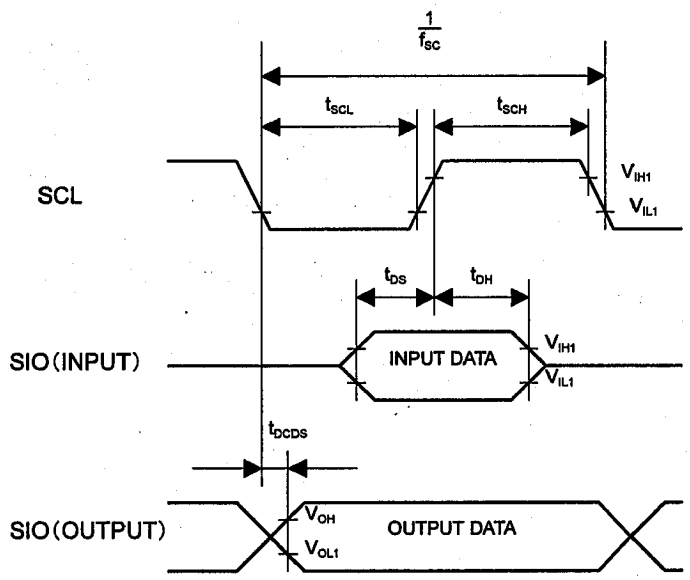
■ ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS 2 SERIAL INTERFACE (V_{DD}=2.7~5.5V, V_{SS}=0V, Ta=-40~85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Serial Operating Frequency	f_{SC}	Internal Clock				(1/12)xf_{OSC}*	Hz
		External Clock				500k	
Clock Pulse Width Low-Level	t_{SCL}	Internal Clock	f_{OSC}=4MHz	1.5			μsec
		External Clock		1.0			
Clock Pulse Width High-Level	t_{SCH}	Internal Clock	f_{OSC}=4MHz	1.5			μsec
		External Clock		1.0			
SIO Setup Time To SCL ↑	t_{DS}			0.5			μsec
SIO Hold Time To SCL ↑	t_{DH}			0.5			μsec
SIO Data Fix Time to SCL	t_{DCD}					0.5	μsec

* The maximum frequency of the internal serial clock f_{SC} is selected the one-divided output of the pre-scaler by the mask option.

■ AC CHARACTERISTICS 2 SERIAL INTERFACE TIMING CHART

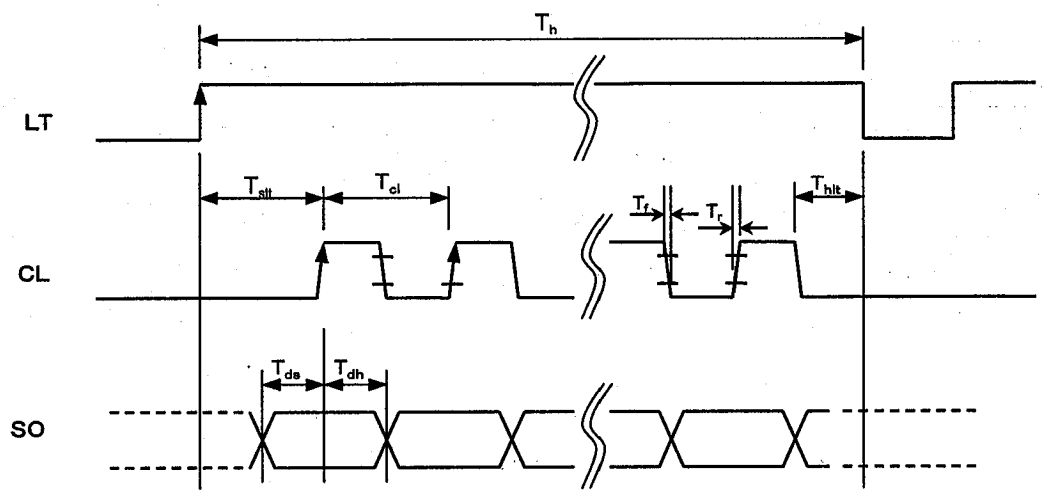


■ ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS 3 (V_{DD}=2.7~5.5V, V_{SS}=0V, Ta=-40~85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
CL Shift Clock Period	T_{Cl}			$12/f_{OSC}$		μsec
CL Rise Time	T_r	Load Capacity :100pF			0.5	μsec
CL Fall Time	T_f	Load Capacity :100pF			0.5	μsec
SIO Setup Time to CL ↑	T_{ds}	f_{osc}=4MHz	1.0			μsec
SIO Hold Time to CL ↑	T_{dh}	f_{osc}=4MHz	1.0			μsec
LT Setup Time	T_{slt}	f_{osc}=4MHz	2.5			μsec
LT Hold Time	T_{hlt}	f_{osc}=4MHz	1.0			μsec
Data Transfer Time	T_b		$3378/f_{OSC}$		$3390/f_{OSC}$	sec

■ AC CHARACTERISTICS 3 EXTENSION DRIVER INTERFACE TIMING CHART



■ MASK OPTION

1) INPUT OUTPUT Terminal Selection

All of input-output terminals select a type for each port from the following table1 and table2 by mask option.

[CIRCUIT TYPE TABLE 1]

Port Name	Circuit Type						
	Input Output Terminals *1			Another Functions		Others	
	Port of Input	Port of Output	Programmable Input/Output				
PA0 /SEG24	ICP IC	OC		SEG	LCD Driver Output		
PA1 /SEG25 / LT	ICP IC	OC		SEG LT	LCD Driver Output LCD Extension Driver Serial Data Latch Output		
PA2 /SEG26 / SYNC	ICP IC	OC		SEG SYN	LCD Driver Output LCD Extension Driver Synchronizing Signal output		
PA3 /SEG27 / MCK	ICP IC	OC		SEG MCK	LCD Driver Output LCD Extension Driver Master Clock Output		
PB0 /SEG28		ONP ON		SEG	LCD Driver Output		
PB1 /SEG29		ONP ON		SEG	LCD Driver Output		
PB2 /SEG30		ONP ON		SEG	LCD Driver Output		
PB3 /SEG31		ONP ON		SEG	LCD Driver Output		
PC0 / SO		OC		SO	LCD Extension Driver Serial Data Output		
PC1 / CL		OC		CL	LCD Extension Driver Shift Clock Output		
PD0			IOP IO	RSP RS	Re-start Signal Input		
PE0 / EXTI	ISP IS			IIP II	External Interrupt Function	R F	Rising Edge Detection Falling Edge Detection
PE1	ISP IS						
PE2	ISP IS						

Note) Symbols described in this table is used at Mask Option Generator Software.

*1) Refer ■ INPUT OUTPUT TERMINAL TYPES.

[CIRCUIT TYPE TABLE 2]

Port Name	Circuit Type						
	Input Output Terminal *1			Another Function		Others	
	Port of Input	Port of Output	Programmable Input/Output				
PF0	ICP IC						
PF1	ICP IC						
PF2	ICP IC						
PF3	ICP IC						
PG0			IOP IO				
PG1			IOP IO				
PG2			IOP IO				
PG3			IOP IO				
PH0	ICP IC	OC					
PH1	ICP IC	OC					
SCL				SCP SC	Serial Clock Input/Output		
SIO				SDP SD	Serial Data Input/Output	MSB LSB	MSB First LSB First

Note）Symbols described in this table is used at Mask Option Generator Software.

*1）Refer ■ INPUT OUTPUT TERMINAL TYPES.

② Restart Signal Input Selection

PD0 terminal can be used as MCU restarting signal input terminal from standby. When this terminal becomes "High" from "Low" on standby, the MCU is cancelled standby mode and restarts running program at stopping address. This function can be selected by mask option.

③ Edge Detector Selection of External Interrupt

PE0 has a external interrupt function. The polarity of edge, rising as "low to high" or falling as "high to low", is selected by the mask option.

④ The data order (MSB, LSB) of the Serial Interface

The data order of the Serial Interface can select either MSB or LSB first by the mask option.

⑤ The count clocks of Timer1 and Timer2 , the internal shift clock of the serial interface.

The frequency of these clock can be selected by the mask option. There are twelve ways of selecting the frequency that is based on the inverse of 1-instruction executing period time (6 / f_{osc}).

Function	Pre-scaler Divider											
	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024	1/2048	1/4096
Timer 1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Timer 2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Serial Interface	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note) The shift clock of the serial interface can select the internal or external clock by the program.

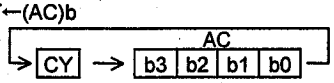
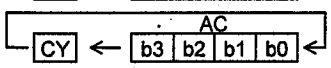
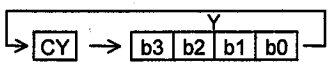
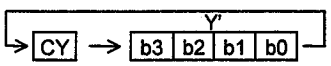
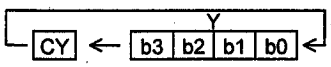
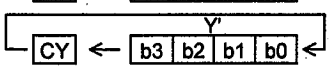
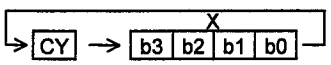
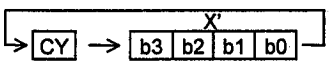
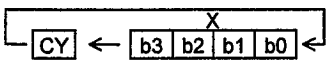
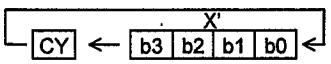
⑥ Frame frequency of LCD Driver

The frame frequency is selected as shown in follow using the clock from the pre-scaler by mask option which is based on the inverse of 1-instruction executing period time (6 / f_{osc}) .

Function	Pre-scaler Divider													
	1/64	1/128	1/192	1/256	1/384	1/512	1/768	1/1024	1/1536	1/2048	1/3072	1/4096	1/6144	1/8192
Frame Frequency	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

■ MNEMONIC LIST

	Mnemonic	Operation code	Function	Status	Cycle	Memo
Data Transference	TAY	04	Y←AC	1	1	RPC=0
			Y'←AC	1	1	RPC=1
	TYA	14	AC←Y	1	1	RPC=0
			AC←Y'	1	1	RPC=1
	XAX	1B	AC↔X	1	1	RPC=0
			AC↔X'	1	1	RPC=1
	TAP	26	PH(Y')←AC	1	1	
	TPA	16	AC←PH(Y')	1	1	
	TAPICY	17	PH(Y')←AC, Y←Y+1	*	1	
	TAPDCY	27	PH(Y')←AC, Y←Y-1	*	1	
	TMA	0D	AC←M(X,Y)	1	1	
	TAM	1D	M(X,Y)←AC	1	1	
	TAMICY	0A	M(X,Y)←AC, Y←Y+1	*	1	
	TAMDCY	1A	M(X,Y)←AC, Y←Y-1	*	1	
	TMY	05	Y←M(X,Y)	1	1	RPC=0
			Y'←M(X,Y)	1	1	RPC=1
	XMA	0B	AC↔M(X,Y)	1	1	
	TPMICY	03	M(X,Y)←PH(Y'), Y←Y+1	*	1	
	TMPICY	13	PH(Y')←M(X,Y), Y←Y+1	*	1	
	TRM	23	M(X,Y)←ROM(PHY13,X',AC)	1	2	Y= an odd number:ROM of 4bit hi-data Y= an even number:ROM of 4bit low-data
	CLA	80	AC←0	1	1	
	LDI A,#K	80~8F	AC←#K	1	1	#K=0~15
	LDI Y,#K	90~9F	Y←#K	1	1	RPC=0, #K=0~15
			Y'←#K	1	1	RPC=1, #K=0~15
	LDI X,#K	A0~AF	X←#K	1	1	RPC=0, #K=0~15
			X'←#K	1	1	RPC=1, #K=0~15
Calculationg	ADD A,M	0E	AC←AC+M(X,Y)	*	1	
	INC A	71	AC←AC+1	*	1	
	DEC A	7F	AC←AC-1	*	1	
	ADD	70~7F	AC←AC+#K	*	1	#K=0~15
	A,#K	0F	AC←AC∧M(X,Y)	*	1	
	AND A,M	2E	AC< >M(X,Y)	*	1	
	CMP A,M	B0~BF	Y< >#K	*	1	#K=0~15
	CMP Y,#K	08	Y←Y+1	*	1	RPC=0
	INC Y		Y'←Y'+1	*	1	RPC=1
		18	Y←Y-1	*	1	RPC=0
	DEC Y		Y'←Y'-1	*	1	RPC=1
		09	AC←M(X,Y)+1	*	1	
	INC M	19	AC←M(X,Y)-1	*	1	
	DEC M	01	Y< >AC	*	1	
	YNEA	1F	AC←AC∨M(X,Y)	*	1	
	OR A,M	2F	AC←AC⊕M(X,Y)	*	1	
	XOR A,M	2D	AC←0-AC	1	1	
	NEG	1E	AC←M(X,Y)-AC	*	1	
	SUB A,M	40~4F	AC←AC∧#K	*	1	#K=0~15
	AND	50~5F	AC←AC∨#K	*	1	#K=0~15
	A,#K					
	OR A,#K					

	Mnemonic	Operation code	Function	Status	Cycle	Memo
Branch	JPL addr	68~6F	ST=1:PC←addr, ST=0 : No branch	1	2	2bite Mnemonic
	JMP addr	C0~FF	ST=1:PC←addr, ST=0 : No branch	1	1	
	CALL addr	60~67	ST=1:(SP)←PC+2, SP←SP+1, PC←addr ST=0 : No branch	1	2	2bite Mnemonic
	RET	2B	PC←(SP), SP←SP-1	1	1	
	RETI	2C	PC←(SP), AC←(SP), SP←SP-1 X←(SP), X'←(SP), Y←(SP), Y'←(SP) RPC←(SP), ST←(SP)	*	1	
Bit Operation	SBIT b	30~33	M(X,Y)b←1	1	1	b=0~3
	RBIT b	34~37	M(X,Y)b←0	1	1	b=0~3
	TBIT b	38~3B	ST←M(X,Y)b	*	1	b=0~3
	TBA b	3C~3F	ST←(AC)b	*	1	b=0~3
	RAR	21		*	1	
	RAL	22		*	1	
	RYR	24		*	1	RPC=0
				*	1	RPC=1
	RYL	25		*	1	RPC=0
				*	1	RPC=1
	RXR	28		*	1	RPC=0
				*	1	RPC=1
	RXL	29		*	1	RPC=0
				*	1	RPC=1
	SEC	0C	CY←1	1	1	
	CLC	1C	CY←0	0	1	
	SRPC	10	RPC←1	1	1	
	RRPC	20	RPC←0	1	1	
Special	NOP	00	No Operation	1	1	
	HLT	07	CPU Halted	1	1	
	MDT	06	Memory Dump Test	-	-	

※

←	: Transfer direction	AC	: Accumulator	SP	: Stack pointer
∧	: AND	X	: X register	RPC	: RPC flag
∨	: OR	X'	: X' register	CY	: Carry flag
⊕	: Exclusive OR	Y	: Y register	ST	: Status flag
+	: Add	Y'	: Y' register	#K	: Immediate data
−	: Subtraction	PH	: Peripheral register	addr	: Blanch address
<>	: Comparison	M	: Data memory	( )	: A content of register or memory Pointed by the address indicated in ( ).
		ROM	: Program memory		
		PC	: Program counter	b	: Bit position

※Status description

1: After the command execution , ST-flag is always set "1".
0: After the command execution , ST-flag is always set "0".
*: Status is changed by the result of command execution.

MEMO