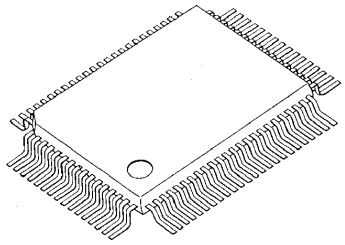
PRELIMINARY

Digital Audio Processor

■ GENERAL DESCRIPTION

The **NJU25030** is a Digital Audio Processor, performing Passive Matrix TruSurround™ 3D Surround and TruBass™ with fully digital processing utilizing the DSP(Digital Signal Processor) technology. Also, because Passive Matrix TruSurround is based on the proprietary SRS 3D Sound technology, when a standard stereo source is fed into the **NJU25030**, the resulting output is an expanded source image. TruBass provides deep, rich bass to small speaker systems without a subwoofer. In addition to the 3D Surround, the **NJU25030** performs BBE sound enhancement process which regenerates high definitive and nearly real clearness sound.

■PACKAGE OUTLINE



NJU25030

■ FEATURES

- ●TruSurround 3D Surround Audio Processing
  360 ° surround from only two speakers
- ●BBE Sound Enhancement
- ●TruBass Bass System Punch/Bass control
- ●Input level Trimmer
- ●Preset surround mode.
- ●Package Outline QFP80

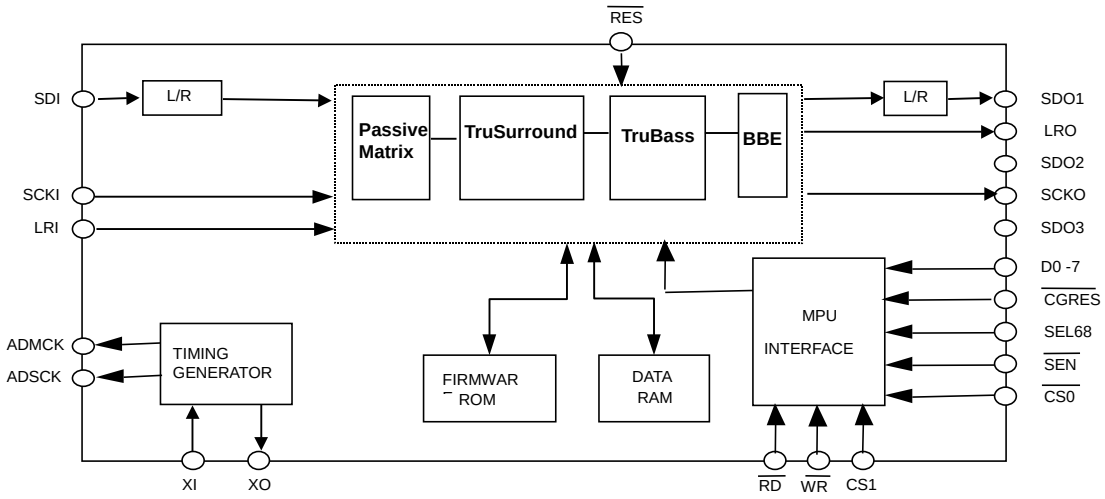


Fig1, NJU25030 BLOCK DIAGRAM

■ PIN CONFIGURATION

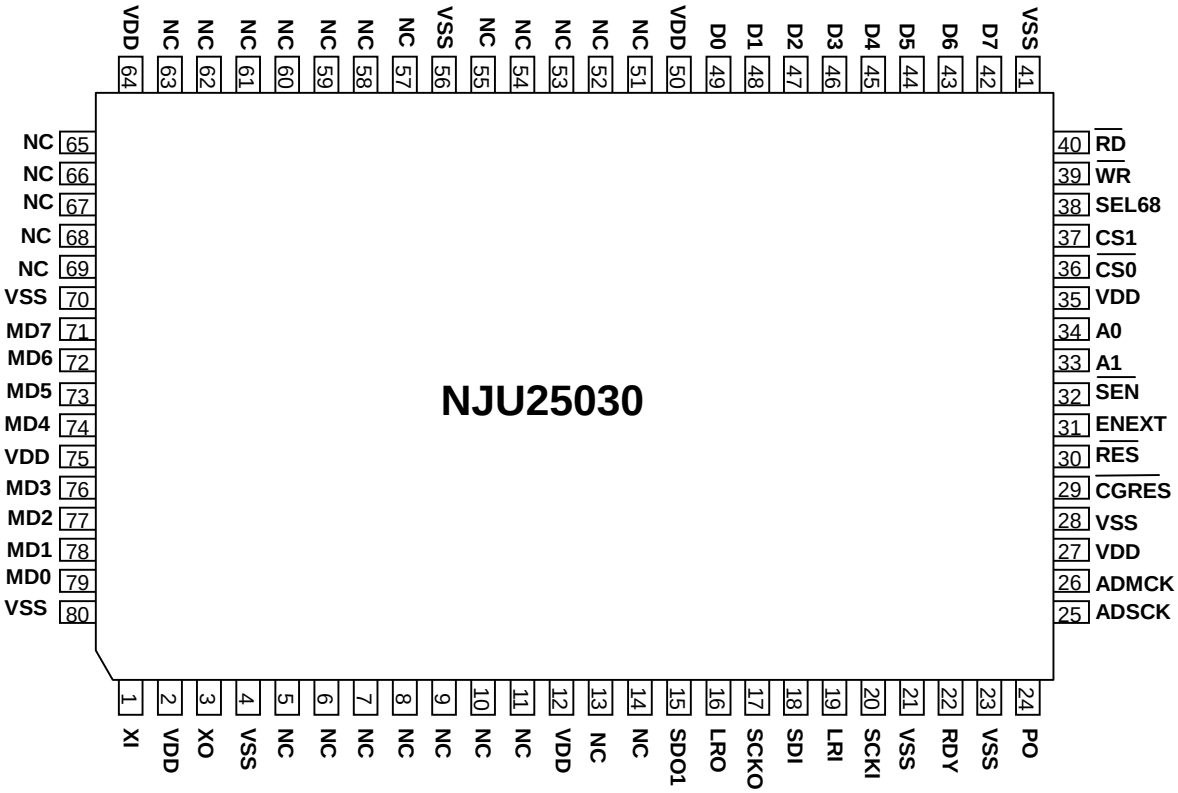


Fig2, NJU25030 Pin Configuration

■ PIN DESCRIPTION

No	Symbol	I/O	Function	No	Symbol	I/O	Function
1	XI	I	Crystal/External clock input	41	VSS	I	Ground
2	VDD	I	Power supply terminal : +5V	42	D7	I/O	MPU data, parallel input(MSB) ✳2
3	XO	O	Crystal	43	D6	I/O	MPU data, parallel input ✳2
4	VSS	I	Ground	44	D5	I/O	MPU data, parallel input ✳2
5	NC ✳1		No connect	45	D4	I/O	MPU data, parallel input ✳2
6	NC		No connect	46	D3	I/O	MPU data, parallel input ✳2
7	NC		No connect	47	D2	I/O	MPU data, parallel input ✳2
8	NC		No connect	48	D1	I/O	MPU data, parallel input ✳2
9	NC		No connect	49	D0	I/O	MPU data, parallel input(LSB), Serial data input($\overline{SEN}$=0)
10	NC		No connect	50	VDD	I	Power supply terminal : 5V
11	NC		No connect	51	NC		No connect
12	VDD	I	Power supply terminal : 5V	52	NC		No connect
13	NC		No connect	53	NC		No connect
14	NC		No connect	54	NC		No connect
15	SDO1	O	Digital audio serial data out	55	NC		No connect
16	LRO	O	Output left/right frame clock	56	VSS	I	Ground
17	SCKO	O	Output digital audio serial clock	57	NC		No connect
18	SDI	I	Input digital audio serial data	58	NC		No connect
19	LRI	I/O	Input left/right frame clock	59	NC		No connect
20	SCKI	I/O	Input digital audio serial clock	60	NC		No connect
21	VSS	I	Ground	61	NC		No connect
22	RDY	I	Test pin, high for normal operation	62	NC		No connect
23	VSS	I	Ground	63	NC		No connect
24	PO	O	Test pin normally open	64	VDD	I	Power supply terminal:+5V
25	ADSCK	O	32Fs/64Fs serial clock for A/D, D/A converters (default 32Fs)	65	NC		No connect
26	ADMCK	O	384Fs/256Fs serial clock for A/D, D/A converters (default 384Fs)	66	NC		No connect
27	VDD	I	Power supply terminal : +5V	67	NC		No connect
28	VSS	I	Ground	68	NC		No connect
29	$\overline{CGRES}$	I	Test pin, normally high	69	NC		No connect
30	$\overline{RES}$	I	Reset, must be held low for at least two clock cycles after power on	70	VSS	I	Ground
31	ENEXT	I	Test pin, normally low	71	MD7	I	BBE On/Off control ✳2
32	$\overline{SEN}$	I	MPU serial interface enable. Serial = L, parallel = H	72	MD6	I	TruBass On/Off control (+12dB) ✳2
33	A1	I	Test pin, Low for normal operation	73	MD5	I	TruSurround On/Off control ✳2
34	A0	I	Test pin, Low for normal operation	74	MD4	I	TruBass On/Off control (+6dB) ✳2
35	VDD	I	Power supply terminal : +5V	75	VDD	I	Power supply terminal:+5V
36	$\overline{CS0}$	I	Chip select. MPU interface enabled when $\overline{CS0}$=0 and CS1=1	76	MD3	I	Port control3 (not assigned) ✳2
37	CS1	I	Chip select. MPU interface enabled when $\overline{CS0}$=0 and CS1=1	77	MD2	I	Port control2 (not assigned) ✳2
38	SEL68	I	MPU interface mode:68K=H, Z80=L	78	MD1	I	Port control1 (not assigned) ✳2
39	$\overline{WR}$	I	Write Strobe(Z80),Write Enable(68K)	79	MD0	I	Port On/Off control
40	$\overline{RD}$	I	Write Strobe(68K)	80	VSS	I	Ground

✳1 : NC pin must be left open.

✳2 : D1- D7(42 – 48pin), MD7 –MD1(71 – 74,76-78pin) should be connected to Vss with pull down resistor respectively, whenever the port is disable.

■ ABSOLUTE MAXIMUM RATINGS(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply Voltage(Ta=25°C)	V_{DD}	-0.3~7	V
Input, Output Pin Voltage(Ta=25°C)	V_X	-0.3~V_{DD}+0.3	V
Operating Temperature	T_{CASE}	-20~70	°C
Storage Temperature	T_{stg}	-55~125	°C

1. Absolute maximum ratings are stress ratings only, and functional operation beyond these limits is not guaranteed. Stress beyond the maximum ratings may affect device reliability or cause permanent damage to the device.

■ ELECTRICAL CHARACTERISTICS (Ta=-20°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		4.75		5.25	V
Operating Current	I_{DD}	f_{OSC}=25MHz		90	125	mA
High Level Input Voltage	V_{IH}		0.80V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		V_{SS}		0.10 V_{DD}	V
High Level Input Current	I_{IH}	V_{IN} =V_{DD}			10	µA
Low Level Input Current	I_{IL}	V_{IN} =V_{DD}			10	µA
High Level Output Voltage	V_{OH}	I_{OH}=2mA	V_{DD}-1.0			V
Low Level Output Voltage	V_{OL}	I_{OH}=2mA			0.5	V
Input Capacitance	C_{IN}			10	20	PF
Clock Frequency	f_{OSC}			25		MHz
Ext. System Clock Duty Cycle	r_{EC}		45		55	%

1. For operation with 37MHz clock frequency, contact factory.
2. Clock frequency is 768Fs. (Fs=32Khz)

■ Functional Description

NJU25030 Function Block Diagram

NJU25030 are consisted by Passive Matrix Tru Surround, TruBass ,and BBE function.

Each function has Bypass mode enable to control independently by Micro controller interface.

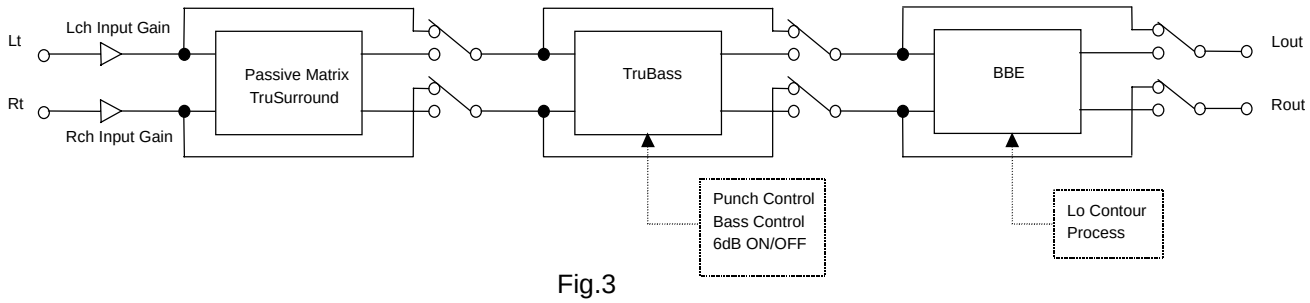


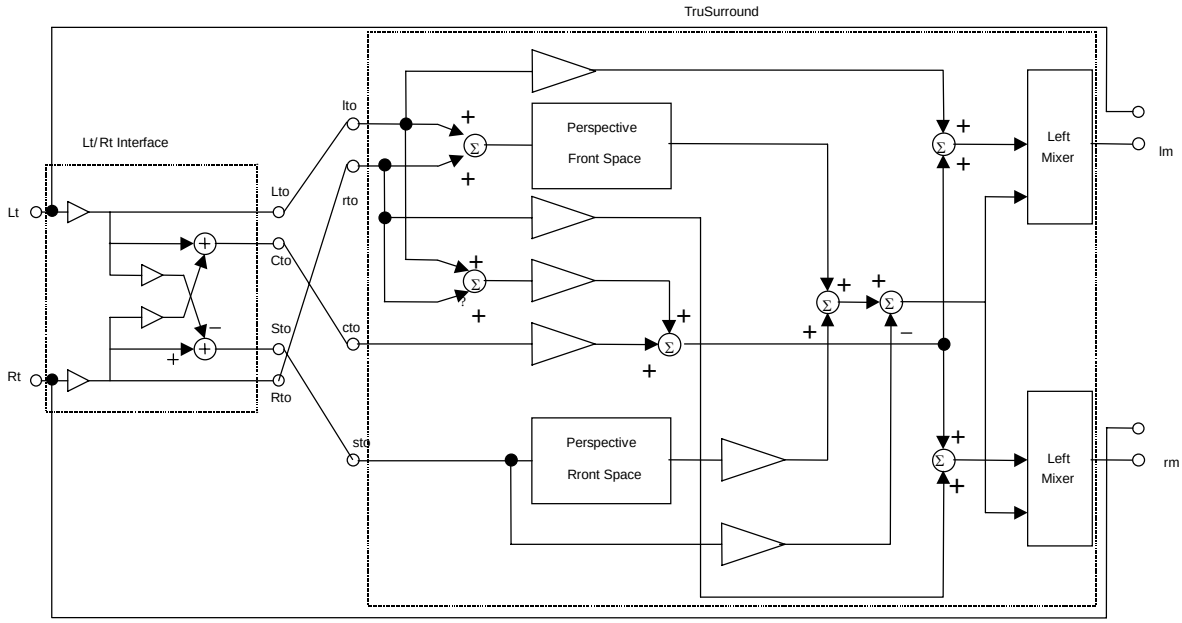
Fig.3

● Passive Matrix TruSurround

Surround information is extracted by the Lt/Rt interface processing in the NJU25030.Head Related Transfer Function (HRTFs), based on the natural characteristics of the human hearing system, are used on both Front and Rear Surround channels to synthesize virtual surround speakers to the side and rear of listener.

The Front HRTFs have frequency tailoring of the difference signals (L-R) to extend the sound image past the physical boundaries of the actual speakers. A different set of frequency coefficients are applied to the Rear HRTFs that have a much greater peak and valley differences and center frequencies.

These are chosen to cause the rear channels to virtualize behind the listener. The virtualized surround is then mixed into the Left and Right output.



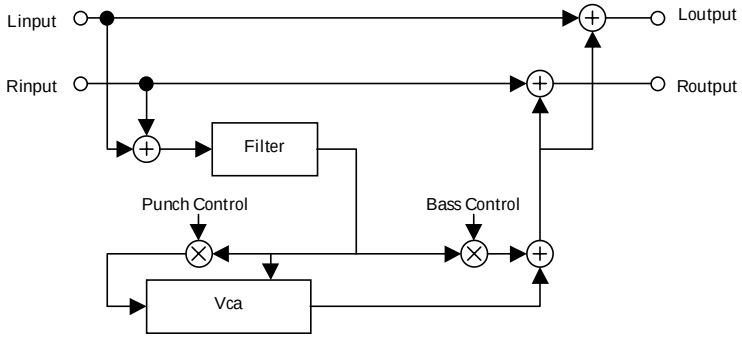
Passive MatrixTruSurround

Fig.4

● **TruBass**

SRS TruBass is a remarkable new technology provide deep bass to small speaker system without limited by low frequency characteristics of speaker. Furthermore, SRS Tru Bass technology provides more rich bass sound with subwoofer system.

NJU25030 enable to adjust the level of BASS and PUCH parameter, and enable to select the speaker size. Furthermore, NJU25030 has +6dB switch for gain adjustment.
Therefore, It is easy to optimize the bass sound for various speaker system.

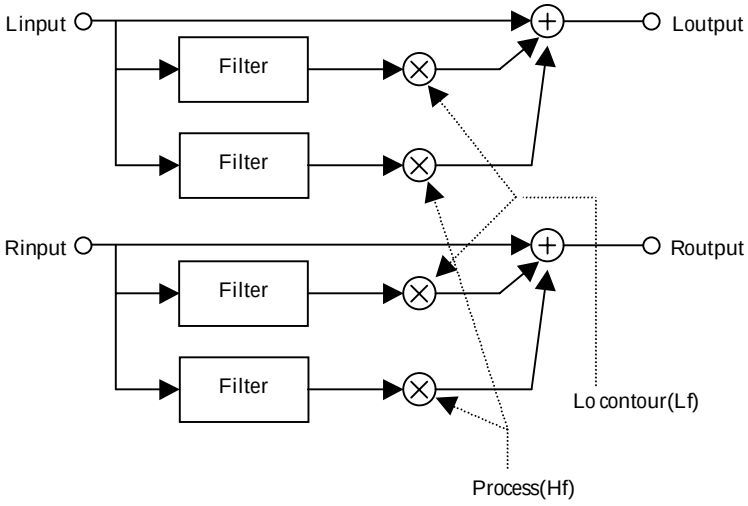


Simple Block Diagram for TruBass

Fig.5

● **BBE**

The BBE technology brings to the listener's ear a more complete and accurate reproduction of the original performance, The BBE is used to recover the clarity of sound compensating for the idiosyncrasy which inherently occurs in speakers and headphones.



Simple Block Diagram for BBE

Fig.6

■ SERIAL DATA FORMATS

The I^2S mode is supported for interfacing an A/D and two D/As to the digital audio interface.
The I^2S mode is similar to Left Justified mode, except that the data is delayed one SCLK period and the sense of LRI and LRO is inverted (see Figure 7). In I^2S mode, LRI and LRO must be low for left channel data and high for right channel data, the opposite of other modes. The polarity of LRI and LRO can be inverted independently in any mode by the use of the LRI and LRO.

Normally, the serial data bits generated by a source change on the falling edge of the serial clock so that they can be easily clocked into a shift register on the rising clock edge. Considering an A/D as the source and the **NJU25030** as a destination, the default setting is to clock the serial data input, SDI, in on the rising edge of SCKI. This can be changed to clock data in on the falling edge using the SCKI bit in the System Download Command.
For the output serial data, the **NJU25030** is considered the source and the D/As are considered the destination. The default interface setting is for data to be clocked out of SDO on the falling edge of SCKO so that the D/A clocks data in on the rising edge. This can be changed independently of the input and interface mode using the SCKO bit in the System Download Command.

The MS (Master/Slave) bit in the fourth System State Download Command byte selects either Master mode or Slave mode. Master mode (MS = 0) is defined such that SCKO and LRO are generated from an internal divider derived from the 768Fs DSP clock (XI).
In Slave mode (MS = 1) SCKO and LRO are the same as SCKI and LRI on the input.
This mode should be used for asynchronous data rates, such as data from an S/PDIF receiver connected to the Digital Output from a laser disc player. The output D/A's must be synchronized to the input data by using the low jitter, recovered clock from the S/PDIF receiver to the D/A master clock. When an A/D is used, its master clock should be synchronous to the **NJU25030** using ADMCK at 256Fs or 384Fs. In this case either Master mode or Slave mode will work. The default setting is Master mode (MS = 0).

In I^2S mode, Master and Slave modes have slightly different meanings. Relative to the **NJU25030**, Slave mode (MS = 1) is defined as LRI and SCKI being inputs from the A/D. This means that the A/D must be in Master mode with L/R and SCLK outputs. Conversely, when the **NJU25030** is in Master mode (MS = 0), LRI and SCKI are outputs that drive the L/R and SCLK inputs of an A/D operating in slave mode. SCKO and LRO to the D/As are always outputs. The D/A converters can run only in Slave mode, receiving both the L/R and SCLK from the **NJU25030**. LRO and SCKO are derived from the 768Fs DSP clock. When slave mode is selected, LRO and SCKO are generated by the LRI and SCKI inputs. Slave mode should be used for asynchronous audio data.

When using a codec in slave mode and operating the **NJU25030** in I^2S Master mode, the LRO signal must be used to drive the L/R input of the codec. Although LRI is not used, it must be programmed with the opposite polarity. This is the default setting upon initialization after reset (LRI=0, LRO=1) for typical 2-channel applications. For more details, refer to the Demonstration Board User's Guide. In all other modes or when using separate A/D and D/A converters that use both LRI and LRO, respectively, the polarity should be the same for LRI and LRO. In Left Justified mode, only Slave mode (MS = 0) is allowed. The A/D is required to be in Master mode and supplies LRI and SCKI to the **NJU25030**. LRO and SCKO are generated from LRI and SCKI inputs.

The I^2S data format, the serial clock frequency for SCKI and SCKO is selected using ADSCK in the System Download Command: either 32Fs (32-bit clocks per sample) or 64Fs (64-bit clocks per sample). SCKI and SCKO must be the same frequency. This clock is generated internally for the SCKI and SCKO in Master mode, but is also available as an output on the ADSCK pin. It is derived from the 768Fs Input Clock to the **NJU25030**.

If SCKI and SCKO are selected to be 32Fs, the data length must be set to 16-bits (BIO = 0) because a stereo pair of 16-bit channels needs all 32 clocks per sample. In this case, both Left and Right Justified modes look exactly the same (see Figure 8), and either mode setting will work. In I^2S mode, the data bits appear shifted by one SCLK and the L/R is inverted (see Figure 9).

An output clock, ADMCK, is derived from the **NJU25030** 768Fs Input Clock for use as an A/D or D/A master clock. ADMCK is set to 256Fs or 384Fs using the ADMCK bit in the System Download Command.

■ **SERIAL DATA INPUT TIMING PARAMETER (V_{DD}=5V±5%, Ta=-20 to +70°C,f_{CLK}=25MHz)**

Parameter	Symbol	Min.	Max.	Unit
SCKI Period		160		
L Pulse Width	t_{SIL}	80		ns
R Pulse Width	t_{SIH}	80		
SCKI to LRI Time	t_{SLI}	50		ns
LRI to SCKI Time	t_{LSI}	75		ns
Data Setup Time	t_{DS}	10		ns
Data Hold Time	t_{DH}	10		ns

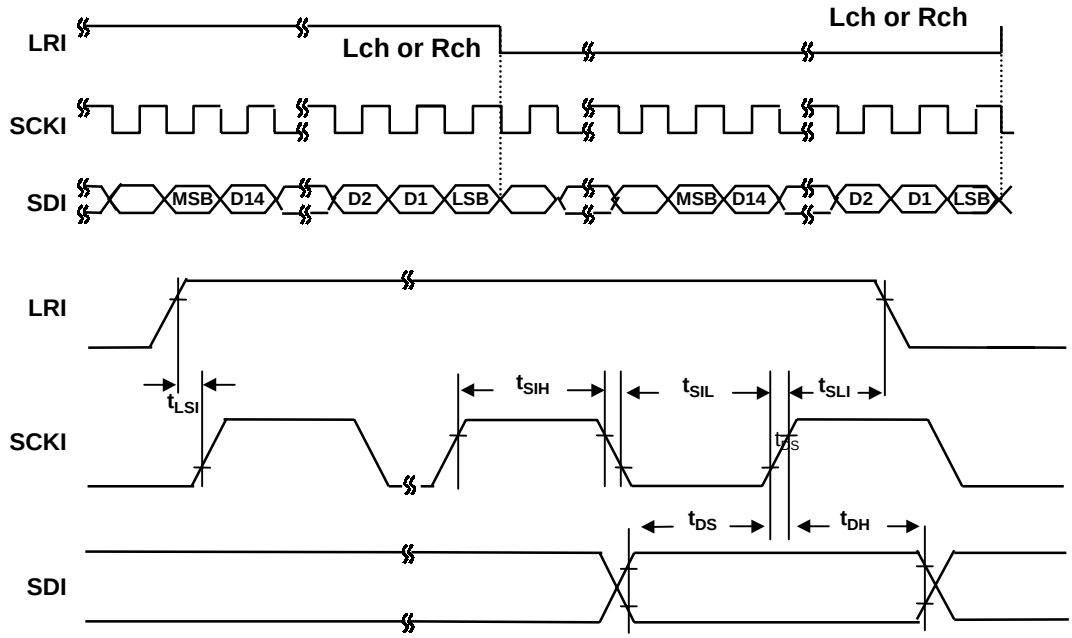


Fig7, Serial Data Input Timing

■ **SERIAL DATA OUPUT TIMING PARAMETER**
(V_{DD}=5V±5%, Ta=-20 to +70°C,f_{CLK}=25MHz, CL:LRO, SCKO, SDO=5pF)

Parameter	Symbol	Min.	Max.	Unit
SCKO Period		160	-	
L Pulse Width	t_{SOL}	80	-	ns
R Pulse Width	t_{SOH}	80	-	
SCKO to LRO Time	t_{SLO}	-	5	ns
Data Output Delay	t_{DOH}	-	5	Ns

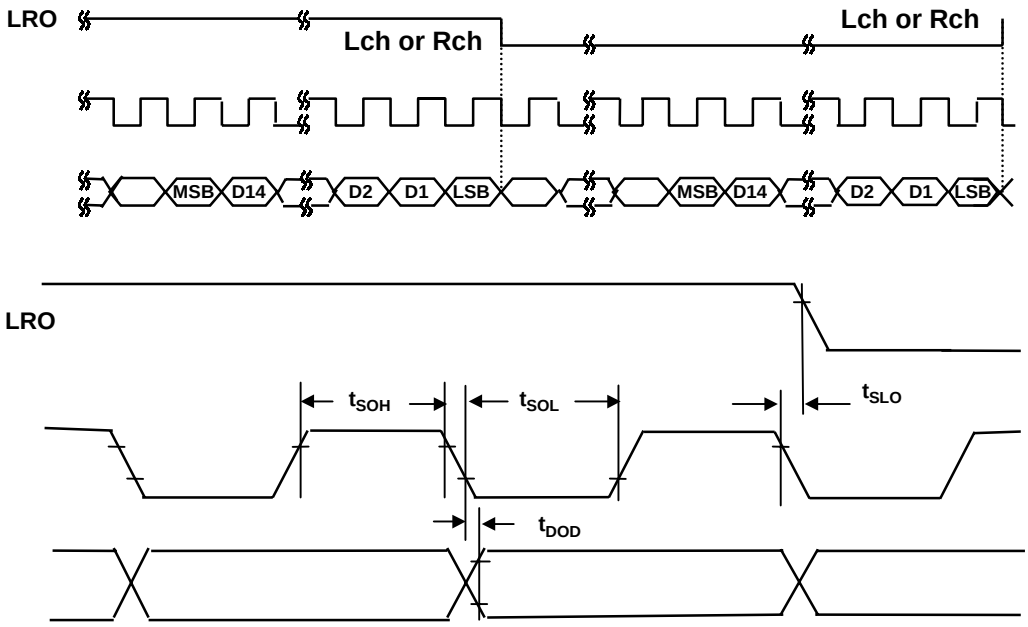


Fig8, Serial Data Output Timing

■ FUNCTIONAL TIMING DIAGRAMS

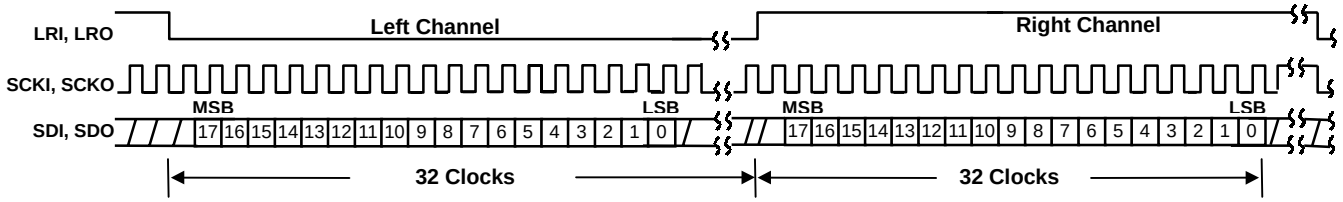


Fig9, I²S Data Format, ADSCK=64Fs, 18bit Data

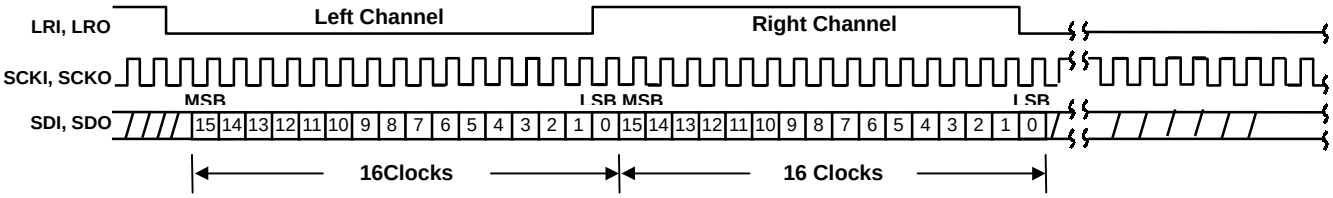


Fig10, I²S Data Formats, ADSCK=32Fs, 16bit Data

■ MICROCONTROLLER INTERFACE

There are two microprocessor interface modes that can be used to work with a variety of micro controllers, including 68000, Z80, or 8031 type interfaces. The primary difference between modes is that data is latched on the rising edge of WR in Z80 mode, while data is latched on the falling edge of RD in 68K mode. For Z80 it is set low. The interface may be configured for 8-bit serial data by a logic low on SEN, and clocking the data in using WR or RD as the serial bit clock, depending on the mode, Z80 (rising edge) or 68K (falling edge), respectively.

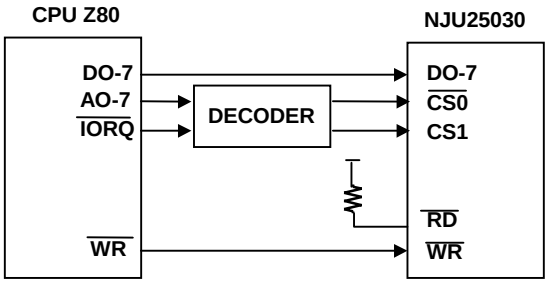


Fig11, Z80 Interface

■ SERIAL INTERFACE

In serial interface mode (SEN = 0), D0 is used for the serial data input. Two types of interface modes are supported. In Z80 mode (SEL68 Low) WR is used as a serial bit clock. In 68K mode (SEL68 High), RD is used to clock the serial data. Data is clocked in 8 bits at a time with a maximum data rate of 1 MHz. As in Parallel mode above, after each byte (8 serial data bits), a wait time of 1 ms must occur before the next byte or command is sent.

■ SERIAL INTERFACE—Z80 MODE

When using a microprocessor with a Z80 type interface, writing serial data to the **NJU25030** is done by clocking the data in on rising edges of the WR, with RD held High (SEL68 = 0). The idle state of WR must be High when CS0 and CS1 become active and return to inactive states. The recommended sequence is:

1. Set SEN = 0
2. Assert chip selects, ($\overline{CS0}$ = 0 and CS1 = 1).
3. Set RD High.
4. Clock in serial data with WR (rising edge).
5. Deactivate chip selects.
6. Wait 1 ms before sending next byte or command.

■ **Z80 INTERFACE TIMING PARAMETERS (V_{DD}=5V±5%, Ta=-20 to +70°C,f_{CLK}=25MHz)**

Parameter	Symbol	Min.	Max.	Unit
Address Setup Time	t_{AS8}	100	-	
Address Hold Time	t_{AH8}	100	-	
System Cycle Time	t_{CYC8}	1,000	-	
Read/Write Pulse Width	t_{CC8}	100	-	
Write Data Setup Time	t_{DS8}	10	-	ns
Write Data Hold Time	t_{DH8}	10	-	ns

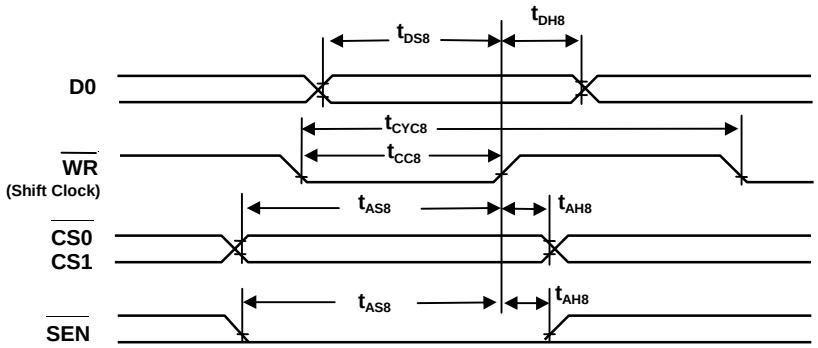


Fig13, Z80 Serial Interface Timing(SEL68 Low)

■ **Port Control**

NJU25030 also enable to control the sound mode by I/O port control.
The ports are assaigned pin 71,72,73,74,and 79. To control the sound mode by port , MD0 shoud be set to Port(High).
The serial control from microcontroller disable to control once port control is active.
The setting of port control is

TruSurround	6dB :MD5
TruBass	6dB :MD6, 12dB(6dB+6dBAmp):MD4
BBE	9dB : MD7

However, As Level of TruBass is multiplex coefficient of internal DSP processing. It may not reflect to output gain directly.
In case of control by serial interface, These MD0 to MD7 should be connected to Vss with proper resistor.

■ **Command Description (* :Default Setting)**

After power is applied and a hardware reset is generated on the RES pin (pin 30), three bytes must be sent from the microprocessor that defines the hardware settings of the NJU25030. This data controls the digital audio interface format, the Clock Generator outputs. This is the only multi-byte command. All the others are single byte and take effect immediately without interruption of the audio processing. The other commands contain a non- zero “op code” and all data bits in one byte. When the DSP receives the first byte of the Configuration Command, which is all zeroes, the audio stops and the DSP waits for two more bytes. These hardware settings are intended to be set once, and not changed unless the chip is reset again.

Byte #1 Configuration Command op code, 00h.
Byte #2 Serial Data Setting
Byte #3 Reserved
Byte #4 Clock Outputs

Command	Byte	Bit								Remarks
		7	6	5	4	3	2	1	0	
Configuration	4	0	0	0	0	0	0	0	0	Initial Setting
		0	0	0	0	0	BIO	FMT1	FMT0	
		0	0	0	1	1	0	0	1	
		1	0	LRI	0	0	MS	ADSCK	ADMCK	
Sampling Frequency	1	0	0	0	0	0	0	FS1	FS0	32kHz
Operation	1	0	0	0	1	0	BBE	TB	TS	BBE,TruBass, TruSurround Mode Selection
TruBass(Size)	1	0	0	0	1	0	6dB S.W.	SIZE1	SIZE0	TruBass Speker Size 6dB SW On/Off
TruBass	1	0	0	1	CNT	LEV3	LEV2	LEV1	LEV0	TruBass Punch/Bass Control
BBE	1	0	1	0	CNT	LEV3	LEV2	LEV1	LEV0	BBE Process/LoCont
Input Trimmer	1	1	0	CH	TR4	TR3	TR2	TR1	TR0	Input Trimmer

● Configuration Commands (4bytes)

1st byte

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	…0x00

2nd byte

7	6	5	4	3	2	1	0
0	0	0	0	0	BIO	FMT1	FMT0

0	0	Reserved	Audio Data Interface Mode
0	1	I2S *	
1	0	Reserved	
1	1	Reserved	

0	16bit	Audio Data Width
1	18bit *	

Reserved

3rd byte

7	6	5	4	3	2	1	0	
0	0	0	1	1	0	0	1	… 0x19

Reserved

4th byte

7	6	5	4	3	2	1	0
1	0	LRI	0	0	MS	ADSCK	ADMCK

- ADMCK: 0 = 384Fs *, 1 = 256Fs — AD-DA MCLK
- ADSCK: 0 = 32Fs, 1 = 64Fs * — AD-DA SCLK
- MS: 0 = Master * — Audio Data Interface Mode; 1 = Slave
- 0 = Reserved
- 0 = ↑ SCKI Data latches on rising edge; Reserved
- LRI: 0 = Master Mode* — Input L/R Clock; 1 = Slave Mode
- 0 = ↓ SCKO Data latches on falling edge; Reserved
- 1 = Output L/R Clock; Reserved

- Sampling Frequency

7	6	5	4	3	2	1	0
0	0	0	0	0	0	Fs1	Fs0

Fs1	Fs0	
0	1	32kHz

- Operation

7	6	5	4	3	2	1	0
0	0	0	1	0	BBE	TB	TS

BBE	TB	TS	
0	0	0	All OFF *
0	0	1	TruSurround
0	1	0	TruBass
0	1	1	TruSurround + TruBass
1	0	0	BBE
1	0	1	TruSurroumd + BBE
1	1	0	TruBass + BBE
1	1	1	TruSurround + Trubass + BBE

(Default Setting)

Tru Surround 6dB
TruBass Size:Medium, 6dBSW Off, Punch/Bass –6dB
BBE LoContour/Process 9dB

TruBass(Size)

7	6	5	4	3	2	1	0
0	0	0	1	1	6dB S.W.	SIZE1	SIZE2

SIZE1	SIZE2	
0	0	Medium *
0	1	Small
1	0	Large

6dB S.W.	
0	Normal (0dB) *
1	6dB ON

Function Parameters

TruBass

7	6	5	4	3	2	1	0
0	0	1	CNT	LEV3	LEV2	LEV1	LEV0

LEV3	LEV2	LEV1	LEV0	
0	0	0	0	0dB
0	0	0	1	-2dB
0	0	1	0	-4dB
0	0	1	1	-6dB*
.....				
1	1	0	1	-26dB
1	1	1	0	-28dB
1	1	1	1	MUTE

CNT	
0	Punch
1	Bass

BBE

7	6	5	4	3	2	1	0
0	1	0	CNT	LEV3	LEV2	LEV1	LEV0

LEV3	LEV2	LEV1	LEV0	
0	0	0	0	0dB
0	0	0	1	1dB
0	0	1	0	2dB
.....				
1	0	0	1	9dB*
.....				
1	1	1	0	14dB
1	1	1	1	15dB

CNT	
0	LoContour
1	Process

Input Trimer

7	6	5	4	3	2	1	0	
1	0	CH	TR4	TR3	TR2	TR1	TR0	
			0	0	0	0	0	0dB *
			0	0	0	0	1	-1dB
			0	0	0	1	0	-2dB
			.....					
			1	1	1	0	0	-28dB
			1	1	1	0	1	-29dB
			1	1	1	1	0	-30dB
			1	1	1	1	1	MUTE
		0						Left
		1						Right

Port Control

Port No.	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
Function	BBE	TruBass (A) 6dB	Tru Surround	TruBass (B) 12dB	NC	NC	NC	Host/Port

Active High

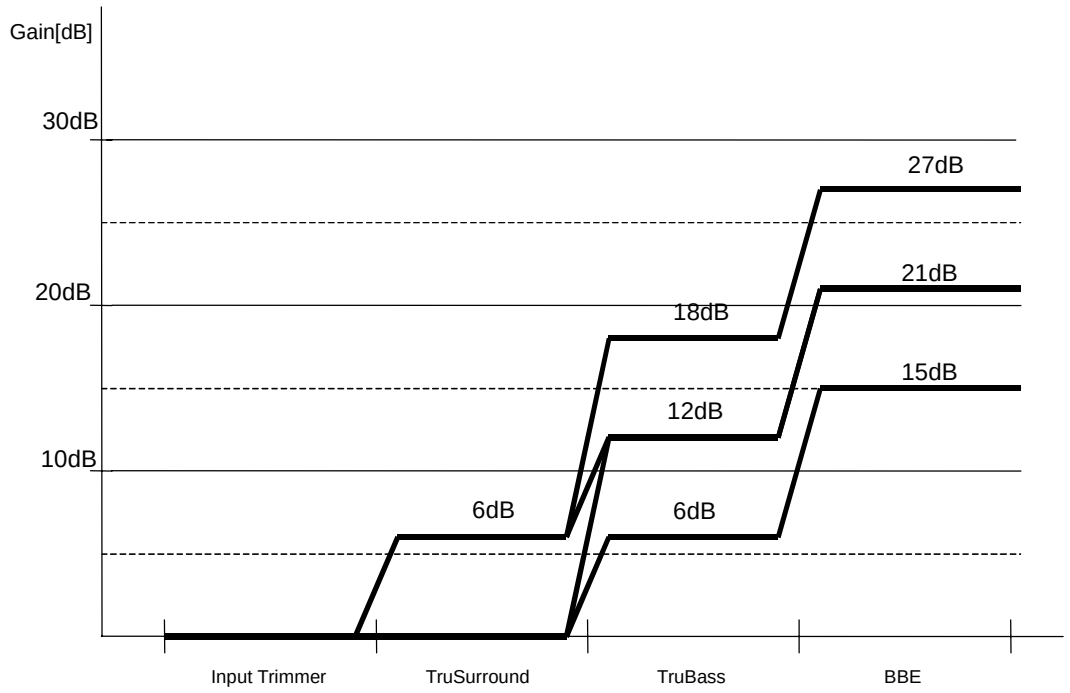


Fig.14

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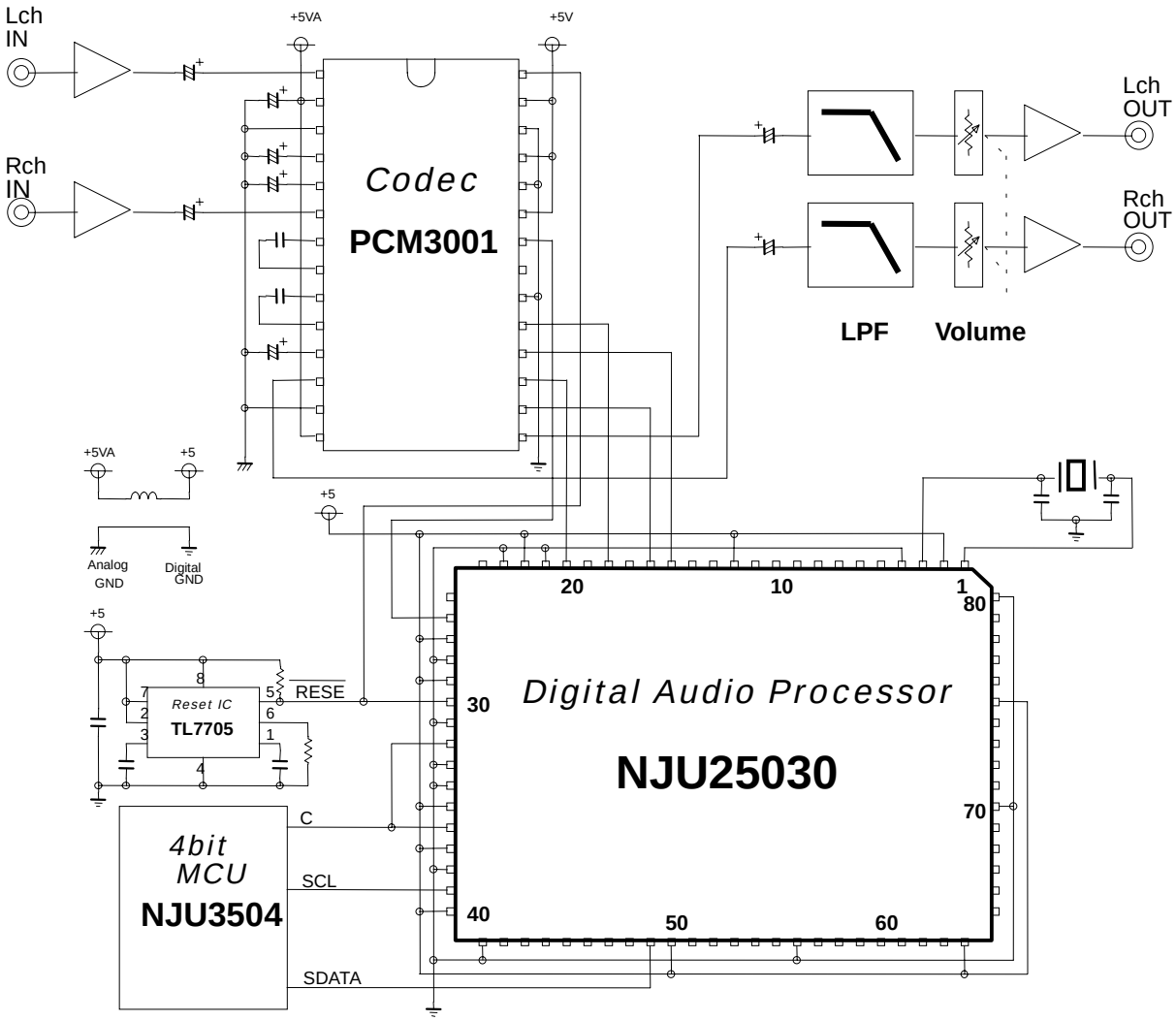
Application Circuit



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