PRELIMINARY

# Virtual Dolby Surround Processor

VIRTUAL DOLBY SURROUND  DOLBY SURROUND PRO • LOGIC

## Description

The NJU25006 is an all-digital surround sound processor that decodes matrix-encoded stereo and produces 2.1 channel PCM digital 3D audio. Because the NJU25006 initially decodes audio into 4.1 channel Dolby Pro Logic and then reprocesses it into 2.1 channels, the resulting 3-D audio contains virtualized surround sound information. The NJU25006 can be used in several system configurations: 2.0 or 2.1 channel Virtual Dolby Surround, and 4.0 or 4.1 channel Pro Logic. The NJU25006 flexibility allows one device to span an entire audio product family and to add enhanced features to your final system configuration.

The Virtual Dolby Surround algorithms create a realistic 360° soundfield that is especially useful in systems that cannot physically accommodate rear surround speakers, such as desktop multi-media computers, arcade games, or stereo TVs. The NJU25006 contains sweet spot adjustment to compensate for the speaker placement relative to the listener.

Note: The Word "DOLBY" and the double D mark are trademarks of Dolby Laboratories. The NJU 25006 can only be delivered to licensees of Dolby Laboratories. Please refer to the licensing application manual issued by Dolby Laboratories.

## Features

- Virtual Dolby Surround Processing
  - 360° surround from just two speakers
  - Realistic rear channel plays through two speakers
  - Optional subwoofer (.1 channel) digital output
- Dolby Pro Logic Decoding
  - 4.1 channel Pro Logic on 6 digital outputs (L, R, SL, SR, C, SW)
  - On-chip digital surround delay, 30ms maximum
  - No External Memory Required
  - Internal Auto Input Balance
- Dolby 3 Stereo
  - 3.1 channel output (L,R,C, SW)
- Mono-to-Stereo Synthesis
- 24-bit Fixed Point Digital Signal Processing
- No DSP Design Required
- 16- or 18-bit External A/D and D/A Converters
- Serial Digital Audio Converter Interface
- $I^2S$, Left and Right Justified Data Modes
- Operates From a Single +5V Supply
- Evaluation Board Available

4

*Figure 1 NJU25006 Block Diagram*

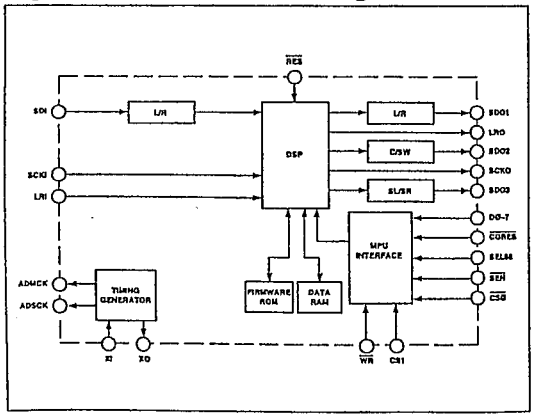



*Figure 2 Virtual Surround System*

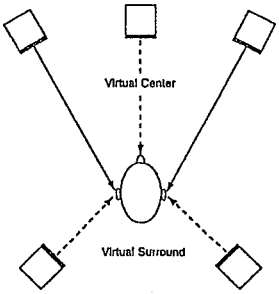


*Figure 3 NJU25006 Pin Configuration*

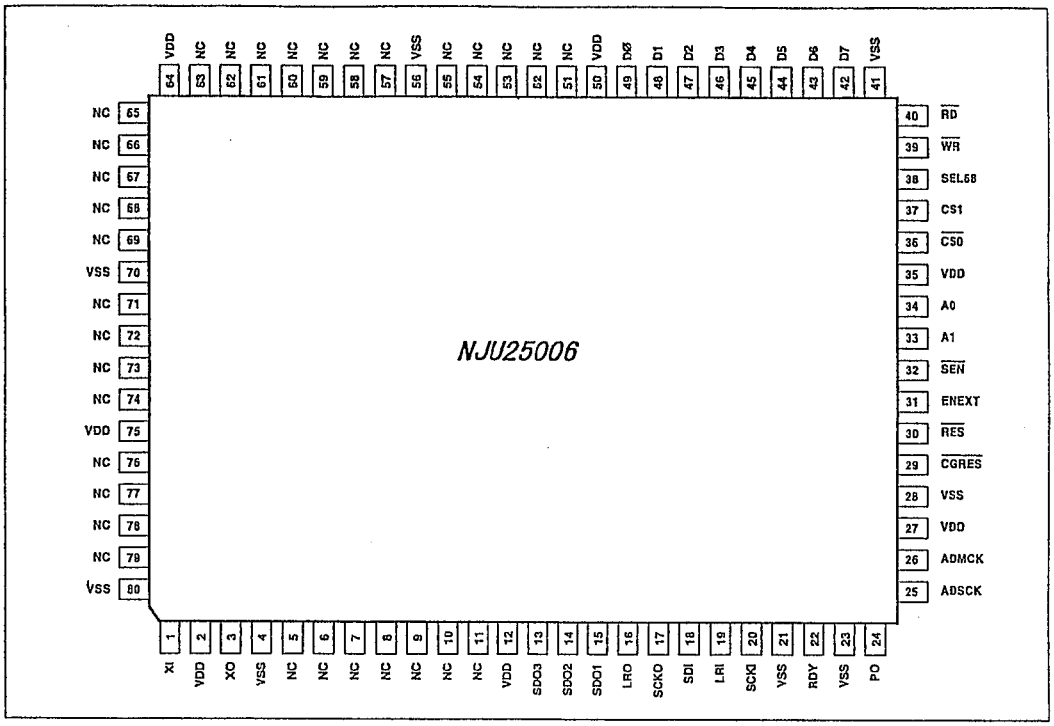
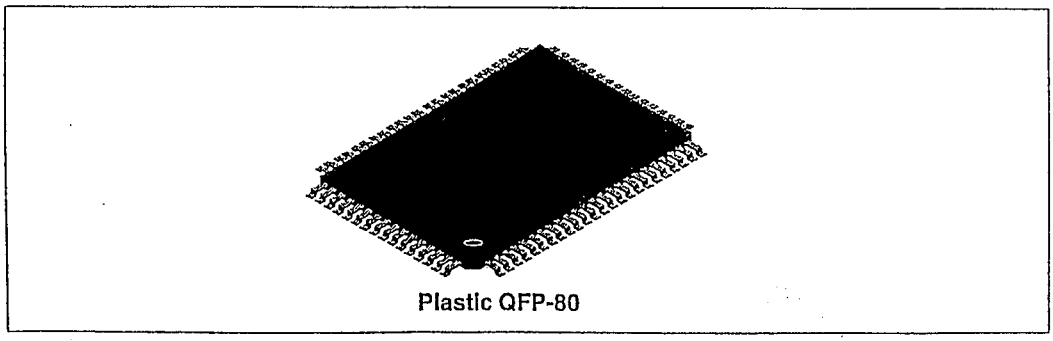



*Figure 4 NJU25006 QFP-80 Package*



## *Table 1 Pin Description*

| No. | Symbol | I/O | Function | No. | Symbol | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1 | XI | I | Crystal/External clock input | 41 | VSS | I | Ground |
| 2 | VDD | I | Power supply terminal: +5V | 42 | D7 | I | MPU data, parallel input (MSB) |
| 3 | XO | O | Crystal | 43 | D6 | I | MPU data, parallel input |
| 4 | VSS | I | Ground | 44 | D5 | I | MPU data, parallel input |
| 5 | NC | | No connect | 45 | D4 | I | MPU data, parallel input |
| 6 | NC | | No connect | 46 | D3 | I | MPU data, parallel input |
| 7 | NC | | No connect | 47 | D2 | I | MPU data, parallel input |
| 8 | NC | | No connect | 48 | D1 | | MPU data, parallel input |
| 9 | NC | | No connect | 49 | D0 | I | MPU data, parallel input (LSB), serial data input ($\overline{SEN}$ = 0) |
| 10 | NC | | No connect | 50 | VDD | I | Power supply terminal: +5V |
| 11 | NC | | No connect | 51 | NC | | No connect |
| 12 | VDD | I | Power supply terminal: +5V | 52 | NC | | No connect |
| 13 | SDO3 | O | Digital audio serial data out, surround right and left | 53 | NC | | No connect |
| 14 | SDO2 | O | Digital studio serial data out, center and subwoofer | 54 | NC | | No connect |
| 15 | SDO1 | O | Digital audio serial data out, front right and left | 55 | NC | | No connect |
| 16 | LRO | O | Output left/right frame clock | 56 | VSS | I | Ground |
| 17 | SCKO | O | Output digital audio serial clock | 57 | NC | | No connect |
| 18 | SDI | I | Input digital audio serial data | 58 | NC | | No connect |
| 19 | LRI | I/O | Input left/right frame clock | 59 | NC | | No connect |
| 20 | SCKI | I/O | Input digital audio serial clock | 60 | NC | | No connect |
| 21 | VSS | I | Ground | 61. | NC | | No connect |
| 22 | RDY | I | Test pin, high for normal operation | 62 | NC | | No connect |
| 23 | VSS | I | Ground | 63 | NC | | No connect |
| 24 | PO | O | Test pin | 64 | VDD | I | Power supply terminal: +5V |
| 25 | ADSCK | O | 32Fs/64Fs serial clock for A/D, D/A converters (default 32Fs) | 65 | NC | | No connect |
| 26 | ADMCK | O | 384Fs/256Fs master clock for A/D, D/A converters (default 384Fs) | 66 | NC | | No connect |
| 27 | VDD | I | Power supply terminal: +5V | 67 | NC | | No connect |
| 28 | VSS | I | Ground | 68 | NC | | No connect |
| 29 | $\overline{CGRES}$ | I | Test pin, normally high | 69 | NC | | No connect |
| 30 | $\overline{RES}$ | I | Reset, must be held low for at least two clock cycles after power on | 70 | VSS | I | Ground |
| 31 | ENEXT | I | Test pin, normally low | 71 | NC | | No connect |
| 32 | $\overline{SEN}$ | I | MPU serial interface enable. Serial = L, parallel = H | 72 | NC | | No connect |
| 33 | A1 | I | Test pin. Low for normal operation | 73 | NC | | No connect |
| 34 | A0 | I | Test pin. Low for normal operation | 74 | NC | | No connect |
| 35 | VDD | I | Power supply terminal: +5V | 75 | VDD | I | Power supply terminal: +5V |
| 36 | $\overline{CS0}$ | I | Chip select, MPU interface enabled when $\overline{CS0}$ = 0 and CS1 = 1 | 76 | NC | | No connect |
| 37 | CS1 | I | Chip select, MPU interface enabled when $\overline{CS0}$ = 0 and CS1 = 1 | 77 | NC | | No connect |
| 38 | SEL68 | I | MPU interface mode: 68K = H, Z80 = L | 78 | NC | | No connect |
| 39 | $\overline{WR}$ | I | Write Strobe (Z80), Write Enable (68K) | 79 | NC | | No connect |
| 40 | $\overline{RD}$ | I | Write Strobe (68K) | 80 | VSS | I | Ground |

## Specifications

The tables in this section give the electrical and timing specifications for the NJU25006. The symbols in the timing parameter tables refer to timing values on the corresponding timing diagrams in the subsection entitled "Timing Diagrams" on page 6.

### Table 2 Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Supply Voltage ($T_A$ = 25°C) | $V_{DD}$ | -0.3 | 7 | V |
| Input, Output Pin Voltage ($T_A$= 25°C) | $V_x$ | -0.3 | $V_{DD}$ + 0.3 | V |
| Operating Temperature | $t_{CASE}$ | -20 | 70 | °C |
| Storage Temperature | $t_{STG}$ | -55 | 125 | °C |

### Table 3 Electrical Characteristics

| Parameter | Symbol | Test Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | $V_{DD}$ pins | 4.75 | | 5.25 | V |
| Operating Current | $I_{DD}$ | $f_{osc}$ = 34 MHz | | 90 | 125 | mA |
| High Level Input Voltage | $V_{IH}$ | | 0.80 $V_{DD}$ | | $V_{DD}$ | V |
| Low Level Input Voltage | $V_{IL}$ | | $V_{SS}$ | | 0.10 $V_{DD}$ | V |
| High Level Input Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | | | 10 | µA |
| Low Level Input Current | $I_{IL}$ | $V_{IN}$ = $V_{SS}$ | | | 10 | µA |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$ = 2 mA | $V_{DD}$ - 1.0 | | | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OH}$ = 2 mA | | | 0.5 | V |
| Input Capacitance | $C_{IN}$ | | | 10 | 20 | pF |
| Clock Frequency | $f_{OSC}$ | | 20 | | 34 | MHz |
| Ext. System Clock Duty Cycle | $r_{EC}$ | | 45 | | 55 | % |

### Table 4 Serial Data Input Timing Parameters ($f_{CLK}$ = 34MHz)

| Parameter | Symbol | Test Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| SCKI Period | | | 160 | | | ns |
| L Pulse Width | $t_{SIL}$ | | 80 | | | |
| H Pulse Width | $t_{SIH}$ | | 80 | | | |
| SCKI to LRI Time | $t_{SLI}$ | | 50 | | | ns |
| LRI to SCKI Time | $t_{LSI}$ | | 75 | | | ns |
| Data Setup Time | $t_{DS}$ | | 10 | | | ns |
| Data Hold Time | $t_{DH}$ | | 10 | | | ns |

### *Table 5 Serial Data Output Timing Parameters ($f_{CLK}$ = 34MHz)*

| Parameter | Symbol | Test Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| SCKO Period | | $C_L$: LRO, SCKO, SDO = 5pF | 160 | | | ns |
| L Pulse Width | $t_{SOL}$ | | 80 | | | |
| H Pulse Width | $t_{SOH}$ | | 80 | | | |
| SCKO to LRO Time | $t_{SLO}$ | | | | 5 | ns |
| Data Output Delay | $t_{DOD}$ | | | | 5 | ns |

### *Table 6 Z80 Interface Timing Parameters ($f_{CLK}$ = 34MHz)*

| Parameter | Symbol | Test Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Address Setup Time | $t_{AS8}$ | | 100 | | | ns |
| Address Hold Time | $t_{AH8}$ | | 100 | | | ns |
| System Cycle Time | $t_{CYC8}$ | | 1,000 | | | ns |
| Read/Write Pulse Width | $t_{CC8}$ | | 100 | | | ns |
| Write Data Setup Time | $t_{DS8}$ | | 10 | | | ns |
| Write Data Hold Time | $t_{DH8}$ | | 10 | | | ns |

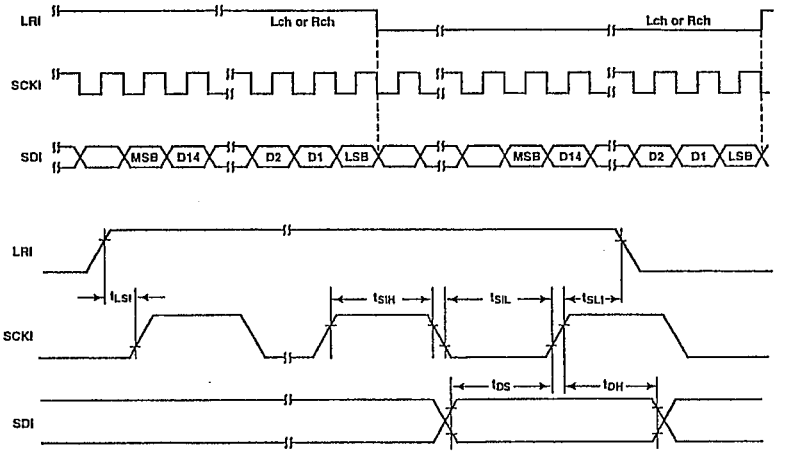
### *Table 7 68K Interface Timing Parameters ($f_{CLK}$ = 34MHz)*

| Parameter | Symbol | Test Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Address Setup Time | $t_{AS6}$ | | 100 | | | ns |
| Address Hold Time | $t_{AH6}$ | | 100 | | | ns |
| System Cycle Time | $t_{CYC8}$ | | 1,000 | | | ns |
| Read/Write Pulse Width | $t_{CC6}$ | | 100 | | | ns |
| Write Data Setup Time | $t_{DS6}$ | | 10 | | | ns |
| Write Data Hold Time | $t_{DH6}$ | | 10 | | | ns |
| Write-to-read Strobe Setup | $t_{WRS}$ | | 100 | | | ns |
| Read-to-write Strobe Setup | $t_{WRH}$ | | 100 | | | ns |

## *Timing Diagrams*

The figures in this section give the timing relationships for the NJU25006. The symbols in the diagrams refer to parameters in the corresponding timing parameter table in the subsection entitled "Specifications" on page 4.

### *Figure 5 Serial Data Input Timing*




### *Figure 6 Serial Data Output Timing*

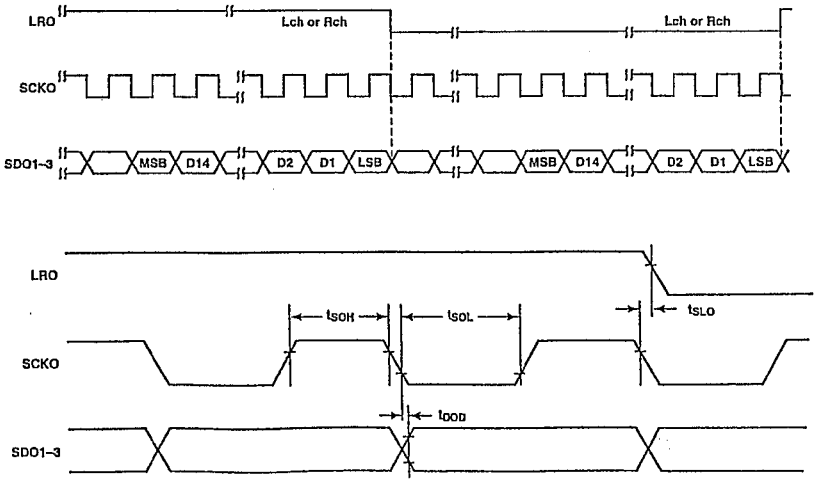


*Figure 7 Left-Justified Data Format, ADSCK = 64 Fs, 18-bit Data*

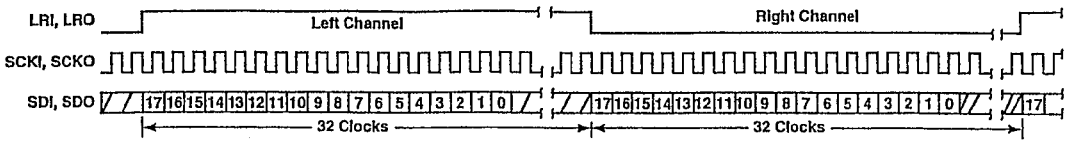



*Figure 8 Right-Justified Data Format, ADSCK = 64 Fs, 18-bit Data*

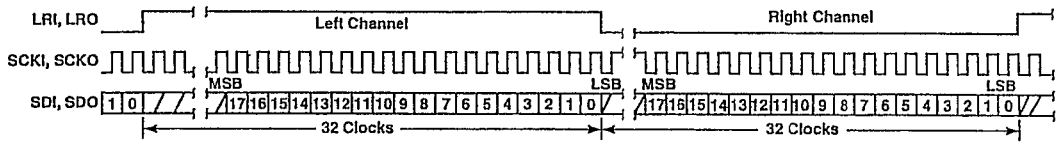



*Figure 9 I²S Data Format, ADSCK = 64 Fs, 18-bit Data*

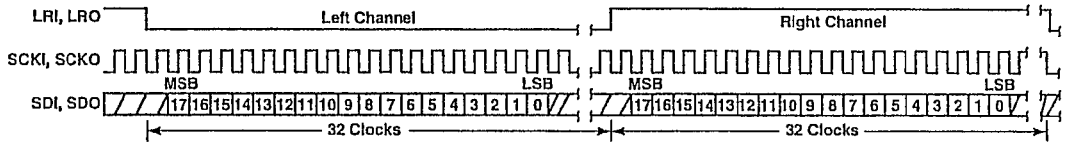



*Figure 10 Right- and Left-Justified Data Formats, ADSCK = 32 Fs, 16-bit Data*

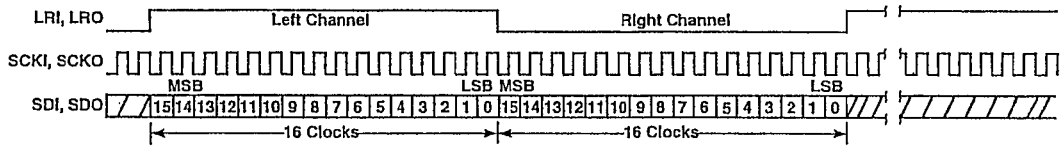



*Figure 11 I²S Data Formats, ADSCK = 32 Fs, 16-bit Data*

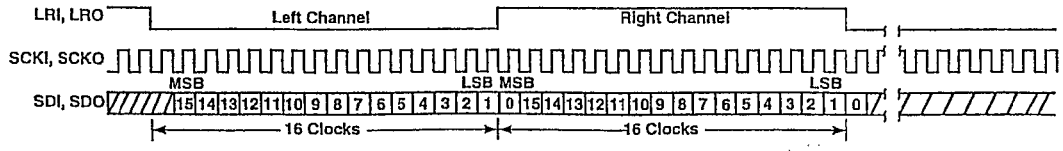


*Figure 12 Z80 Parallel Interface Timing (SEL68 Low)*

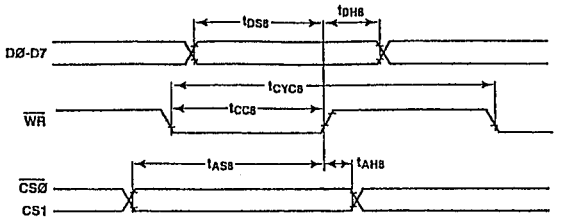



*Figure 13 Z80 Serial Interface Timing (SEL68 Low)*

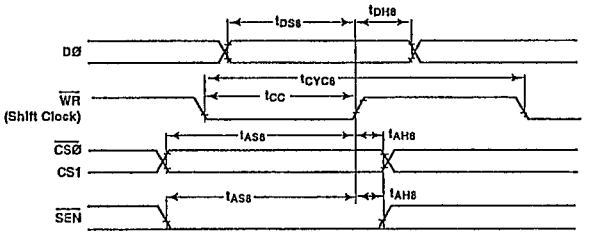



*Figure 14 68K Parallel Interface Timing (SEL68 High)*

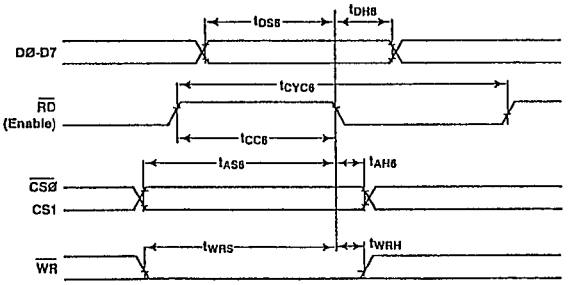
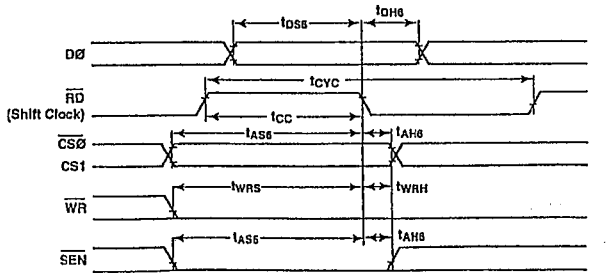



*Figure 15 68K Serial Interface Timing (SEL68 High)*



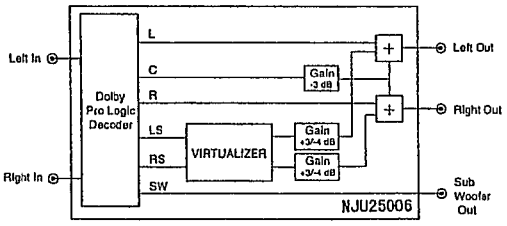
## Functional Description

### Dolby Virtual Surround

The high-quality Medianix 24-bit DSP technology and algorithms in the NJU25006 create the effect that rear speaker surround sound audio is present while only two front speakers are active. A digital audio "0.1 channel" output for a subwoofer is included on the NJU25006.

The processing of virtual Dolby surround begins with decoding audio that includes surround sound information (preferably matrix-encoded stereo). The decoding process uses an on-chip Dolby Pro Logic algorithm, resulting in 4 channel (L, C, R, S) surround sound. Next, the virtualizer algorithm processes the discrete surround sound and combines it, along with the center channel data, with the left and right audio channels. Highly directional encoded source material, such as a movie soundtrack, will result in the most dramatic virtual 3-D sound effect during playback, although all stereo audio sources benefit from Virtual Dolby Surround processing.

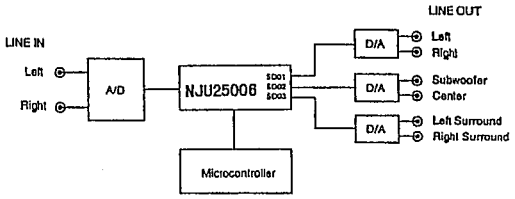
## Figure 16 Virtual Dolby Surround Mode




### Dolby Pro Logic Surround

In order to create Virtual Dolby Surround, it is necessary to perform Dolby Pro Logic decoding first. Because the audio data is available for full 5.1 channel Pro Logic, all the multichannel outputs are optionally available as well, including Left, Right, Left Surround, Right Surround, Center, and Subwoofer. The NJU25006 can be switched under microprocessor control between 2-ch and 6-ch modes. For 4-channel applications using only one surround output feeding both surround speakers and no subwoofer, the Left Surround and Subwoofer data can be swapped in the Configuration Command. This requires only two D/As, or one codec and one D/A on the output for a 4-channel (4.1 ch) surround system with Left, Right, Center, and Surround.

## Figure 17 Typical Dolby Pro Logic System




### Clock Generator

A 768Fs crystal wired to pins XI and XO of the NJU25006 will generate signals that operate the chip's internal circuits as well as signals for external circuits such as A/Ds and D/As. Alternatively, an external clock of 768Fs can be applied to XI, with XO remaining unconnected. Fs can be 32kHz or 44.1 kHz. The signal at the ADMCK pin is set to either 384Fs or 256Fs, and the signal at the ADSCK pin is set to either 32Fs or 64Fs. The default settings are 384Fs and 32Fs, respectively.

### Digital Audio Data Interface

Three digital audio data formats are supported: left justified, right justified, and $I^2S$. The data is always MSB first, 2's complement. Either 16-bit or 18-bit data can be accommodated. The polarities of the L/R clocks (LRI, LRO) are programmable, along with the active edge of the serial bit clocks (SCKI, SCKO). Master clock (ADMCK) and serial bit clock (ADSCK) outputs for the A/D and D/A converters are provided by an internal, programmable clock generator for synchronous operation with the DSP clock (768Fs). Asynchronous data rates are possible as long as the output is slaved to the input and it is close to the two supported sampling frequencies (32kHz and 44.1kHz).

There is one stereo digital audio input and three stereo digital audio outputs for the L and R main channels, L and R surround channels, Center, and Subwoofer. All three serial data outputs must have identical data formats. In each data format mode, SCLK and LRCLK polarities are independently programmable for input and output. Audio data width (16/18 bits), SCK and MCK frequencies (32/64Fs, 256/384Fs, respectively) must be the same for both input and output.

### Serial Data Formats

There are three serial data formats supported for interfacing an A/D and three D/As to the digital audio interface. Either Left Justified, Right Justified, or $I^2S$ mode is selected by the FMT0 and

FMT1 bits in the second byte of the three-byte System State Download Command. In Left Justified Mode, the MSB is aligned to the edge of LRI or LRO. The data is positioned at the left or "front" side of the L/R pulse (see Figure 7). In Right Justified Mode, the LSB is aligned to the LRI or LRO edge. The data is at the right or "rear" of the L/R pulse (see Figure 8). Sometimes this mode is called Japanese Mode or EIAJ Mode. The $I^2S$ Mode is similar to Left Justified Mode, except that the data is delayed one SCLK period and the sense of LRI and LRO is inverted (see Figure 9). In $I^2S$ Mode, LRI and LRO must be low for left channel data and high for right channel data, the opposite of other modes. The polarity of LRI and LRO can be inverted independently in any mode by the use of the LRI and LRO.

Normally, the serial data bits generated by a source change on the falling edge of the serial clock so that they can be easily clocked into a shift register on the rising clock edge. Considering an A/D as the source and the NJU25006 as a destination, the default setting is to clock the serial data input, SDI, in on the rising edge of SCKI. This can be changed to clock data in on the falling edge using the SCKI bit in the System Download Command.

For the output serial data, the NJU25006 is considered the source and the D/As are considered the destination. The default interface setting is for data to be clocked out of SDO on the falling edge of SCKO so that the D/A clocks data in on the rising edge. This can be changed independently of the input and interface mode using the SCKO bit in the System Download Command.

The MS (Master/Slave) bit in the second System State Download Command byte selects either Master Mode or Slave Mode. In Right Justified Mode, Master Mode (MS = 0) is defined such that SCKO and LRO are generated from an internal divider derived from the 768Fs DSP clock (XI). In Slave Mode (MS = 1) SCKO and LRO are the same as SCKI and LRI on the input. This mode should be used for asynchronous data rates, such as data from an S/PDIF receiver connected to the Digital Output from a laser disc player. The output D/A's must be synchronized to the input data by using the low jitter, recovered clock from the S/PDIF receiver to the D/A master clock. When an A/D is used, its master clock should be synchronous to the NJU25006 using ADMCK at 256Fs or 384Fs. In this case either Master Mode or Slave Mode will work. The default setting is Master Mode (MS = 0).

In $I^2S$ Mode, Master and Slave modes have slightly different meanings. Relative to the NJU25006, Slave Mode (MS = 1) is defined as LRI and SCKI being inputs from the A/D. This means that the A/D must be in Master Mode with L/R and SCLK outputs. Conversely, when the NJU25006 is in Master Mode (MS = 0), LRI and SCKI are outputs that drive the L/R and SCLK inputs of an A/D operating in slave mode. SCKO and LRO to the D/As are always outputs. The D/A converters can run only in Slave Mode, receiving both the L/R and SCLK from the NJU25006. LRO and SCKO are derived from the 768Fs DSP clock. When slave mode is selected, LRO and SCKO are generated by the LRI and SCKI inputs. Slave mode should be used for asynchronous audio data.

When using a codec in slave mode and operating the NJU25006 in $I^2S$ Master Mode, the LRO signal must be used to drive the L/R input of the codec. Although LRI is not used, it must be programmed with the opposite polarity. This is the default setting upon initialization after reset (LRI=0, LRO=1) for typical 2-channel Virtual Dolby Surround applications. For more details, refer to the EVB25006-3 Demonstration Board User's Guide. In all other modes or when using separate A/D and D/A converters that use both LRI and LRO, respectively, the polarity should be the same for LRI and LRO.

For applications that switch between Virtual and Pro Logic Surround modes using a codec for L/R input and front L/R output, and two D/A converters for the other four channels, the L/R input clock for all the converters must operate from the LRO signal generated by the NJU25006. The LRI signal is not used when a codec is included, but it must be programmed with opposite polarity. The same applies for a single 6-channel codec. When using a codec and two D/A's, it may be better to use the codec for the surround channels, since the discrete D/A's often have better audio performance, critical for the main Left and Right output. The Left and Right Surround outputs can afford to have lower S/N and THD specifications, characteristic of many low cost codecs.

In Left Justified Mode, only Slave Mode (MS = 0) is allowed. The A/D is required to be in Master Mode and supplies LRI and SCKI to the NJU25006. LRO and SCKO are generated from LRI and SCKI inputs.

For each data format, the serial clock frequency for SCKI and SCKO is selected using ADSCK in the System Download Command: either 32Fs (32-bit clocks per sample) or 64Fs (64-bit clocks per sample). SCKI and SCKO must be the same fre-

quency. This clock is generated internally for the SCKI and SCKO in Master Mode, but is also available as an output on the ADSCK pin. It is derived from the 768Fs Input Clock to the NJU25006.

If SCKI and SCKO are selected to be 32Fs, the data length must be set to 16-bits (BL = 0) because a stereo pair of 16-bit channels needs all 32 clocks per sample. In this case, both Left and Right Justified Modes look exactly the same (see Figure 10), and either mode setting will work. In $I^2S$ mode, the data bits appear shifted by one SCLK and the L/R is inverted (see Figure 11).

An output clock, ADMCK, is derived from the NJU25006 768Fs Input Clock for use as an A/D or D/A master clock. ADMCK is set to 256Fs or 384Fs using the ADMCK bit in the System Download Command.

### *Microcontroller Interface*

Either a Z80 or 68K type microcontroller can be used to download commands to the NJU25006. SEL68 must be set high for 68K and low for Z80. Either serial or 8-bit parallel interface modes may be used, depending on SEN input (L = serial and H = parallel). The MPU interface is enabled when CS0 = 0 and CS1 = 1, allowing a control signal of either polarity to be used.

*Figure 18 Z80 Interface*

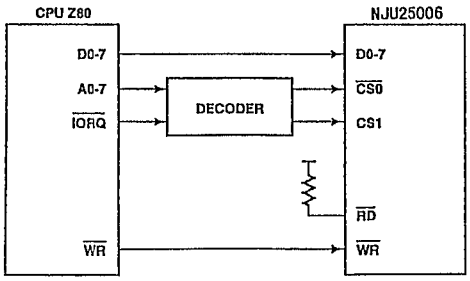
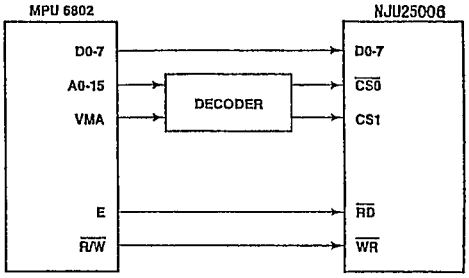



*Figure 19 68K Interface*




The audio stops when the NJU25006 receives a System State Download Command, when Simulated Surround Mode coefficients are downloaded, or when the Noise Sequencer is turned on. All other commands take immediate effect without interruption in the audio. Only one command should be sent from the microprocessor per L/R period. The DSP in the NJU25006 spends most of the time processing audio, during which time microprocessor interrupts are disabled. Writing to the MPU interface sets an interrupt request flag inside the chip and holds the data in a register, which is read as soon as the interrupt can be serviced. Successive writes to the MPU interface while the interrupts are disabled will overwrite the previous contents. There is a window of time in each audio sample when it is possible to service several MPU commands. However; there is no way for the microprocessor to determine how long this window is before the audio interrupt arrives and successive MPU writes will be lost. Therefore, when audio is being processed, it is recommended that only one command be sent to the NJU25006 for each audio sample, even though the logic will accept parallel writes up to 1 Mbyte per second. When the audio is interrupted (for example, during System State Download Commands or when Simulated Surround coefficients are being transferred), data can be transferred at the maximum data rate, with at least 1 ms between bytes written to the NJU25006.

The MPU interface was designed for both read and write operations. However, the DSP firmware only supports write operations.

### *Parallel Interface*

#### *Z80 Mode*

Writing commands to the NJU25006 from a Z80 type microprocessor is accomplished by setting SEL68 low placing data on the input data port, D0 to D7, setting the chip selects, and strobing WR low then high. Successive writes, as in the three-byte System Download Command, can be done without resetting the chip select(s). It is recommended to return the Chip Select to the inactive state as soon as the command is sent. The recommended sequence for writing parallel data to the NJU25006 is:

1. Set RD high (can be tied to Vcc).
2. Place data on the data port, D0:7.
3. Assert chip selects, CS0 = 0 and CS1 = 1).

   One can be permanently tied to its active state, while the other is controlled.
4. Strobe WR low, then high.
5. Deactivate chip selects.
6. Wait at least one audio sample before sending another command.

#### *68K Mode*

In 68K mode (SEL68 High) RD acts as a strobe for both read and write operations. WR defines whether a read or write is to be performed (L = write to NJU25006; H = there is no provision for reading from NJU25006). Since only write operations are allowed, WR can be tied low. The recommended sequence to write parallel data to the **NJU25006** in this mode is:

1. Set WR low (can be tied to GND).
2. Place data on the data port, D0:7.
3. Assert chip selects, (CS0 = 0 and CS1 = 1).

   One can be permanently tied to its active state, while the other is controlled.
4. Strobe RD high, then low.
5. Deactivate chip selects.
6. Wait at least one audio sample before sending another command.

### *Serial Interface*

In serial interface mode (SEN = 0), D0 is used for the serial data input. Two types of interface modes are supported. In Z80 mode (SEL68 low) WR is used as a serial bit clock. In 68K mode (SEL68 high), RD is used to clock the serial data. Data is clocked in 8 bits at a time with a maximum data rate of 1 MHz. As in Parallel Mode above, it is recommended that only one command be sent per audio sample while audio is playing. For commands that cause the audio to stop, data can be written to the microprocessor interface at the maximum bit rate of 1MHz (and 1 ms between bytes).

#### *Z80 Mode*

When using a microprocessor with a Z80 type interface, writing serial data to the NJU25006 is done by clocking the data in on rising edges of the WR, with RD held high (SEL68 = 0). The recommended sequence is:

1. Set SEN = 0
2. Assert chip selects, (CS0 = 0 and CS1 = 1).
3. Set RD high.
4. Clock in serial data with WR (rising edge).
5. Deactivate chip selects.
6. Wait 1 audio sample before sending next byte (1 ms if audio stopped).

#### *68K Mode*

For 68K type microprocessors, the function of RD and WR is opposite of the Z80. Writing serial data to the NJU25006 is done by setting WR low and clocking the data in on rising edges of RD (SEL68 = 1) The recommended sequence is:

1. Set SEN = 0.
2. Assert chip selects, (CS0 = 0 and CS1 = 1).
3. Set WR low.
4. Clock in serial data with RD (falling edge).
5. Deactivate chip selects.
6. Wait 1 audio sample before sending next byte (1 ms if audio stopped).

## *Microcontroller Command Descriptions*

This section explains each of the commands that can be sent to the NJU25006. See the subsection entitled "Microcontroller Command Tables" on page 17 for details on each of the command bytes

### *Configuration Command*

After power is applied and a hardware reset is generated on the RES pin (pin 30), three bytes must be sent from the microprocessor that defines the hardware settings of the NJU25006. This data controls the digital audio interface format, the Clock Generator outputs, and the channel assignment for the output surround data. This is the only multi-byte command. All the others are single byte and take effect immediately without interruption of the audio processing. The other commands contain a non-zero "op code" and all data bits in one byte.

When the DSP receives the first byte of the Configuration Command, which is all zeroes, the audio stops and the DSP waits for two more bytes. These hardware settings are intended to be set once, and not changed unless the chip is reset again. The definitions of all the data bits are listed in the subsection entitled "Microcontroller Command Tables" on page 17.

Byte #1—Configuration Command op code, 00h.

Byte #2

| MODE 1, 0 | Serial audio data justification format |
|---|---|
| 0,0 | Right justified |
| 1,0 | $I^2S$ |
| 1,1 | Left justified |

| MS | Master/Slave |
|---|---|
| 0 | Master mode* |
| 1 | Slave mode |

| BIO | Serial audio data I/O number of bits |
|---|---|
| 0 | 16 bits |
| 1 | 18 bits* |

| LRI | Input L/R Clock polarity |
|---|---|
| 0 | Left data on SDI when High, Right data on SDI when Low* |
| 1 | Right data on SDI when High, Left data on SDI when Low |

Note: In $I^2S$ Master Mode, LRI becomes an output.

* Indicates the default setting

| SCKI | Serial Clock for Input audio data |
|---|---|
| 0 | Serial data on SDI latches on rising edge* |
| 1 | Serial data on SDI latches on falling edge |

Note: In $I^2S$ Master Mode, SCKI becomes an output, and the function is identical to SCKO.

| LRO | Output L/R Clock |
|---|---|
| 0 | Left data on SDOn when High, Right data on SDOn when Low |
| 1 | Right data on SDOn when High, Left data on SDOn when Low* |

| SCKO | Serial Clock for Output audio data |
|---|---|
| 0 | Serial data on SDOn changes on falling edge* |
| 1 | Serial data on SDOn changes on rising edge |

Byte #3

| ADMCK | A/D-D/A Master Clock output |
|---|---|
| 0 | 384Fs* (1/2 DSP clock, 768Fs) |
| 1 | 256Fs (1/3 DSP clock, 768Fs) |

| ADSCK | A/D-D/A Serial data Clock output |
|---|---|
| 0 | 32Fs* (1/24 DSP clock, 768Fs) |
| 1 | 64Fs (1/12 DSP clock, 768Fs) |

| SWP | Swap Subwoofer and Left Surround |
|---|---|
| 0 | 6ch mode: L/R on SDO1, SW/C on SDO2, LS/RS on SDO3 |
| 1 | 4ch mode: L/R on SDO1, LS/C on SDO2, SW/RS on SDO3. Allows 4ch Pro Logic Surround using only 2 stereo DACs |

### *Sampling Frequency Command*

In most cases, it is desirable to keep the 768Fs DSP clock synchronous with the converter clocks and the sample rate according to the following table.

| Sample Rate | 768Fs DSP Clock |
|---|---|
| 32 kHz | 24.576 MHz |
| 44.1 kHz | 33.8688 MHz |

There are time constants and other audio processing functions that require an absolute time reference. Since the DSP has no way of knowing what frequency the input clock is, this com-

mand is necessary to establish a real time reference according to the data below.

| FS1, FS0 | Sampling Frequency |
|---|---|
| 0, 0 | 32kHz |
| 0, 1 | 44.1kHz* |
| 1, 0 | Reserved |

### *Noise Sequencer Command*

A pink noise generator is required for Dolby Pro Logic to set the levels for the front, center, and surround speakers. When the noise sequencer is turned ON, the audio input is ignored, and the noise generator is output on the channel selected, with all other channels muted.

| NS | Noise Sequencer On/Off |
|---|---|
| 0 | OFF*, normal audio output |
| 1 | ON, noise generator on selected channel |

| NCH1, 0 | Noise Sequencer Channel |
|---|---|
| 0, 0 | Left |
| 0, 1 | Center |
| 1, 0 | Right |
| 1, 1 | Surround (both LS and RS) |

### *Auto Input Balance/Crossover Filters Command*

The NJU25006 can automatically compensate for mismatch in level between the Left and Right stereo input. This is done by continuously comparing the ratio of Center Channel signal to the other signals and minimizing the Center from Left and Right. At the same time, this assures optimum Surround under varying conditions, such as slight shift in balance due to program changes in TV.

| IBL | Auto Input Balance |
|---|---|
| 0 | OFF |
| 1 | ON* |

There is a single-pole, low-pass crossover filter for the Subwoofer output with a -3dB cutoff frequency selected. When using external filters, the Low Pass Filter on the SW output may be bypassed with full-bandwidth mix of L and R.

| LPF1, 0 | Low Pass Crossover Filter |
|---|---|
| 0, 0 | Full bandwidth, no filtering |
| 0, 1 | 80Hz* |
| 1, 0 | 120Hz |
| 1, 1 | 160Hz |

If a subwoofer is used, typically smaller front speakers may be used that have limited low frequency response. In this case, driving them with full bandwidth audio may cause distortion. Turning on the single- pole High Pass Crossover Filters on the Front Left and Right channels will prevent this. When turned ON, the High Pass -3dB cutoff frequency is set to match the Subwoofer cutoff frequency set above.

| HPF | High Pass Crossover Filter |
|---|---|
| 0 | OFF*, full bandwidth to Front Left and Right |
| 1 | ON, cutoff frequency same as Subwoofer |

Note: High-pass filters are bypassed (full bandwidth) when Noise Sequencer is ON.

### *Operating Mode Command*

Sets the audio processing to be performed: Dolby Pro Logic, Virtual Dolby Surround, Simulated Stereo, or Surround Off (normal stereo).

| OP1, OP0 | Operating Mode |
|---|---|
| 0, 0 | Dolby Pro Logic (5.1ch, L,R,SW,C,LS,RS) |
| 0, 1 | Virtual Dolby Surround (2.1ch, L,R,SW)* |
| 1, 0 | Simulated Stereo (mono-to-stereo synthesis) |
| 1, 1 | Surround OFF (Normal Stereo) |

### *Surround Mode Command*

For systems limited to only the front speakers, Left, Center, and Right, Dolby 3 Stereo can be selected to mix the surround information into the front Left and Right outputs. All the Dolby Surround information can be heard, except from the front only. The Center Channel is output the same way in both Dolby 3 Stereo and Dolby Pro Logic modes.

| SM | Surround Mode |
|---|---|
| 0 | Dolby 3 Stereo (3.1ch, L,R,C) |
| 1 | Dolby Pro Logic* (5.1ch, L,R,SW,C,LS,RS) |

Because the Surround audio in Dolby Pro Logic is mono (same audio data for both Left and Right Surround), the NJU25006 provides an enhanced, "Widefield Surround" with additional audio processing that decorrelates the Left and Right Surround channels, similar to the technique used for mono-to-stereo synthesis in the Simulated Surround Mode. In addition, the surround channels are full bandwidth. Because this is added processing to Pro Logic, Dolby may require a separate indicator showing that this function is operating in conjunction with Dolby Pro Logic.

| WFS | Widefield Surround |
|---|---|
| 0 | OFF* |
| 1 | ON |

Normally, for all the surround modes, the surround channels are delayed by a minimum of 15 ms. For Dolby Pro Logic, the delay requirement is 15 to 30ms. There may be some cases where zero surround delay is desired. The delay memory may be bypassed by setting the DLY bit. Since the delay memory is 16 bits wide, the output data is reduced to 16 bits when interfacing to 18-bit data input. Bypassing the Surround Delay maintains 18-bit data from input to output in Dolby Surround mode. Note that Dolby certified equipment may require a front panel indicator showing the departure from the Pro Logic specification.

| DLY | Surround Delay |
|---|---|
| 0 | ON* |
| 1 | OFF (bypass) |

### *Center Mode Command*

Pro Logic requires the Center channel control to include a Phantom Mode, in addition to Normal and OFF mode. Phantom Mode is intended for 4.1channel systems where there is no center channel. In this mode, the Center audio is mixed equally with the Right and Left front channels to create a center image between the speakers. In Virtual Dolby Mode, by definition, the Center channel is already operated as a Phantom mode. This setting has no further effect in Virtual Dolby Mode.

Turning the Center Channel OFF has the effect of removing the center image audio, similar to a "Vocal Fader" Karaoke mode where the singer's voice or dialog can be diminished. In Virtual Dolby Surround mode, when Center is turned OFF, it is removed from the 2 channel Left/Right mix.

Because the Center Channel in Dolby Pro Logic is primarily intended for movie dialog, filtering is applied to the Center so that very low bass energy and high frequency sound effects are removed leaving mostly voice bandwidth in the center speaker. The center normally needs to be band limited because usually a small speaker or internal TV speaker is used that is unable to handle full bandwidth. However, when listening to music in Dolby Pro Logic or Virtual Dolby Surround Modes, it may be desirable to allow full bandwidth audio to go to the center channel. A musical source may include low or high frequency solo instruments that were recorded as a center stereo image. In this case, the NJU25006 filters can be removed from the Center Channel processing by activating the Wide Band Center Mode. Dolby may require an indicator showing this is not the normal Pro Logic processing.

| CM1, CM0 | Center Mode |
|---|---|
| 0, 0 | Center ON* |
| 0, 1 | Phantom |
| 1, 0 | Wide Band (full bandwidth) |
| 1, 1 | Center OFF |

### *Balance Command*

Left/Right balance control is accomplished by attenuating one channel at a time up to 16 dB in 1dB steps according to the command data. Balance operates in any Operating Mode, but only on the front channels—Left and Right Surround channels are unaffected. The data field is coded as a 2's complement binary value.

| BAL4-BAL0 | Left | Right | Balance |
|---|---|---|---|
| 01111 | 0dB | -15dB | Minimum Right |
| 01110 | 0dB | -14dB | |
| • | • | • | • |
| 00001 | 0dB | -1dB | |
| 00000 | 0dB | 0dB | Center* |
| 11111 | -1dB | 0dB | |
| • | • | • | • |
| 10001 | -15dB | 0dB | |
| 10000 | -16dB | 0dB | Minimum Left |

### *Level Trim Command*

The Center and Surround Channels are required to have a level trim for Dolby Pro Logic of +10dB to -10dB. The NJU25006 provides a range of 0 dB to -31 dB attenuation. To obtain +10dB gain, it will be necessary to set the NJU25006 to nominal -10 dB and apply +10 dB gain in the audio path for that channel. In addition to Center and Surround, the Subwoofer and Master Volume may be attenuated by the same range. The volume and trim control may be done either digitally in the NJU25006 or with analog techniques. In order to preserve the maximum signal-to-noise audio performance, it is better to use analog attenuators external to the DSP, since the signal and noise will be attenuated in the same ratio. Attenuation in the digital domain, although easily

done, attenuates the signal only with the system noise level remaining constant. The signal- to-noise ratio increases with increasing attenuation. Nothing is lost in the NJU25006 that has over a 140 dB dynamic range. However, system signal-to-noise is limited by the resolution and S/N of the A/D and D/A converters in a digital audio system. After deducting operating headroom for input signal range and level trims, inadequate dynamic range remains unless high resolution data converters are employed.

| CH1, CH0 | Channel |
|---|---|
| 0, 0 | Center |
| 0, 1 | Surround |
| 1, 0 | Subwoofer |
| 1, 1 | Master Volume* |

| TR4-TR0 | Trim Level |
|---|---|
| 00000 | 0dB* |
| 00001 | -1dB |
| • | • |
| 11110 | -30dB |
| 11111 | -31dB |

4

### *Surround Delay Time Command*

Dolby Pro Logic requires the surround channels to be delayed from 15 ms to 30 ms. An internal 16-bit wide SRAM has 1.5 Kbytes for 1,536 audio samples. The delay memory can be bypassed (0 ms delay) using the DLY bit of the Surround Mode Command.

| DLY3-DLY0 | Delay |
|---|---|
| 1111 | 30 ms |
| 1110 | 29 ms |
| • | • |
| 0101 | 20 ms* |
| • | • |
| 0001 | 16 ms |
| 0000 | 15 ms |

### *Virtual Surround Angle Command*

Virtual Dolby Surround is optimized for speakers that are relatively close together, such as multimedia computer and TV applications. For speakers that are farther apart, there is an angle control to change the optimization. If the speakers are spread out at a 15° angle or less from the listener, best surround is achieved using the narrow 15° setting. For speakers which are closer to 20°, the surround effect will be better using the wide setting.

| AGL | Angle |
|---|---|
| 0 | 15° Narrow* |
| 1 | 20° Wide |

### *Virtual Surround Level Command*

The amount of rear channel surround effect that is mixed into the front channels has an adjustment range of -4 dB to +3 dB (default). This is unaffected by the Surround Trim in the Pro Logic processing that precedes the Virtualizer process.

| VSL2-VSL0 | Virtual Surround Level |
|---|---|
| 111 | +3dB* |
| 100 | 0dB |
| 000 | -4dB |

* indicates the default setting

## *Microcontroller Command Tables*

In the following tables, * indicates the default setting.

### *Configuration Command (3 bytes)*

#### *Byte 1—Download Command*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Command |

#### *Byte 2—Download Data, Hardware Settings*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 2 | |
|---|---|---|---|---|---|---|---|---|---|
| MODE1 | MODE0 | MS | BIO | LRI | SCKI | LRO | SCKO | Data, Hardware Settings | |
| | | | | | | | 0 | ⌐▼⌐ | Data on SDOn changes on falling edge* |
| | | | | | | | 1 | ⌐▲⌐ | Data on SDOn changes on rising edge |
| | | | | | | 0 | | L R | Left data on SDOn when high; right if low |
| | | | | | | 1 | | L R | Right data on SDOn when high; left if low* |
| | | | | | 0 | | | ⌐▲⌐ | Serial data on SDI latches on rising edge* |
| | | | | | 1 | | | ⌐▼⌐ | Serial data on SDI latches on falling edge |
| | | | | 0 | | | | L R | Left data on SDI when high; right if low* |
| | | | | 1 | | | | L R | Right data on SDI when high; left if low |
| | | | 0 | | | | | | Data width 16 bits |
| | | | 1 | | | | | | Data width 18 bits* |
| | | 0 | | | | | | | Master mode* |
| | | 1 | | | | | | | Slave Mode |
| 0 | 0 | | | | | | | | Right justified |
| 1 | 0 | | | | | | | | I²S* |
| 1 | 1 | | | | | | | | Left justified |

Note: In I²S Master Mode, SCK1 becomes an output, and the function is identical to SCKO. Also, in I²S Master Mode, LRI becomes an output

#### *Byte 3—Download Data, Clock Outputs*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 3 | |
|---|---|---|---|---|---|---|---|---|---|
| ADMCK | ADSCK | 1 | 0 | 0 | 1 | SWP | 0 | Data, Clock Outputs | |
| | | | | | | | | Reserved | |
| | | | | | | 0 | | 6ch mode | (SW/C,LS/RS)* |
| | | | | | | 1 | | 4ch mode | (LS/C,SW/RS) |
| | | | | | | | | Reserved | |
| | 0 | | | | | | | 32Fs* | A/D-D/A SCLK |
| | 1 | | | | | | | 64Fs | |
| 0 | | | | | | | | 384Fs* | A/D-D/A MCLK |
| 1 | | | | | | | | 256Fs | |

### *Sampling Frequency*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | FS1 | FS0 | 0 | Command | |
| | | | | | | | | Reserved | |
| | | | | | 0 | 0 | | 32kHz | |
| | | | | | 0 | 1 | | 44.1kHz* | |

*Noise Sequencer*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | NS | NCH1 | NCH0 | Command |
| | | | | | | 0 | 0 | Left |
| | | | | | | 0 | 1 | Center |
| | | | | | | 1 | 0 | Right |
| | | | | | | 1 | 1 | Surround* |
| | | | | | 0 | | | OFF* |
| | | | | | 1 | | | ON |

*Auto Input Balance/Crossover Filters*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | IBL | HPF | LPF1 | LPF0 | Command | |
| | | | | | | 0 | 0 | Full BW | Subwoofer Cutoff Frequency |
| | | | | | | 0 | 1 | 80Hz* | |
| | | | | | | 1 | 0 | 120 Hz | |
| | | | | | | 1 | 1 | 160 Hz | |
| | | | | | 0 | | | OFF* | Front L/R High-pass filter |
| | | | | | 1 | | | ON | |
| | | | | 0 | | | | OFF | Auto Input Balance |
| | | | | 1 | | | | ON* | |

*Operating Mode*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | OP1 | OP0 | 0 | Command |
| | | | | | | | 0 | Reserved |
| | | | | | 0 | 0 | | Dolby Pro Logic (5.1ch) |
| | | | | | 0 | 1 | | Virtual Surround (2.1ch)* |
| | | | | | 1 | 0 | | Simulated Stereo |
| | | | | | 1 | 1 | | Surround OFF (Normal Stereo) |

*Surround Mode*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | SM | WFS | DLY | Command | |
| | | | | | | | 0 | ON* | Surround Delay |
| | | | | | | | 1 | OFF | |
| | | | | | | 0 | | OFF* | Widefield Surround |
| | | | | | | 1 | | ON | |
| | | | | | 0 | | | Dolby 3 Stereo (3.1ch) | |
| | | | | | 1 | | | Dolby Pro Logic (5.1ch)* | |

*Center Mode*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | CM1 | CM0 | 0 | Command |
| | | | | | | | 0 | Reserved |
| | | | | | 0 | 0 | | Center ON* |
| | | | | | 0 | 1 | | Phantom |
| | | | | | 1 | 0 | | Wideband (full BW) |
| | | | | | 1 | 1 | | Center OFF |

*Balance*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | BAL4 | BAL3 | BAL2 | BAL1 | BAL0 | Left | Right | |
| | | | 0 | 1 | 1 | 1 | 1 | 0 dB | -15 dB | Minimum Right |
| | | | 0 | 1 | 1 | 1 | 0 | 0 dB | -14 dB | |
| | | | • | • | • | • | • | • | • | |
| | | | 0 | 0 | 0 | 0 | 1 | 0 dB | -1 dB | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 dB | 0 dB | Center* |
| | | | 1 | 1 | 1 | 1 | 1 | -1 dB | 0 dB | |
| | | | • | • | • | • | • | • | • | |
| | | | 1 | 0 | 0 | 0 | 1 | -15 dB | 0 dB | |
| | | | 1 | 0 | 0 | 0 | 0 | -16 dB | 0 dB | Minimum Left |

*Level Trim*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 1 | CH1 | CH0 | TR4 | TR3 | TR2 | TR1 | TR0 | Command |
| | | | 0 | 0 | 0 | 0 | 0 | 0 dB* Level |
| | | | 0 | 0 | 0 | 0 | 1 | -1dB |
| | | | 0 | 0 | 0 | 1 | 0 | -2dB |
| | | | • | • | • | • | • | • |
| | | | 1 | 1 | 1 | 1 | 0 | -30dB |
| | | | 1 | 1 | 1 | 1 | 1 | -31dB |
| | 0 | 0 | | | | | | Center Channel |
| | 0 | 1 | | | | | | Surround Channel |
| | 1 | 0 | | | | | | Subwoofer Channel |
| | 1 | 1 | | | | | | Master Volume* |

*Surround Delay*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | DY3 | DLY2 | DLY1 | DLY0 | Command |
| | | | | 1 | 1 | 1 | 1 | 30 ms |
| | | | | 1 | 1 | 1 | 0 | 29 ms |
| | | | | • | • | • | • | • |
| | | | | 0 | 1 | 0 | 1 | 20 ms* |
| | | | | • | • | • | • | • |
| | | | | 0 | 0 | 0 | 1 | 16 ms |
| | | | | 0 | 0 | 0 | 0 | 15 ms |

*Virtual Surround Angle*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | AGL | Command | |
| | | | | | | | 0 | ±15°* | Narrow |
| | | | | | | | 1 | ±20° | Wide |
| | | | | | | | | Reserved | |

*Virtual Surround Level*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | VSL2 | VSL1 | VSL0 | Command |
| | | | | | 1 | 1 | 1 | +3 dB* |
| | | | | | • | • | • | • |
| | | | | | 1 | 0 | 0 | 0 dB |
| | | | | | • | • | • | • |
| | | | | | 0 | 0 | 0 | -4 dB |

MEMO