PRELIMINARY

Dolby Pro Logic Surround Processor

DOLBY SURROUND PRO • LOGIC

Description

The NJU25005 is a digital surround processor which decodes Dolby Pro Logic surround signals and generates simulated surround sound. It consists of a 24-bit fixed point digital signal processor, internal memory (ROM and RAM), interface circuits, and other logic necessary to implement a true digital surround sound decoder. The NJU25005 incorporates all functions of Dolby Pro Logic using high quality digital signal processing techniques. It can also easily create various kinds of surround sound in the simulated surround mode, generating soundfields by using optional external memory to digitally implement larger delays.

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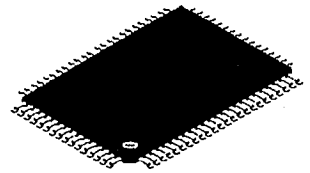

Plastic QFP-80

Features

- Dolby Pro Logic Surround Decoding
  - 24-bit fixed point Digital Signal Processing
  - On-Chip Digital Delay, 30ms Max.
  - No External Memory Required
  - Dolby 3 Stereo Mode
  - Internal Auto Input Balance
- Soundfield Simulation Modes
  - Hall Effect Built-in
  - Custom Modes Downloadable
  - Digital Delay (1.5s max) Using External Memory
  - Stereo, Full Bandwidth Widefield Surround
  - Supports External SRAM and DRAM
- Mono-to-Stereo Synthesis
- 16- or 18-bit External A/D and D/A Converters
- Serial Digital Audio Converter Interface
  - I^2S, Left and Right Justified Data Modes
  - Programmable MCK, SCK Outputs
  - Master and Slave Modes
- Serial or Parallel Command Control Interface
- Operates from a Single +5V Supply
- Evaluation Board Available
- No DSP Design Required

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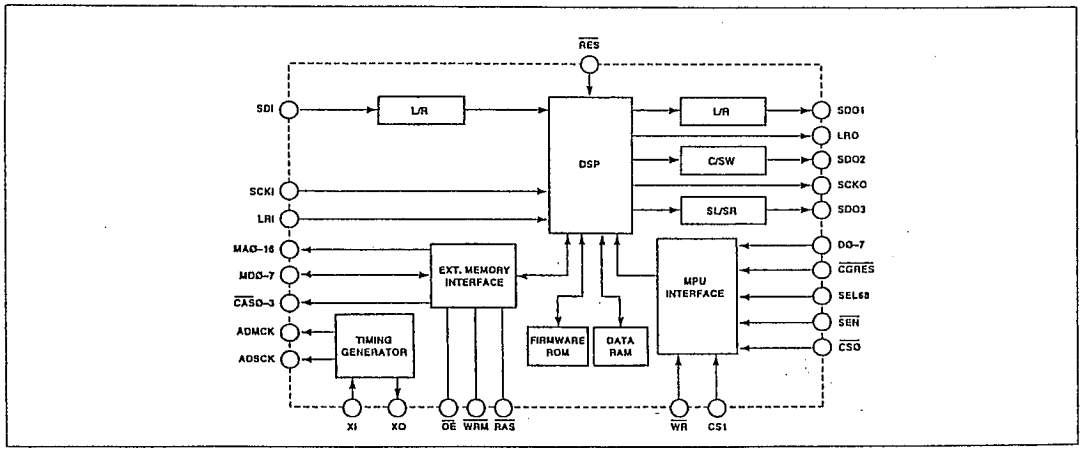
Figure 1. Block Diagram



Pin Configuration

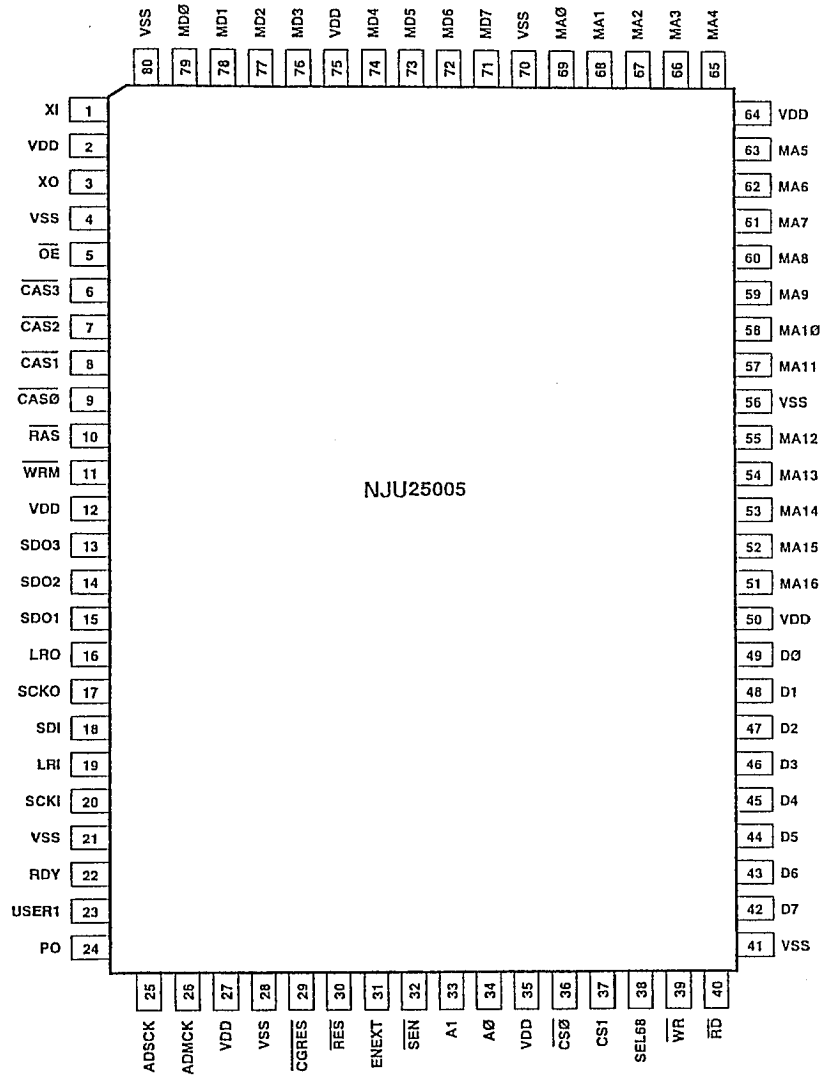


Figure 2.NJU25005 PIN CONFIGURATION

Pin Description

No.	Symbol	I/O	Function
1	XI	I	Crystal/External clock input
2	VDD	I	Power supply, +5V
3	XO	O	Crystal
4	VSS	I	Ground
5	$\overline{OE}$	O	External memory output enable
6	$\overline{CAS3}$	O	External memory column address strobe
7	$\overline{CAS2}$	O	External memory column address strobe
8	$\overline{CAS1}$	O	External memory column address strobe
9	$\overline{CAS0}$	O	External memory column address strobe
10	$\overline{RAS}$	O	External memory row address strobe
11	$\overline{WRM}$	O	External memory write enable, Low to write data
12	VDD	I	Power supply, +5V
13	SDO3	O	Digital audio serial data out, surround right and left
14	SDO2	O	Digital studio serial data out, center and subwoofer
15	SDO1	O	Digital audio serial data out, front right and left
16	LRO	O	Left/Right frame clock output
17	SCKO	O	Digital audio serial clock output
18	SDI	I	Digital audio serial data input
19	LRI	I	Left/Right frame clock input
20	SCKI	I	Digital audio serial clock input
21	VSS	I	Ground
22	RDY	I	Test pin, high for normal operation
23	USER1	I	Test pin, low for normal operation
24	PO	O	Test pin
25	ADSCK	O	32Fs/64Fs serial clock for A/D, D/A converters (default 32Fs)
26	ADMCK	O	384Fs/256Fs master clock for A/D, D/A converters (default 384Fs).
27	VDD	I	Power supply, +5V
28	VSS	I	Ground
29	$\overline{CGRES}$	I	ACK reset terminal for TEST, normally high when not used
30	$\overline{RES}$	I	Reset, must be held low for at least two clock cycles after power on.
31	ENEXT	I	Test pin
32	$\overline{SEN}$	I	MPU serial interface enable. Serial: L, parallel: H
33	A1	I	Test pin. Low for normal operation
34	A0	I	Test pin. Low for normal operation
35	VDD		Power supply, +5
36	$\overline{CS0}$	I	Chip select, MPU interface enabled when CS0 = 0 and CS1 = 1.
37	CS1	I	Chip select, MPU interface enabled when CS0 = 0 and CS1 = 1.
38	SEL68	I	MPU interface mode: 68K-H, Z80-L
39	$\overline{WR}$	I	Write Strobe (Z80), Write Enable (68K)
40	$\overline{RD}$	I	Write Strobe (68K)

Pin Description (Continued)

No.	Symbol	I/O	Function
41	VSS	I	Ground
42	D7	I	MPU data, parallel input (MSB)
43	D6	I	MPU data, parallel input
44	D5	I	MPU data, parallel input
45	D4	I	MPU data, parallel input
46	D3	I	MPU data, parallel input
47	D2	I	MPU data, parallel input
48	D1	I	MPU data, parallel input
49	DØ	I	MPU data, parallel input (LSB), serial data input (SEN = Ø)
50	VDD	I	Power supply, +5V
51	MA16	O	External memory address (MSB)
52	MA15	O	External memory address
53	MA14	O	External memory address
54	MA13	O	External memory address
55	MA12	O	External memory address
56	VSS	I	Ground
57	MA11	O	External memory address
58	MA1Ø	O	External memory address
59	MA9	O	External memory address
60	MA8	O	External memory address
61	MA7	O	External memory address
62	MA6	O	External memory address
63	MA5	O	External memory address
64	VDD	I	Power supply terminal: +5V
65	MA4	O	External memory address
66	MA3	O	External memory address
67	MA2	O	External memory address
68	MA1	O	External memory address
69	MAØ	O	External memory address (LSB)
70	VSS	I	Ground
71	MD7	O	External memory data (MSB)
72	MD6	O	External memory data
73	MD5	O	External memory data
74	MD4	O	External memory data
75	VDD	I	Power supply terminal: +5V
76	MD3	O	External memory data
77	MD2	O	External memory data
78	MD1	O	External memory data
79	MDØ	O	External memory data (LSB)
80	VSS	I	Ground

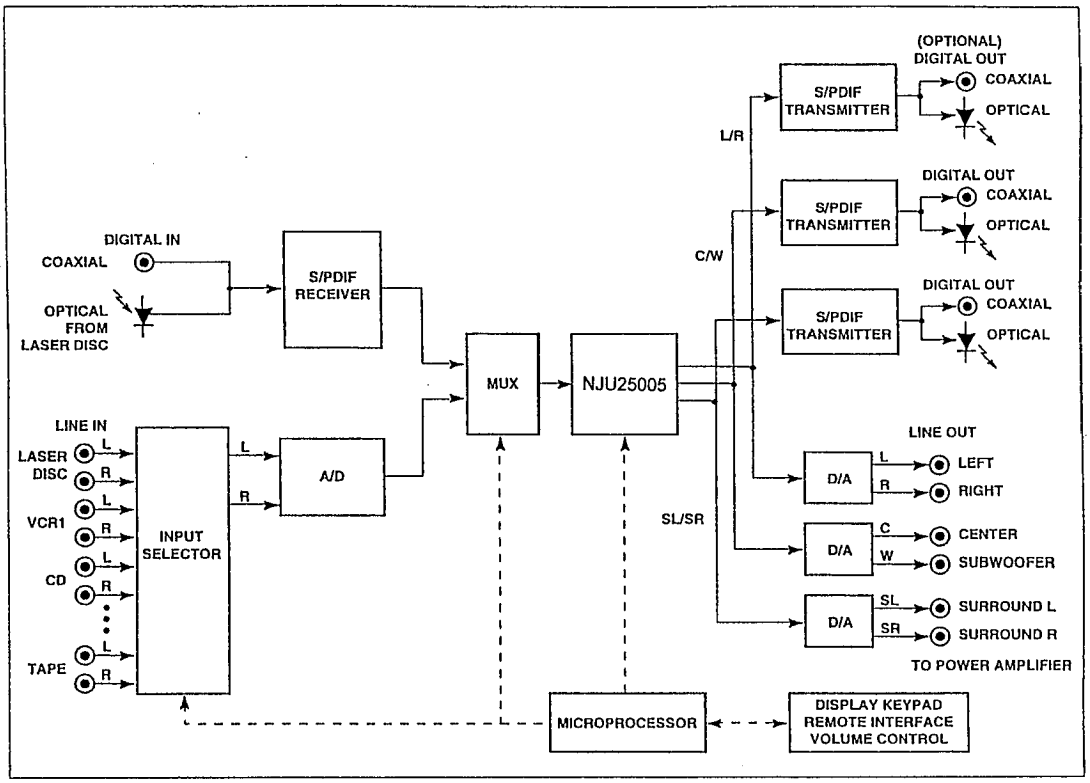
Absolute Maximum Ratings (V_{SS} = 0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage (T_A = 25°C)	V_{DD}	−0.3	7	V
Input, Output Pin Voltage (T_A = 25°C)	V_X	−0.3	V_{DD} + 0.3	V
Operating Temperature	t_{OPR}	−20	70	°C
Storage Temperature	t_{STG}	−55	125	°C

Electrical Characteristics (V_{DD} = 5V, T_A = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	V_{DD} pins	4.75		5.25	V
Operating Current	I_{DD}	f_{OSC} = 36.9MHz		90	125	mA
High Level Input Voltage	V_{IH}		0.80V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		V_{SS}		0.20V_{DD}	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD}	−1		+1	µA
Low Level Input Current	I_{IL}	V_{IN} = V_{SS}	−1		+1	µA
High Level Output Voltage	V_{OH}	I_{OH} = 500µA	V_{DD}−0.5			V
Low Level Output Voltage	V_{OL}	I_{OL} = 500µA			0.5	V
Input capacitance	C_{IN}			10	20	pF
Clock Frequency	f_{OSC}		20		40	MHz
Ext. System Clock Duty Cycle	r_{EC}		45		55	%

Figure 3. Typical Dolby Pro Logic System



Clock Generator

The NJU25005 with a 768Fs crystal wiring to XI and XO terminals generates signals to operate the internal circuits and signals to external circuits, or inputting external clock (768Fs) to XI terminal is also available. 32kHz, 44.1kHz, or 48kHz can be used as Fs frequency. The output signal of ADMCK terminal is selective of 384Fs or 256Fs on user's command. The output signal of ADSCK is also selective of 32Fs or 64Fs on user's command.

(Initial conditions are 384Fs and 32Fs, respectively.)

Functional Description

Digital Audio Data Interface

Three digital audio data formats are supported: left justified, right justified, and I²S. The data is always MSB first, 2's complement. Either 16-bit or 18-bit data can be accommodated. The polarity of the L/R clocks (LRI, LRO) is programmable along with the active edge of the serial bit clocks (SCKI, SCKO). A master clock (ADMCK) and serial bit clock (ADSCK) output for the A/D and D/A converters are provided by an internal, programmable clock generator for synchronous operation with the DSP clock (768Fs). Asynchronous data rates are possible as long as the output is slaved to the input and it is close to the three supported sampling frequencies (32kHz, 44.1kHz, and 48kHz).

There is one stereo digital audio input and three stereo digital audio outputs for L and R main channel, L and R surround, Center, and Subwoofer. All three serial data outputs must have identical data formats. In each data format mode, SCLK and LRCLK polarities are independently programmable for input and output. Audio data width (16/18 bits), SCK and MCK frequencies (32/64Fs, 256/384Fs, respectively) must be the same for both input and output.

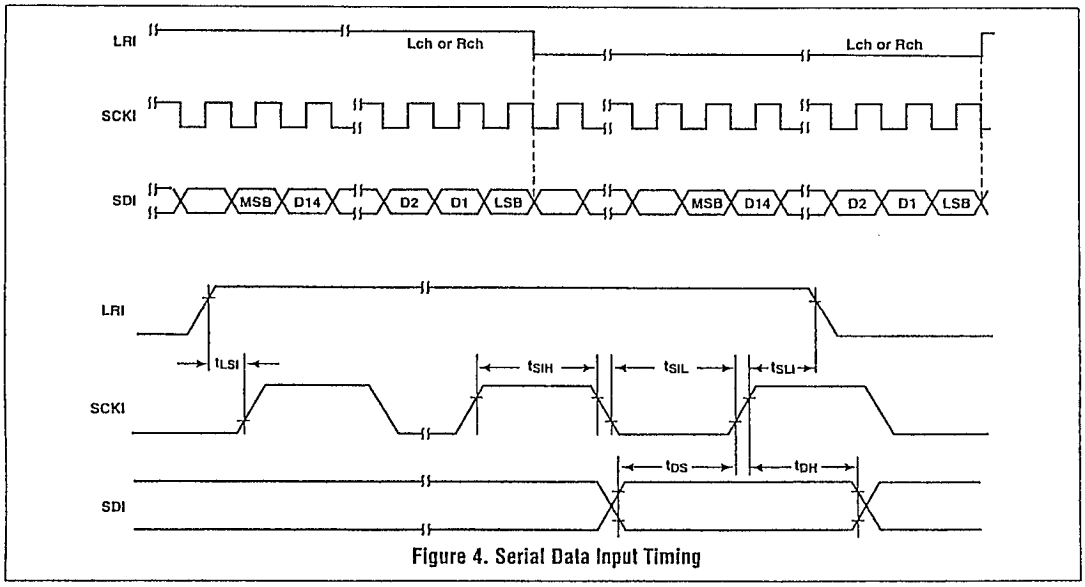


Figure 4. Serial Data Input Timing

Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, f_{CLK} = 34MHz)

Serial Data Input

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SCKI Period			160			ns
L Pulse Width	t_{SIL}		80			ns
H Pulse Width	t_{SIH}		80			ns
SCKI to LRI Time	t_{SLI}		30			ns
LRI to SCKI Time	t_{LSI}		75			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns

Serial Data Formats

There are three serial data formats supported for interfacing an A/D and three D/A's to the digital audio interface. Either Left Justified, Right Justified or I^2S mode is selected by FMT0 and FMT1 bits in the second byte of the three-byte System State Download Command. In Left Justified Mode, the MSB is aligned to the edge of LRI or LRO. The data is positioned at the left or "front" side of the L/R pulse (Fig. 6). In Right Justified Mode, the LSB is aligned to the LRI or LRO edge. The data is at the right or "rear" of the L/R pulse (Fig. 7). Sometimes this mode is called Japanese Mode or EIAJ Mode. The I^2S Mode is similar to Left Justified Mode, except that the data is delayed one SCLK period and the sense of LRI and LRO is inverted (Fig. 8). In I^2S Mode, the LRI and LRO are low for left channel data and high for right channel data, normally opposite of other modes. The polarity of LRI and LRO can be inverted independently in any mode by the use of the LRI and LRO.

Normally, the serial data bits generated by a source change on the falling edge of the serial clock so that they can be easily clocked into a shift register on rising clock edge. Considering an A/D as the source and the NJU25005 as a destination, the default setting is to clock the serial data input, SDI, in on the rising edge of SCKI. This can be changed to clock data in on the falling edge using the SCKI bit in the System Download Command.

For the output serial data, the NJU25005 is considered the source and the D/A's are considered the destination. The default interface setting is for data to be clocked out of SDO on the falling edge of SCKO so that the D/A clocks data in on the rising edge. This can be changed as well independently of the input and interface mode using the SCKO bit in the System Download Command.

The MS bit in the second System State Download Command byte selects either Master Mode or Slave Mode. In Right Justified Mode, Master Mode (MS = 0) is defined such that SCKO, the serial data clock to the D/A's, is generated from an internal divider derived from the 768Fs DSP clock (Xi). In Slave Mode (MS = 1) the serial data clock to the D/A's is a copy of the serial data clock on the input, SCKI, from the A/D. This mode should be used for asynchronous data rates, such as data from an S/PDIF receiver connected to the Digital

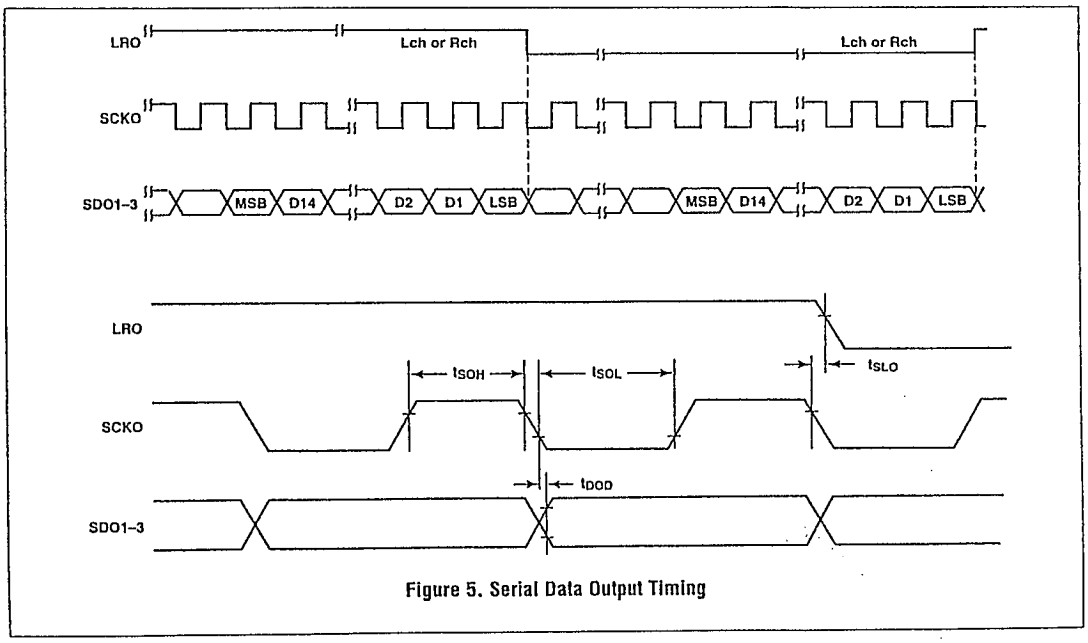


Figure 5. Serial Data Output Timing

Output from a laser disc player. When an A/D is used with analog inputs, its master clock should be synchronous to the NJU25005 using ADMCK at 256Fs or 384Fs. In this case either Master Mode or Slave Mode will work. The default setting is Master Mode (MS = 0).

In I^2S Mode, Master and Slave modes have slightly different meaning, which is closer to the conventional definitions associated with A/D and D/A converters. Considering the NJU25005 point of reference, Slave Mode (MS = 1) is defined in this case as LRI and SCKI are *inputs from* the A/D. This means that the A/D must be in Master Mode with L/R and SCLK *outputs*. Conversely, when the NJU25005 is in Master Mode (MS = 0), the LRI and SCKI are *outputs* which drive the L/R and SCLK inputs of an A/D operating in slave mode. The SCKO and LRO to the D/A's are always *outputs*. The D/A converters, therefore can only run in Slave Mode expecting both the L/R and SCLK from the NJU 25005. As in Right Justified mode, LRO and SCKO are derived from the 768Fs DSP clock. When slave mode is selected, LRO and SCKO are generated by the LRI and SCKI inputs. Slave mode should be used for asynchronous audio data.

In the third mode, Left Justified Mode, only Slave Mode (MS = 0) is allowed. The A/D is required to be in Master Mode supplying the LRI and SCKI clocks to the NJU25005 inputs. The LRO and SCKO are generated from the LRI and SCKI inputs.

In each data format mode the serial clock frequency for SCKI and SCKO can be selected using ADSCK in the System Download Command to be either 32Fs (32-bit clocks per sample) or 64Fs (64-bit clocks per sample). Both SCKI and SCKO must be the same frequency. This clock is generated internally for use on the SCKI and SCKO pins (Master Mode), but is also available as a separate output on a pin called ADSCK. It is derived from the 768Fs Input Clock to the NJU25005.

If SCKI and SCKO are selected to be 32Fs, the data length must be set to 16-bits (BL = 0) since a stereo pair of 16-bit channels needs all 32 clocks per sample. In this case, both Left and Right Justified Modes look exactly the same (Fig. 9), and either mode setting will work. In I^2S mode the data bits appear shifted by one SCLK and the L/R is inverted (Fig. 10).

An output clock, ADMCK, is derived from the NJU25005 768Fs Input Clock for use as an A/D or D/A master clock. ADMCK is set to 256Fs or 384Fs using the ADMCK bit in the System Download Command.

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Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, f_{CLK} = 34MHz)

Serial Data Output

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SCKO Period		C_L: LRO, SCKO, SDO = 5pF	160			ns
L Pulse Width	t_{SOL}		80			ns
H Pulse Width	t_{SOH}		80			ns
SCKO to LRO Time	t_{SLO}				5	ns
Data Output Delay	t_{DOD}				5	ns

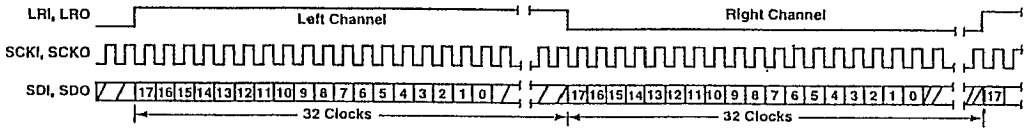

Figure 6. Left justified data format, ADSCK = 64Fs, 18-bit data

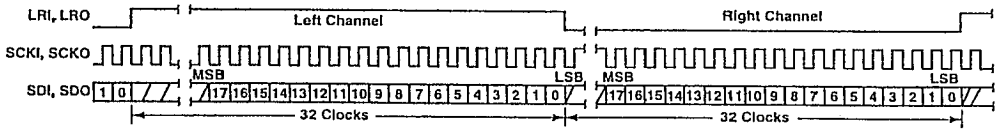

Figure 7. Right justified data format, ADSCK = 64Fs, 18-bit data

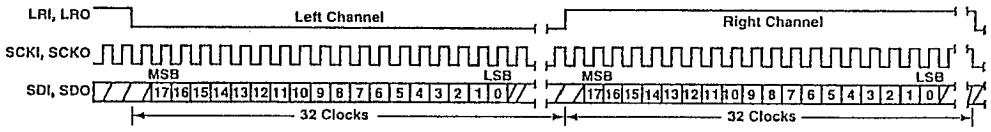

Figure 8. I²S data format, ADSCK = 64Fs, 18-bit data

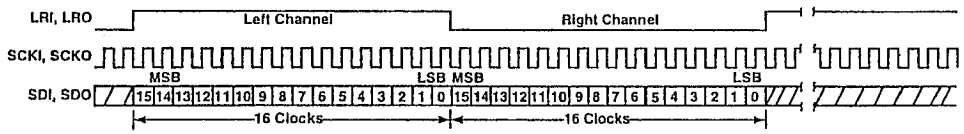

Figure 9. Either Right or Left Justified data formats, ADSCK = 32Fs, 16-bit data

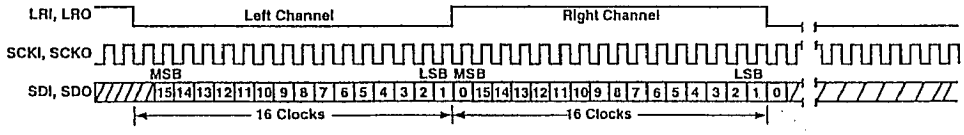

Figure 10. I²S data format, ADSCK = 32Fs, 16-bit data

Microcontroller Interface

Either a Z80 or 68K type microcontroller can be used to download commands to the NJU25005. SEL68 must be set high for 68K and low for Z80. Either serial or 8-bit parallel interface modes may be used, depending on $\overline{SEN}$ input (L:serial; H:parallel). The MPU interface is enabled when $\overline{CS0}$ = Ø AND CS1 = 1, allowing a control signal of either polarity to be used.

The audio stops when NJU25005 receives a System State Download Command, when Simulated Surround Mode coefficients are downloaded, or when the Noise Sequencer is turned on. All other commands take immediate effect without interruption in the audio. Only one command should be sent from the microprocessor per L/R period. The DSP in the NJU25005 spends most of the time processing audio, during which time microprocessor interrupts are disabled. Writing to the MPU interface sets an interrupt request flag inside the chip and holds the data in a register which is read as soon as the interrupt can be serviced. Successive writes to the MPU interface while the interrupts are disabled will overwrite the previous contents. There is a window of time in each audio sample when it is possible to service several MPU commands. However, there is no way for the microprocessor to determine how long this window is before the audio interrupt arrives and successive MPU writes will be lost. Therefore, when audio is being processed, it is recommended that only one command be sent to the NJU25005 for each audio sample, even though the logic will accept parallel writes up to 1 Mbyte per second. When the audio is interrupted, as in the System State Download Command or when Simulated Surround coefficients are being transferred, data can be transferred at the maximum data rate, with at least 1µs between bytes written to the NJU25005.

The MPU interface was designed for both read and write operations. However, the DSP firmware only supports write operations.

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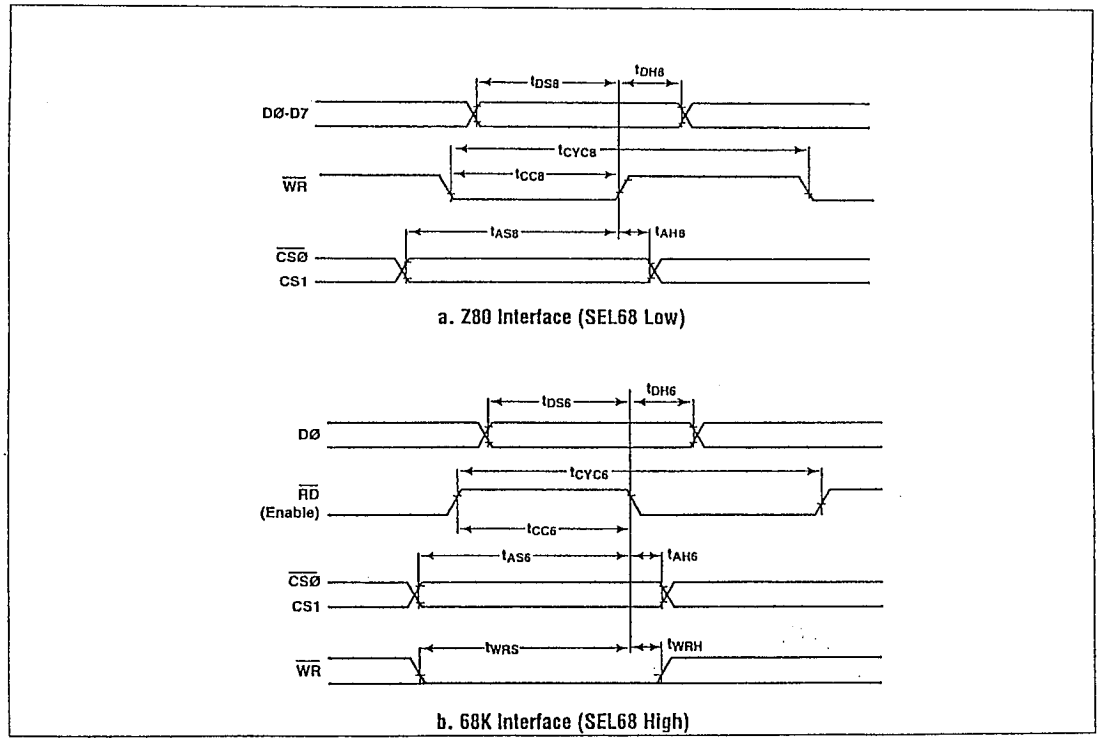

Figure 11. Parallel Interface Timing

Parallel Interface

Z80 Mode

Writing commands to the NJU25005 from a Z80 type microprocessor is accomplished by setting SEL68 low, placing data on the input data port, DØ to D7, setting the chip selects, and strobing $\overline{WR}$ low then high. Successive writes, as in the three-byte System Download Command, can be done without resetting the chip select(s). It is recommended to return the Chip Select to the inactive state as soon as the command is sent. The recommended sequence for writing parallel data to the NJU25005 is:

1. Set $\overline{RD}$ high (can be tied to V_{CC}).
2. Place data on the data port, D0:7.
3. Assert chip selects, ($\overline{CS0}$ = Ø AND CS1 = 1). One can be permanently tied to its active state, while the other is controlled.
4. Strobe $\overline{WR}$ low, then high.
5. De-activate chip selects.
6. Wait at least one audio sample before sending another command.

68K Mode

In 68K mode (SEL68 High) $\overline{RD}$ acts as a strobe for both read and write operations. $\overline{WR}$ defines whether a read or write is to be performed (L:write to NJU25005; H:there is no provision for reading from NJU25005). Since only write operations are allowed, $\overline{WR}$ can be tied low. The recommended sequence to write parallel data to the NJU25005 in this mode is:

1. Set $\overline{WR}$ low (can be tied to GND).
2. Place data on the data port, D0:7.
3. Assert chip selects, ($\overline{CS0}$ = Ø AND CS1 = 1). One can be permanently tied to its active state, while the other is controlled.
4. Strobe $\overline{RD}$ high, then low.
5. De-activate chip selects.
6. Wait at least one audio sample before sending another command.

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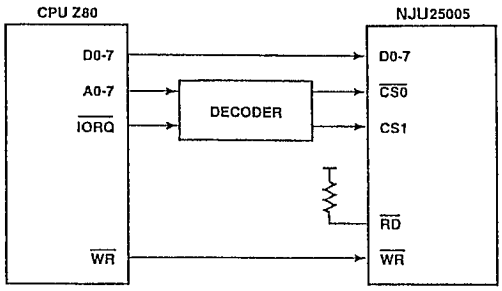
Z80 Interface Timing

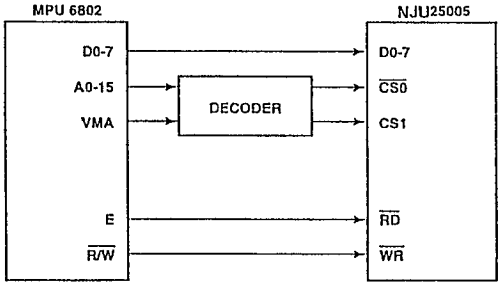
Parameter	Symbol	Condition	Min.	Max.	Unit
Address Setup Time	t_{AS8}		100		ns
Address Hold Time	t_{AH8}		100		ns
System Cycle Time	t_{CYC8}		1,000		ns
Read/Write Pulse Width	t_{CC8}		100		ns
Write Data Setup Time	t_{DS8}		10		ns
Write Data Hold Time	t_{DH8}		10		ns

68K Interface Timing

Parameter	Symbol	Condition	Min.	Max.	Unit
Address Setup Time	t_{AS6}		100		ns
Address Hold Time	t_{AH6}		100		ns
System Cycle Time	t_{CYC6}		1,000		ns
Read/Write Pulse Width	t_{CC6}		100		ns
Write Data Setup Time	t_{DS6}		10		ns
Write Data Hold Time	t_{DH6}		10		ns
Write-to-read Strobe Setup	t_{WRS}		100		ns
Read-to-write Strobe Setup	t_{WRH}		100		ns



12a. Z80 Interface



12b. 68K Interface

Serial Interface

In serial interface mode ($\overline{SEN}$ = Ø), DØ is used for the serial data input. Two types of interface modes are supported. In Z80 mode (SEL68 low) $\overline{WR}$ is used as a serial bit clock. In 68K mode (SEL68 high), $\overline{RD}$ is used to clock the serial data. Data is clocked in 8 bits at a time with a maximum data rate of 1MHz. As in Parallel Mode, above, it is recommended that only one command be sent per audio sample while audio is playing. For commands which cause the audio to stop, data can be written to the microprocessor interface at the maximum bit rate of 1MHz (and 1µs between bytes).

Z80 Mode

When using a microprocessor with a Z80 type interface, writing serial data to the NJU25005 is done by clocking the data in on rising edges of the $\overline{WR}$, with $\overline{RD}$ held high (SEL68 = Ø). The recommended sequence is:

1. Set $\overline{SEN}$ = Ø.
2. Assert chip selects, ($\overline{CSØ}$ = Ø AND CS1 = 1).
3. Set $\overline{RD}$ high.
4. Clock in serial data with $\overline{WR}$ (rising edge).
5. De-activate chip selects.
6. Wait 1 audio sample before sending next byte (1µs if audio stopped).

68K Mode

For 68K type microprocessors, the function of $\overline{RD}$ and $\overline{WR}$ is opposite of Z80. Writing serial data to the NJU25005 is done by setting $\overline{WR}$ low and clocking the data in on rising edges of $\overline{RD}$ (SEL68 = 1). The recommended sequence is:

1. Set $\overline{SEN}$ = Ø
2. Assert chip selects, ($\overline{CSØ}$ = Ø and CS1 = 1).
3. Set $\overline{WR}$ low.
4. Clock in serial data with $\overline{RD}$ (falling edge).
5. De-activate chip selects.
6. Wait 1 audio sample before sending next byte (1µs if audio stopped).

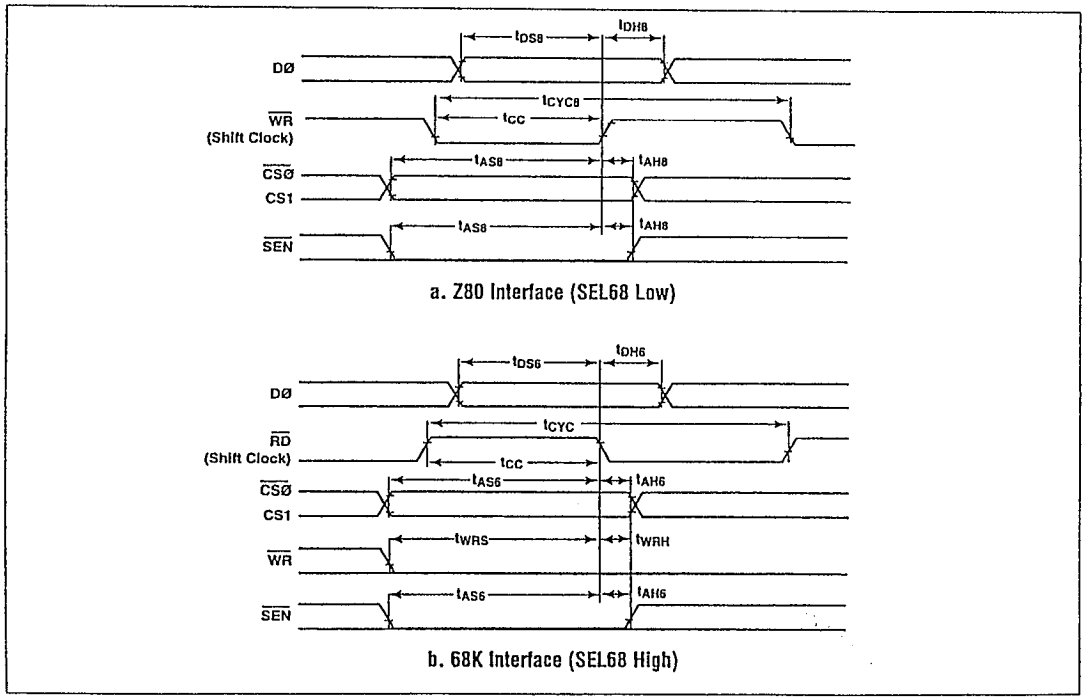


Figure 13. Serial Interface Timing

External Memory Interface

An external delay memory is used with the NJU25005 to implement effects in Simulated Surround mode. Memory size requirements are dictated by maximum soundfield coefficient settings. See Simulation Surround mode section for details.

The NJU25005 interfaces to a wide range of memory devices. External memory can be SRAM or DRAM with either 4-bit or 8-bit wide data ports. The NJU25005 translates between an external memory data path of 4-bits or 8-bits and the 16-bit wide internal data bus. From one to four memory devices can be connected.

Figure 14 shows a single 1Mbit DRAM device connected to the NJU25005. Figures 15 show examples of connecting single 256kbit and 1Mbit SRAM devices to the NJU25005. Figure 16 shows connection of two 256kbit SRAM devices, which can be extended by example to the case of connecting three or four memory devices by using $\overline{CAS2}$ and $\overline{CAS3}$ pins.

Access time of RAM must be 100ns or less. Fast Page mode capability is not required for DRAM devices.

Settings of System State Download bits for Memory connection examples

Figure	Memory Devices	Memory Configuration	System State Down Load bits MSIZE1	MSIZE0	MTYPE	MWIDE
14	1	1Mbit (256k x 4) DRAM	0	1	0	0
15	1	1Mbit (128k x 8)SRAM	1	0	1	1
	1	256kbit (32k x 8)SRAM	0	1	1	1
16	2	256kbit (32k x 8)SRAM	0	1	1	1

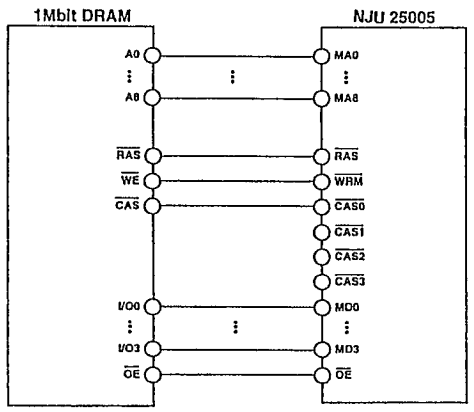
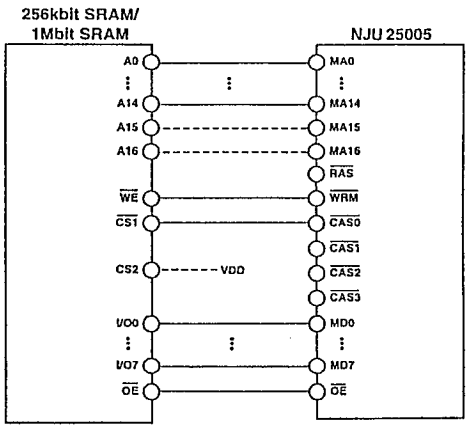


Figure 14. Single DRAM Connecting Device toNJU25005



Note: Dotted line indicates connections for 1Mbit SRAM device only.

Figure 15. Connecting single SRAM device toNJU25005

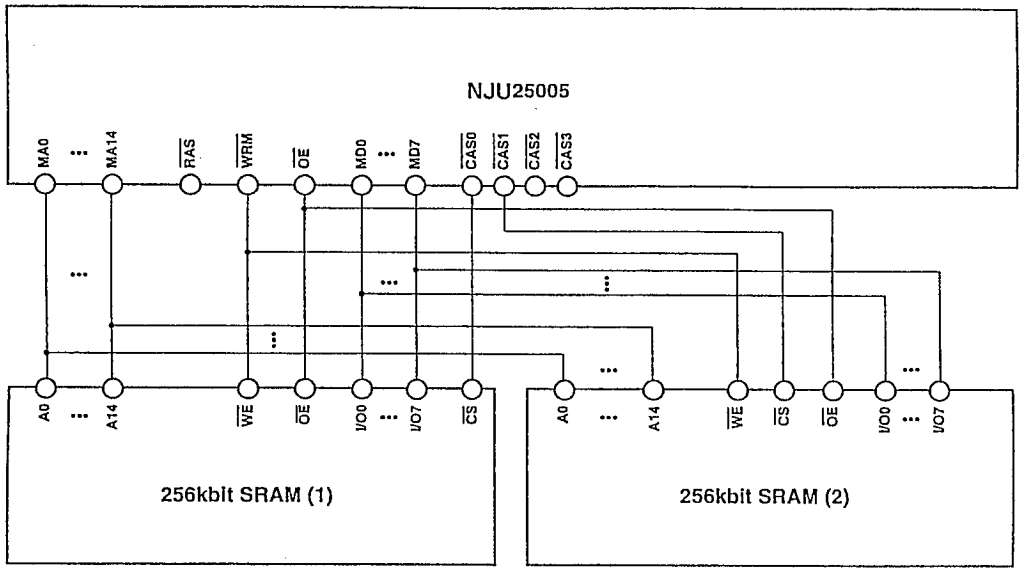


Figure 16. Connecting multiple memory devices toNJU25005

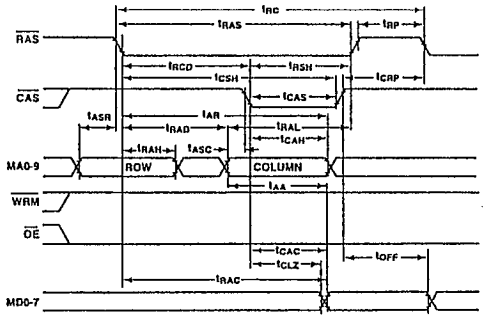


Figure 17. DRAM Read Cycle Timing

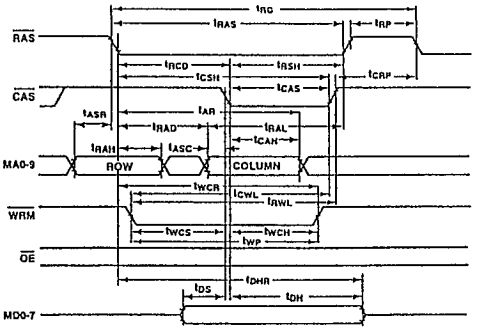
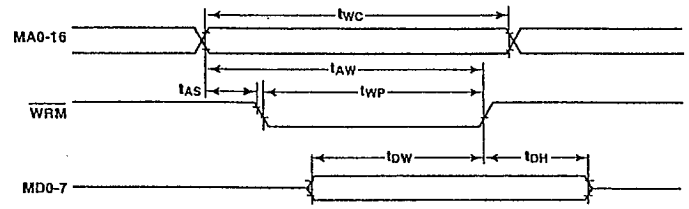


Figure 18. DRAM Write Cycle Timing

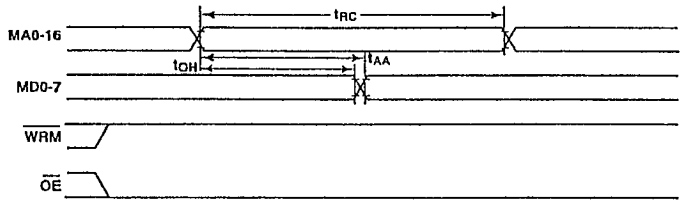
Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, f_{CLK} = 34MHz, C_L = 70pF)

DRAM Interface Timing

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Read Cycle	t_{CYC1}				20,000	ns
Write Cycle	t_{CYC2}				1,000	ns
Random Read or Write Cycle Time	t_{RC}		200			ns
Access Time from $\overline{RAS}$	t_{RAC}				100	ns
Access Time from $\overline{CAS}$	t_{CAC}				40	ns
Access Time from Column Address	t_{AA}				50	ns
$\overline{CAS}$ to Output Low Impedance	t_{CLZ}		0			ns
Output Buffer Turn-off Delay	t_{OFF}		0			ns
$\overline{RAS}$ Precharge Time	t_{RP}		100			ns
$\overline{RAS}$ Pulse Width	t_{RAS}		100			ns
$\overline{RAS}$ Hold Time	t_{RSH}		40			ns
$\overline{CAS}$ Hold Time	t_{CSH}		100			ns
$\overline{CAS}$ Pulse Width	t_{CAS}		40			ns
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}		40			ns
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}		30			ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}		100			ns
Row Address Setup Time	t_{ASR}		0			ns
Row Address Hold Time	t_{RAH}		25			ns
Column Address Setup Time	t_{ASC}		0			ns
Column Address Hold Time	t_{CAH}		30			ns
Column Address Hold Time form $\overline{RAS}$	t_{AR}		90			ns
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}		50			ns
Write Command Hold Time	t_{WCH}		40			ns
Write Command Hold Time from $\overline{RAS}$	t_{WCR}		90			ns
Write Command Pulse Width	t_{WP}		70			ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}		70			ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}		70			ns
Data-In Setup Time	t_{DS}		0			ns
Data-In Hold Time	t_{DH}		40			ns
Data-In Hold Time Reference to $\overline{RAS}$	t_{DHR}		100			ns
Write Command Setup Time	t_{WCS}		10			ns



SRAM WRITE Cycle Timing



SRAM READ Cycle Timing

Figure 19. Timing Diagrams

Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, f_{CLK} = 34MHz, C_L = 70pF)

SRAM Interface Tming

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}		200			ns
Address Access Time	t_{SAA}				200	ns
Output Hold from Address Change	t_{OH}		10			ns
Write Cycle Time	t_{WC}		200			ns
Address Setup Time	t_{AS}		10			ns
Address valid to End of Write	t_{AW}		150			ns
Write Pulse Width	t_{WP}		100			ns
Data to Write Time Overlap	t_{DW}		60			ns
Data Hold from Write Time	t_{DH}		10			ns

Microcontroller Commands

Configuration

System State Down Load (3 Bytes)

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Download Command, byte 1

7	6	5	4	3	2	1	0		
MODE1	MODE0	MS	BIO	LRI	SCKI	LRO	SCKO	Download Data, byte 2	
							0	⌐‾_	Data changes on falling edge*
							1	_/‾¬	Data changes on rising edge
						0		L R	Left:high; right:low*
						1		L R	Left:low; right:high
					0			_/‾¬	Data latches on rising edge*
					1			⌐‾_	Date latches on falling edge
				0				L R	Left:high; right:low*
				1				L R	Left:low; right:high
			0					16-bits*	Data width 16-bits
			1					18-bits	Data width 18-bits
0	0	0						Right justified*	Master mode*
0	0	1						Right justified	Slave mode
1	0	0						I^2S	Master mode
1	0	1						I^2S	Slave mode
1	1	1						Left justified	Slave mode

7	6	5	4	3	2	1	0		
ADMCK	ADSCK	MTYPE	MSIZE1	MSIZE0	MWIDE	0	0	Download Data, byte 3	
						0	0	Reserved	
					0			4-bits*	Ext. memory width
					1			8-bits	
			0	0				256K (DRAM)*; 64K (SRAM)	Ext.
			0	1				1M (DRAM); 256K (SRAM)	memory
			1	0				4M (DRAM); 1M (SRAM)	size
		0						DRAM	Ext. memory type
		1						SRAM	
	0							32Fs*	A/D-D/A SCLK
	1							64Fs	
0								384Fs*	A/D-D/A MCLK
1								256Fs	

* Default values

Sampling Frequency

7	6	5	4	3	2	1	0
0	0	0	1	0	FS1	FS0	0

		Reserved	
0	0	32kHz	Sample Rate
0	1	44.1kHz*	
1	0	48kHz	

Noise Sequencer

7	6	5	4	3	2	1	0
0	0	1	0	0	NS	NCH1	NCH0

	0	0	Left* Channel
	0	1	Center
	1	0	Right
	1	1	Surround
0			OFF* Noise Sequencer
1			ON

4

Auto Input Balance

7	6	5	4	3	2	1	0
0	1	0	0	IBL	0	0	0

	Reserved	
0	OFF	Auto Balance
1	ON*	

Operating Mode

7	6	5	4	3	2	1	0
0	0	0	1	1	OP1	OP0	0

		Reserved
0	0	Dolby Pro Logic*
0	1	Simulated Surround
1	0	Simulated Stereo
1	1	Surround OFF (Normal stereo)

Surround Mode

7	6	5	4	3	2	1	0
0	0	1	1	1	SM	WFS	0

		Reserved	
	0	OFF*	Widefield Surround
	1	ON	
0		Front Surround	
1		Rear Surround*	

* Default values

Center Mode

7	6	5	4	3	2	1	0
0	0	1	1	0	CM1	CM0	CTR

		0	OFF	Center Channel
		1	ON*	
0	0		ON (Normal)*	Center Mode
0	1		Phantom	
1	0		Wide Band	

Balance

7	6	5	4	3	2	1	0
0	1	1	BAL4	BAL3	BAL2	BAL1	BAL0

0	1	1	1	1	0.0dB	−7.5dB	Min. Right
0	1	1	1	0	0.0dB	−7.0dB	
			⋮			⋮	
0	0	0	0	1	0.0dB	−0.5dB	
0	0	0	0	0	0.0dB	0.0dB	Center*
1	1	1	1	1	−0.5dB	0.0dB	
			⋮			⋮	
1	0	0	0	1	−7.5dB	0.0dB	
1	0	0	0	0	−8.0dB	0.0dB	Min. Left

Surround Trim

7	6	5	4	3	2	1	0
1	CH1	CH0	TR4	TR3	TR2	TR1	TR0

		0	0	0	0	0	0dB*	Level	
		0	0	0	0	1	−1dB		
		0	0	0	1	0	−2dB		
					⋮				
		1	1	1	1	0	−30dB		
		1	1	1	1	1	−31dB		
0	0						Center	Channel	
0	1						Surround		
1	0						Subwoofer		

Surround Delay Time

7	6	5	4	3	2	1	0
0	1	0	1	DLY3	DLY2	DLY1	DLY0

1	1	1	1	30 msec	Delay Time
1	1	1	0	29 msec	
		⋮			
0	1	0	1	20 msec*	
		⋮			
0	0	0	1	16 msec	
0	0	0	0	15 msec	

* Default values

Simulated Surround Mode

The soundfield simulator digitally simulates the effect of multiple acoustic echos which are present in large listening spaces such as a concert hall or theatre. These electronic echos are added to the Center channel and Surround channel out puts to create the illusion of a large listening space. The DSP architecture of the NJU25005 allows a wider range of complex soundfield effects to be simulated than is possible with most analog architectures. A pre-loaded "Hall Effect mode" soundfield can be selected, or custom sound fields can be implemented by downloading coefficients via the microprocessor interface.

Figure 20. illustrates how the NJU25005 adds soundfield effects to the center and surround channels. Details of the Soundfield Generators are shown in Figure 21.

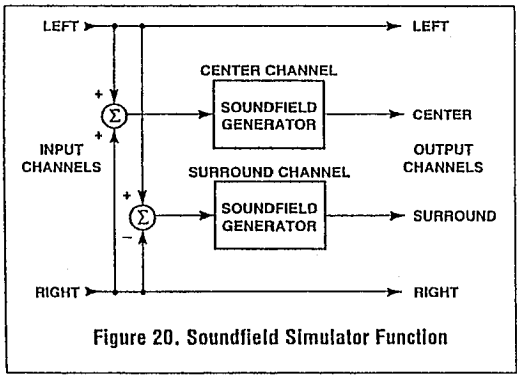


Figure 20. Soundfield Simulator Function

Nine coefficients and four switch settings define the behavior of each of the two Soundfield Generators for center and surround channels. These coefficients can be preset to values for "Hall" mode surround. Alternatively, custom coefficients can be loaded to design any sedireds ound field characteristics.

Hall Effect Mode

Soundfield coefficients for the built-in Hall Effect mode are loaded by issuing th following command when the Operating Mode is set to Simulated Surround (OP1, Ø = Ø1):

Hall Mode Command

7	6	5	4	3	2	1	Ø
Ø	1	Ø	1	Ø	Ø	Ø	Ø

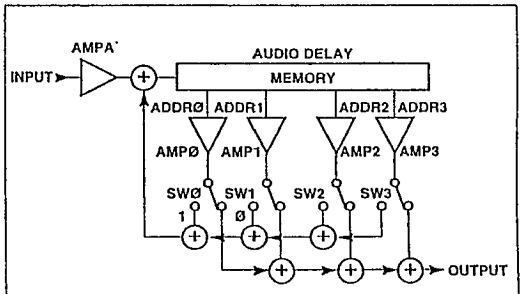


Figure 21. Soundfield Generator and Coefficients

Downloading Soundfield Simulation Coefficients (39 bytes)

This command sequence downloads the complete set of soundfield coefficients for both center and surround channels when the Operating Mode is set to Simulated Surround Mode (OP1, Ø = Ø1). These soundfield coefficients control the functions identified in Figure 21. The following command code initiates the download sequence written to the microprocessor interface. Asserting hardware reset ($\overline{RES}$ = Ø) or selecting Hall Effect (command 50H) will reload all the soundfield coefficients with values for Hall mode. Previously downloaded coefficients are lost.

Command Sequence:

Initiate Download Command

7	6	5	4	3	2	1	Ø
Ø	1	Ø	Ø	Ø	Ø	Ø	Ø

SW0 - SW3 are the switch settings that establish a feedforward or feedback path for each delay tap.

7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	SWØ	SW1	SW2	SW3

ADDR0 – ADDR3 are address values of the four audio delay taps. These addresses correspond to 16-bit audio samples in delay memory. ADDRx is sent as a two byte code with upper byte transferred first. Delay associated with each tap equals the ADDRx setting divided by sample rate, Fs:

Delay (mS) = ADDRx / Fs (kHz).

AMPA, and AMP0 – AMP3 are bipolar gain values. Allowed range is –1 (inverting unity) to +1 (non-inverting unity) for AMPA, and –4 to +4 for AMP0-AMP3. AMPA is coded in a two byte, twos-complement code where 8000(Hex) corresponds to –1 and 7FFF(Hex) corresponds to +1 (0.99997). In the case of AMP0 - AMP3, 8000(Hex) corresponds to –4 and 7FFF(Hex) corresponds to +4 (3.99988). Upper byte of code is transferred first.

Byte	Data	Function
1	40h	Command code
2	SW0-3	Center channel switch settings
		Center channel delay taps:
3	ADDR0	upper byte
4	ADDR0	lower byte
5	ADDR1	upper byte
6	ADDR1	lower byte
7	ADDR2	upper byte
8	ADDR2	lower byte
9	ADDR3	upper byte
10	ADDR3	lower byte
		Center channel gain settings:
11	AMPA	upper byte
12	AMPA	lower byte
13	AMP0	upper byte
14	AMP0	lower byte
15	AMP1	upper byte
16	AMP1	lower byte
17	AMP2	upper byte
18	AMP2	lower byte
19	AMP3	upper byte
20	AMP3	lower byte
21	SW0-3	Surround channel switch settings
		Surround channel delay taps:
22	ADDR0	upper byte
23	ADDR0	lower byte
24	ADDR1	upper byte
25	ADDR1	lower byte
26	ADDR2	upper byte
27	ADDR2	lower byte
28	ADDR3	upper byte
29	ADDR3	lower byte
		Surround channel gain setings:
30	AMPA	upper byte
31	AMPA	lower byte
32	AMP0	upper byte
33	AMP0	lower byte
34	AMP1	upper byte
35	AMP1	lower byte
36	AMP2	upper byte
37	AMP2	lower byte
38	AMP3	upper byte
39	AMP3	lower byte

To program AMPA positive gain values (0.0 to 0.99997):

AMPA = 8000(Hex) x gain setting

To program AMPA negative gain values (–1.0 to –0.00003):

AMPA = 10000(Hex) – [8000(Hex) x gain setting]

Gain Setting	AMPA Data
+0.99997	7FFF
+0.99994	7FFE
⋮	⋮
+0.00003	0001
0.00000	0000
–0.00003	FFFF
⋮	⋮
–0.99997	8001
–1.00000	8000

To program AMP0-AMP3 positive gain values (0.0 to 0.99997):

AMP0-AMP3 = 8000(Hex) x gain setting / 4

To program AMP0-AMP3 negative gain values (–1.0 to –0.00003):

AMP0-AMP3 = 10000(Hex) – [8000(Hex) x gain setting / 4]

Memory Requirements for Soundfield Simulation

The total size of installed memory determines the maximum audio delay addresses (ADDRx) that may be programmed for the center and surround channel soundfield generators. The NJU25005 allocates memory use between center and surround channels as follows:

1) The first 0600(Hex) center channel audio delay addresses are served by on-chip memory. Center channel audio delay addresses above 0600H are served by external RAM.

2) Surround channel audio delay addresses are served entirely by external RAM.

The maximum limits for Center Channel and Surround Channel delay addresses (ADDRx) are determined from total installed RAM bit size as follows:

Max. Center Ch. delay address	≤	RAM/16 = 0600(Hex) – 1
Max. Surround Ch. delay address	≤	RAM/16 – 1
Max. Center Ch. + Surround Ch. delay addresses	≤	RAM/16 + 0600(Hex) – 1

MEMO