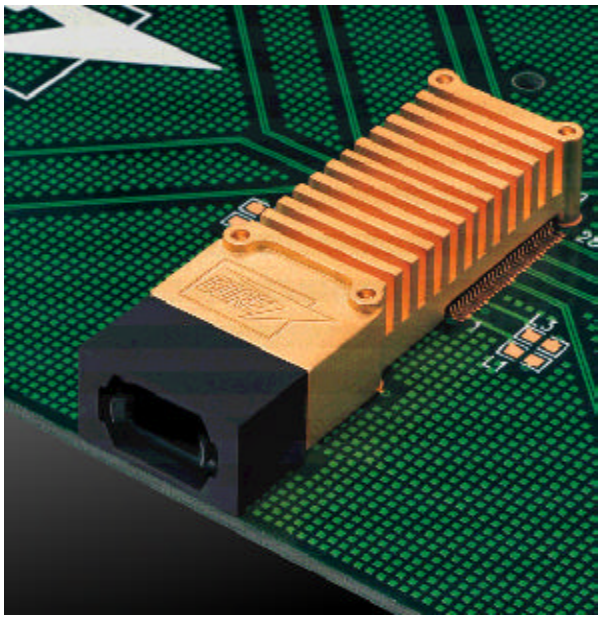
# nLIGHTEN™ PARALLEL FIBER OPTIC DATA LINK

W. L. GORE & ASSOCIATES, INC. • ELECTRONIC PRODUCTS DIVISION

## Executive Summary

W. L. Gore & Associates, Inc. is completing the development of a versatile family of multichannel optical transmitters and receivers targeted at intra-system and short reach inter-system high data rate communication links. The transmitter module utilizes Gore's Vertical Cavity Surface Emitting Laser (VCSEL) technology which makes multi-Gigabit / sec data rates possible while minimizing space and cost. The nLIGHTEN™ modules offer an 8X improvement in density over standard 1x9 serial transceiver products and significant reductions in costs at the same time. It utilizes 62.5 µm multimode fiber and its operational wavelength is 850 nm. Gore has combined its technology in high density packaging, precision micro-molding and VCSELs with its knowledge of high performance data link requirements to develop the nLIGHTEN family of high bandwidth * density, cost-effective, transmission products.

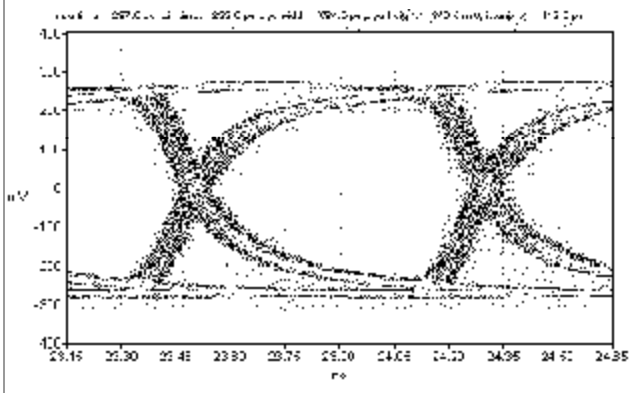


nLIGHTEN Parallel Fiber Optic Transmitter

## nLIGHTEN Features

- Robust Link Performance
  - Gore VCSEL Technology
  - Low Jitter
  - Receiver Sensitivity Margin
- High Bandwidth * Density
- Versatile Mounting Options
- Standard MPO Interface
- Multi-Source Footprint Design

nLIGHTEN Receiver Parallel Fiber Optic Transmitter Eye Pattern



High Data Rate Performance: Gore's nLIGHTEN Parallel Fiber Optic Receiver, 1.25 Gbit / s ($2^7-1$ PRBS) at minimum receive power (-18dBm).

## Robust Link Performance

### Gore VCSEL Technology

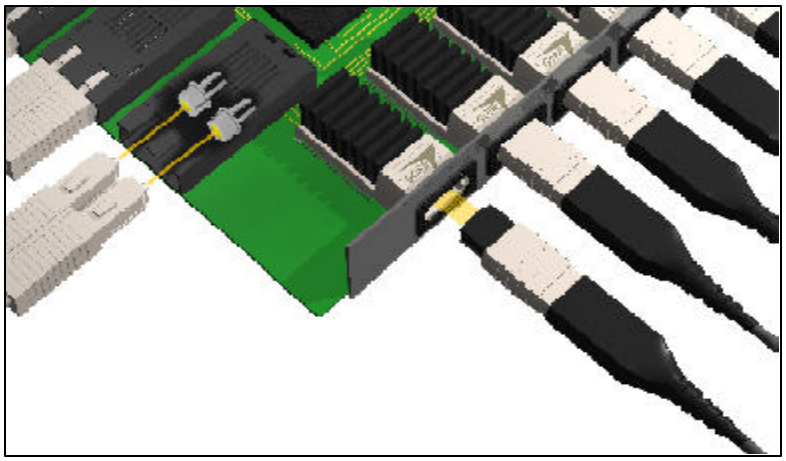
nLIGHTEN modules can deliver up to 1.5 Gbits / sec / channel data rates over multimode ribbon fiber cable. This is made possible by Gore's unique high speed VCSEL technology which not only provides scalability to higher data rates, but also has very stable light output over typical system temperature variations. Gore VCSELs have been demonstrated at data rates of up to 12.5 Gbps. This bandwidth headroom allows for wide open optical eyes, forming the foundation of nLIGHTEN's robust link operation.

### Low Jitter

Both copper and fiber optic data links create timing uncertainties, or jitter, in the transmitted data stream resulting in eye closure. Jitter in optical data links is a combination of effects; Inter-Symbol Interference (ISI) - created by

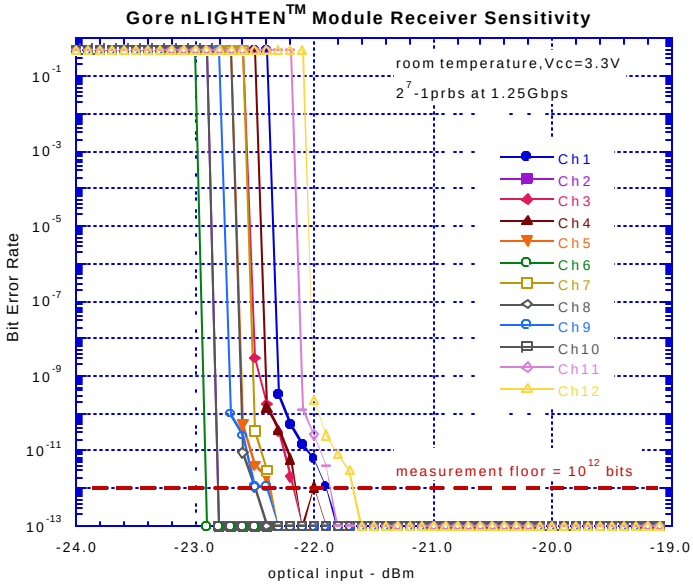
**W. L. Gore & Associates, Inc.**
**USA 1-800-445-4673**
**Fax 302-737-2819**
Visit our website on www.gore.com

**Europe +44 1382 561511**
**Fax +44 1382 561007**



Comparison of 12 channel nLIGHTEN ™ Module utilizing MPO optical I/O with serial 1 x 9 transceiver employing dual SC optical I/O.

bandwidth constrictions in the data path, Duty Cycle Distortion - created by timing variations in rising and falling edges of the data stream, and Random Noise-created by crosstalk and thermal noise in the circuits. Gore's design minimizes these effects through increased bandwidth in the active and passive components. The signal integrity of the data is ensured by careful design, simulation and fabrication of the transmission line path. The bandwidth of Gore's VCSEL devices and PIN photodetectors exceed 2.5 GHz. The laser driver and photo receiver circuits are fabricated in a high performance silicon bi-polar process and have been designed to meet the broadly utilized Gigabit Ethernet (IEEE 802.3) jitter budget.




## Receiver Sensitivity Margin

While the optical budget for the nLIGHTEN link specifies a minimum receive power of –18dBm (for an infinite extinction ratio), typical sensitivity achieved is better than –21dBm. The sensitivity plot shows the 12 nLIGHTEN module channels BER vs. received power. This margin of sensitivity allows designers to statistically estimate typical bit errors substantially below the specified $10^{-12}$.

## High Bandwidth * Density

Gore's parallel array module provides about 20 Gbps / inch (8 Gbps / cm) Bandwidth Density on the edge of the board. By comparison, this is approximately eight times higher than 1 x 9 serial transceiver modules. Through creative designs and Gore's unique high density packaging technologies, we've created a module that is just slightly wider than the cable connector that plugs to it.

## Versatile Mounting Options

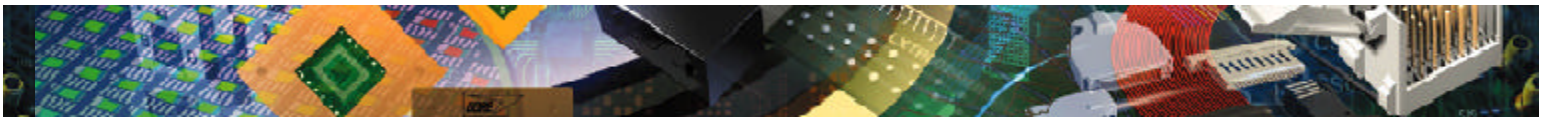
The nLIGHTEN modules are typically mounted on the edge of the printed circuit board as shown above. Other mounting options are "In-Board" where the connector interface does not overhang the edge of the PCB and "Thru-Backplane" which will directly mate with the emerging backplane adapters being introduced as part of the IEC 1076-4-101 2mm backplane connector families.

## Standard MPO Interface

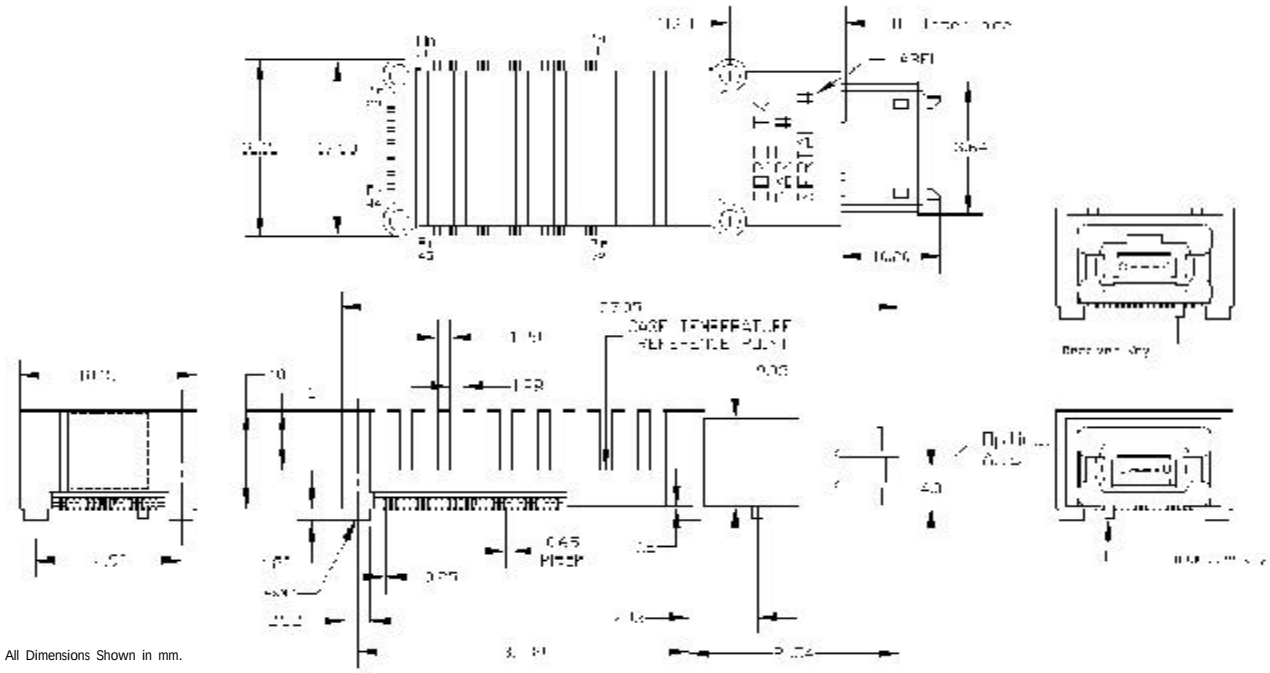
The Gore parallel array module is easily cabled using the standard MPO ribbon fiber connector (IEC 1754-7 and TIA / EIA 604-5). This interface was chosen because of its ten years of proven performance in telecommunications and computing systems. It is the only optical array connector currently available from multiple sources. The MPO is the "recommended" optical connector for HiPPI 6400 with cable assemblies available through a large number of qualified vendors.

## Multi-Source Footprint Design

In anticipation of market needs, Gore has entered into a multi-source agreement with other suppliers. The modules are designed to common specifications, footprints, and pin functionality.



## Transmitter / Receiver CAD Drawing



All Dimensions Shown in mm.

## Preliminary nLIGHTEN™ Transmitter Specifications

| General | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Dissipation | | | 900 | 1305 | mW | |
| Power Supply | Vcc | 3.135 | 3.3 | 3.465 | V | |
| Operating Case Temperature | | 0 | | 80 | C° | |
| **Optical Parameters** | **Symbol** | **Min** | **Typical** | **Max** | **Units** | **Notes** |
| Data Rate | | | 1.25 | | Gb/s | |
| Launch Power (ave) | Pout | -10 | | -4 | dBm | 1,2 |
| Extinction Ratio | | 6 | 12 | | dB | |
| Center Wavelength | λ | 830 | | 860 | nm | |
| Spectral Width (rms) | Δλ | | | 0.85 | nm | |
| Relative Intensity Noise | RIN | | | -117 | dB/Hz | |
| Output Risetime (20-80) | Tr | | | 260 | ps | |
| Output Falltime (20-80) | Tf | | | 260 | ps | |
| Total Jitter (pk-pk) | Tj | | | 227 | ps | 3 |
| Deterministic Jitter | Dj | | | 80 | ps | 3 |
| Channel-Channel Skew | | | | 75 | ps | |

Notes:
1. Maximum average power is not to exceed the lesser of -4 dBm or IEC 825-1 Class 3a laser safety and CDRH CFR 21 Ch. 1 (J) part 1040 Class 1 laser safety requirements.
2. Minimum average power is equivalent to 120 µW OMA (Optical modulation amplitude). OMA defined as the difference in optical power between a logic 1 and a logic 0 as defined in the HiPPI-6400 Optical PHY specification.
3. Equals TP1 to TP2 as defined in IEEE 802.3z Gigabit Ethernet Specification Section 38.5.

| Electrical Parameters | Symbol | Min | Typ. | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Differential In Amplitude | $\|V_{IH}-V_{IL}\|$ | 150 | | 400 | mV | 1 |
| Input Common Mode | | 1.0 | 1.2 | Vcc | V | 2 |
| Input Overshoot | | | | 20 | % | |
| Input Impedance | | 90 | 100 | 110 | Ω | 3 |

Notes:
1. Into 100 ohm differential termination.
2. Common mode (logic threshold) relative to ground.
3. On-module termination: input-to-complementary input.

## Preliminary nLIGHTEN™ Transmitter Pin Description

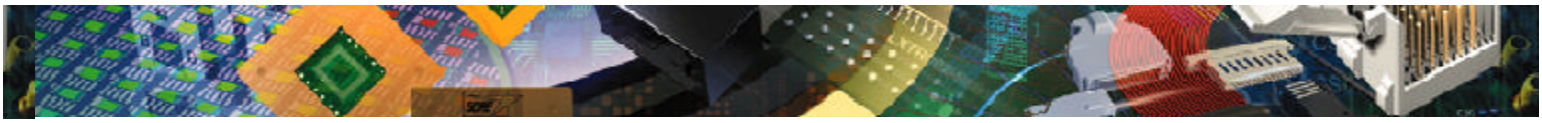
| Pin | Pin Name | Description | Logic Level | Notes | Pin | Pin Name | Description | Logic Level | Notes |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Vcc | Power Supply Voltage | 3.3 V DC | 1 | 37 | IN 7b | Input #7 Inverted | LVDS | |
| 2 | NC | Not Connected | | | 38 | IN 7a | Input #7 Non-Inverted | LVDS | |
| 3 | NC | Not Connected | | | 39 | GND | Ground | | |
| 4 | NC | Not Connected | | | 40 | GND | Ground | | |
| 5 | NC | Not Connected | | | 41 | IN 8b | Input #8 Inverted | LVDS | |
| 6 | WDOUT | Watchdog Ouput | LV CMOS Output | | 42 | IN 8a | Input #8 Non-Inverted | LVDS | |
| 7 | GND | Ground | | | 43 | GND | Ground | | |
| 8 | GND | Ground | | | 44 | GND | Ground | | |
| 9 | NC | Not Connected | | | 45 | GND | Ground | | |
| 10 | NC | Not Connected | | | 46 | IN 9b | Input #9 Inverted | LVDS | |
| 11 | GND | Ground | | | 47 | IN 9a | Input #9 Non-Inverted | LVDS | |
| 12 | GND | Ground | | | 48 | NC | Not Connected | | |
| 13 | IN 1b | Input #1 Inverted | LVDS | | 49 | GND | Ground | | |
| 14 | IN 1a | Input #1 Non-Inverted | LVDS | | 50 | GND | Ground | | |
| 15 | GND | Ground | | | 51 | IN 10b | Input #10 Inverted | LVDS | |
| 16 | GND | Ground | | | 52 | IN 10a | Input #10 Non-Inverted | LVDS | |
| 17 | IN 2b | Input #2 Inverted | LVDS | | 53 | GND | Ground | | |
| 18 | IN 2a | Input #2 Non-Inverted | LVDS | | 54 | GND | Ground | | |
| 19 | GND | Ground | | | 55 | IN 11b | Input #11 Inverted | LVDS | |
| 20 | GND | Ground | | | 56 | IN 11a | Input #11 Non-Inverted | LVDS | |
| 21 | IN 3b | Input #3 Inverted | LVDS | | 57 | GND | Ground | | |
| 22 | IN 3a | Input #3 Non-Inverted | LVDS | | 58 | GND | Ground | | |
| 23 | GND | Ground | | | 59 | IN 12b | Input #12 Inverted | LVDS | |
| 24 | GND | Ground | | | 60 | IN 12a | Input #12 Non-Inverted | LVDS | |
| 25 | NC | Not Connected | | | 61 | GND | Ground | | |
| 26 | IN 4b | Input #4 Inverted | LVDS | | 62 | GND | Ground | | |
| 27 | IN 4a | Input #4 Non-Inverted | LVDS | | 63 | NC | Not Connected | | |
| 28 | GND | Ground | | | 64 | WDRST | Watchdog Reset | LV CMOS Input | |
| 29 | IN 5b | Input #5 Inverted | LVDS | | 65 | GND | Ground | | |
| 30 | IN 5a | Input #5 Non-Inverted | LVDS | | 66 | GND | Ground | | |
| 31 | GND | Ground | | | 67 | LINKEN | Link Enable | LV CMOS Input | |
| 32 | GND | Ground | | | 68 | NC | Not Connected | | |
| 33 | IN 6b | Input #6 Inverted | LVDS | | 69 | NC | Not Connected | | |
| 34 | IN 6a | Input #6 Non-Inverted | LVDS | | 70 | NC | Not Connected | | |
| 35 | GND | Ground | | | 71 | NC | Not Connected | | |
| 36 | GND | Ground | | | 72 | Vcc | Power Supply Voltage | 3.3 V DC | 1 |

Notes:
1. Bypass capacitor of 10 µF Tantalum and .1µF MLC recommended.

## Preliminary nLIGHTEN Receiver Specifications

| General | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Dissipation | | | 1500 | 2500 | mW | |
| Power Supply | Vcc | 3.135 | 3.3 | 3.465 | V | |
| Operating Case Temperature | | 0 | | 80 | C | |
| **Optical Parameters** | **Symbol** | **Min** | **Typical** | **Max** | **Units** | **Notes** |
| Data Rate | | | 1.25 | | Gb/s | 1 |
| Receive Power (ave) | Pin | -16 | | 0 | dBm | 1, 2 |
| Center Wavelength | λ | 770 | | 860 | nm | |
| Return Loss | | 12 | | | dB | 3 |
| Total Jitter (pk-pk) | Tj | | | 266 | ps | 1,4 |
| Deterministic Jitter | Dj | | | 170 | ps | 1,4 |
| Channel-Channel Skew | Skew | | | 75 | ps | |

Notes:
1. With DC balanced data pattern and maximum run length less than 8 nsec.
2. BER = $10^{-12}$. Pin minimum equivalent to -18 dBm @ infinite extinction ratio or 30 µW OMA (Optical modulation amplitude). OMA is defined as the difference in optical power between a logic 0 and a logic1 as defined in the HiPPI-6400 Optical PHY specification.
3. Return loss measurement is defined in TIA/EIA FOTP-107
4. Equals TP3 to TP4 as defined in IEEE 802.3z Gigabit Ethernet Specification Section 38.5.



## Preliminary nLIGHTEN™ Receiver Specifications Continued

| Electrical Parameters | Symbol | min | typ. | max | unit | notes |
|---|---|---|---|---|---|---|
| Differential Out Amplitude | $\|V_{OH}-V_{OL}\|$ | 250 | | 400 | mV | 1 |
| Output Rise Time | Tr | | 375 | 350 | ps | 2 |
| Output Fall Time | Tf | | 375 | 350 | ps | 2 |
| Output Common Mode | | 1125 | | 1275 | mV | 3 |
| Output high state | | | | 1475 | mV | |
| Output low state | | 925 | | | mV | |
| Output overshoot | | | | 20 | % | |
| Duty Cycle Distortion | | | | TBD | % | |

Notes:
1. Into 100 Ω differential termination.
2. Measured between the 20% & 80% levels.
3. Common mode (logic threshold) relative to ground.

## Preliminary nLIGHTEN Receiver Pin Description

| Pin | Pin Name | Description | Logic Level | Notes | Pin | Pin Name | Description | Logic Level | Notes |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | Ground | | | 37 | Out7a | Output #7 Non-inverted | LVDS | |
| 2 | Vcc | Power Supply Voltage | 3.3 V DC | 1 | 38 | Out7b | Output #7 Inverted | LVDS | |
| 3 | Vcc | Power Supply Voltage | 3.3 V DC | 1 | 39 | GND | Ground | | |
| 4 | NC | Not Connected | | | 40 | GND | Ground | | |
| 5 | LNKE | Link Enable | LV CMOS input | | 41 | Out8a | Output #8 Non-inverted | LVDS | |
| 6 | DVAL | Data Valid output | LV CMOS output | 2 | 42 | Out8b | Output #8 Inverted | LVDS | |
| 7 | Vcc | Power Supply Voltage | 3.3 V DC | 3 | 43 | GND | Ground | | |
| 8 | GND | Ground | | | 44 | GND | Ground | | |
| 9 | NC | Not Connected | | | 45 | GND | Ground | | |
| 10 | GND | Ground | | | 46 | Out9a | Output #9 Non-inverted | LVDS | |
| 11 | GND | Ground | | | 47 | Out9b | Output #9 Inverted | LVDS | |
| 12 | GND | Ground | | | 48 | NC | Not Connected | | |
| 13 | Out1a | Output #1 Non-inverted | LVDS | | 49 | GND | Ground | | |
| 14 | Out1b | Output #1 Inverted | LVDS | | 50 | GND | Ground | | |
| 15 | GND | Ground | | | 51 | Out10a | Output #10 Non-inverted | LVDS | |
| 16 | GND | Ground | | | 52 | Out10b | Output #10 Inverted | LVDS | |
| 17 | Out2a | Output #2 Non-inverted | LVDS | | 53 | GND | Ground | | |
| 18 | Out2b | Output #2 Inverted | LVDS | | 54 | GND | Ground | | |
| 19 | GND | Ground | | | 55 | Out11a | Output #11 Non-inverted | LVDS | |
| 20 | GND | Ground | | | 56 | Out11b | Output #11 Inverted | LVDS | |
| 21 | Out3a | Output #3 Non-inverted | LVDS | | 57 | GND | Ground | | |
| 22 | Out3b | Output #3 Inverted | LVDS | | 58 | GND | Ground | | |
| 23 | GND | Ground | | | 59 | Out12a | Output #12 Non-inverted | LVDS | |
| 24 | GND | Ground | | | 60 | Out12b | Output #12 Inverted | LVDS | |
| 25 | NC | Not Connected | | | 61 | GND | Ground | | |
| 26 | Out4a | Output #4 Non-inverted | LVDS | | 62 | GND | Ground | | |
| 27 | Out4b | Output #4 Inverted | LVDS | | 63 | GND | Ground | | |
| 28 | GND | Ground | | | 64 | NC | Not Connected | | |
| 29 | Out5a | Output #5 Non-inverted | LVDS | | 65 | GND | Ground | | |
| 30 | Out5b | Output #5 Inverted | LVDS | | 66 | Vcc | Power Supply Voltage | 3.3V DC | 3 |
| 31 | GND | Ground | | | 67 | DVAL | Data Valid output | LV CMOS Output | |
| 32 | GND | Ground | | | 68 | NC | Not Connected | | |
| 33 | Out6a | Output #6 Non-inverted | LVDS | | 69 | NC | Not Connected | | |
| 34 | Out6b | Output #6 Inverted | LVDS | | 70 | Vcc | Power Supply Voltage | 3.3 V DC | 1 |
| 35 | GND | Ground | | | 71 | Vcc | Power Supply Voltage | 3.3 V DC | 1 |
| 36 | GND | Ground | | | 72 | GND | Ground | | |

Notes:
1. Analog Vcc. Recommend 100 ohm@100 MHz ferrite bead to host board Vcc. Part Numbers: Steward # HZ0805E601R Digi-key part # 240-1-18-1-ND
2. LV CMOS Output. No pull-up resistor required.
3. Bypass capacitor of 10 µF Tantalum and .1µF MLC recommended.



**W. L. Gore & Associates, Inc.**
**USA 1-800-445-4673**
**Fax 302-737-2819**
Visit our website on www.gore.com

**Europe +44 1382 561511**
**Fax +44 1382 561007**

F109 2/20 CTREE