NTF2955

Power MOSFET

−60 V, 2.4 A, Single P−Channel SOT−223

Features

- TMOS7 Design for low $R_{DS(on)}$
- Withstands High Energy in Avalanche and Commutation Modes

Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−2.4	A
		T_A = 85°C		−1.7	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.92	W
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−1.6	A
		T_A = 85°C		−1.1	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.83	W
Pulsed Drain Current	tp = 10 μs		I_{DM}	9.2	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 25 V, V_G = 10 V, I_{PK} = 6.7 A, L = 10 mH, R_G = 25 Ω)			EAS	225	mJ
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Tab (Drain) − Steady State (Note 2)	$R_{\theta JC}$	14	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	65	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	150	

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.127 in^2 [1 oz] including traces)
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu. area = 0.341 in^2)

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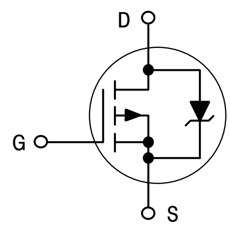
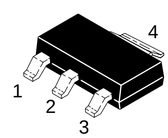
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−60 V	145 mΩ @ −10 V	−2.4 A

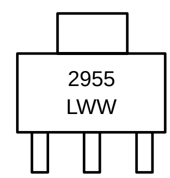
P−Channel





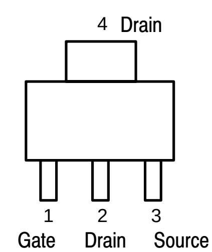
SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM



2955 = Device Code
L = Location Code
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTF2955T1	SOT−223	1000/Tape & Reel
NTF2955T3	SOT−223	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				66.4		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −60 V	T_J = 25°C			−1.0	μA
			T_J = 125°C			−50	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −1.0 mA		−2.0		−4.0	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −0.75 A			145	170	mΩ
		V_{GS} = −10 V, I_D = −1.5 A			150	180	
		V_{GS} = −10 V, I_D = −2.4 A			154	185	
Forward Transconductance	g_{FS}	V_{GS} = −15 V, I_D = −0.75 A			1.77		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			492		pF
Output Capacitance	C_{OSS}				165		
Reverse Transfer Capacitance	C_{RSS}				50		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 30 V, I_D = 1.5 A			14.3		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.2		
Gate−to−Source Charge	Q_{GS}				2.3		
Gate−to−Drain Charge	Q_{GD}				5.2		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 25 V, I_D = 1.5 A, R_G = 9.1 Ω R_L = 25 Ω			11		ns
Rise Time	t_r				7.6		
Turn−Off Delay Time	$t_{d(OFF)}$				65		
Fall Time	t_f				38		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.5 A	T_J = 25°C		−1.10	−1.30	V
			T_J = 125°C		−0.9		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 1.5 A			36		ns
Charge Time	t_a				20		
Discharge Time	t_b				16		
Reverse Recovery Charge	Q_{RR}				0.139		nC

3. Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

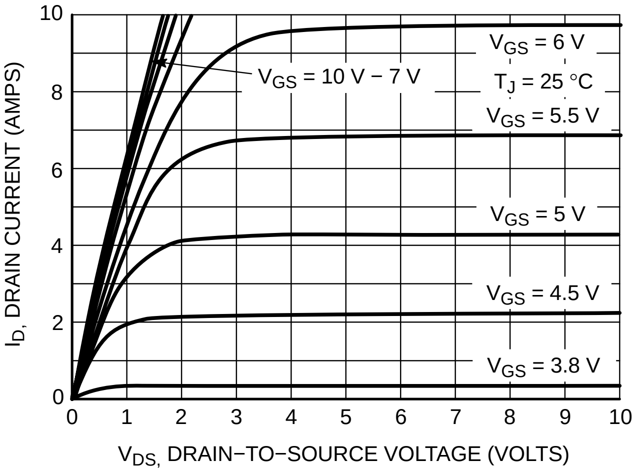


Figure 1. On−Region Characteristics

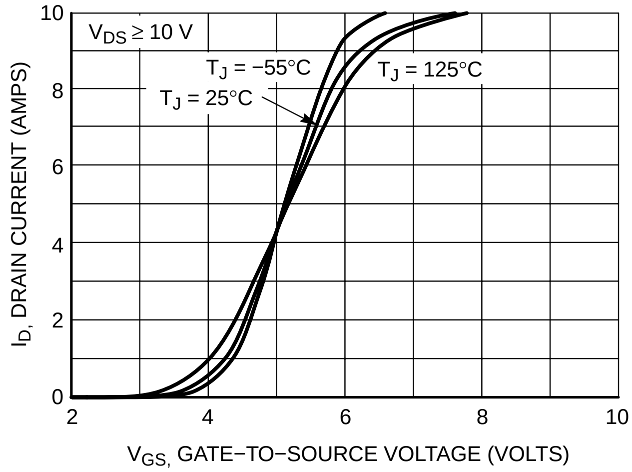


Figure 2. Transfer Characteristics

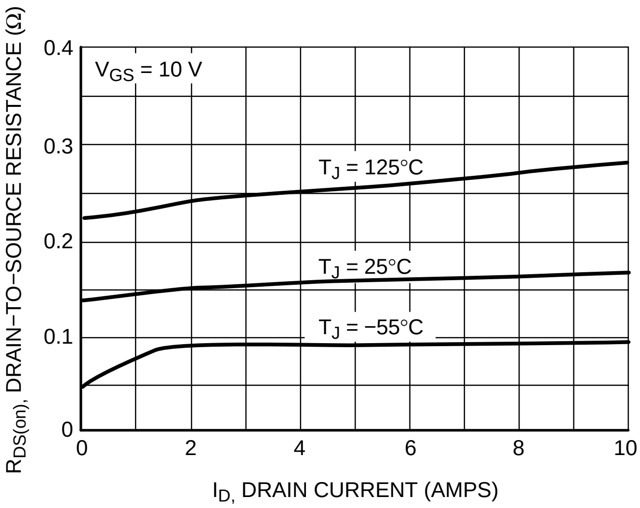


Figure 3. On−Resistance versus Drain Current and Temperature

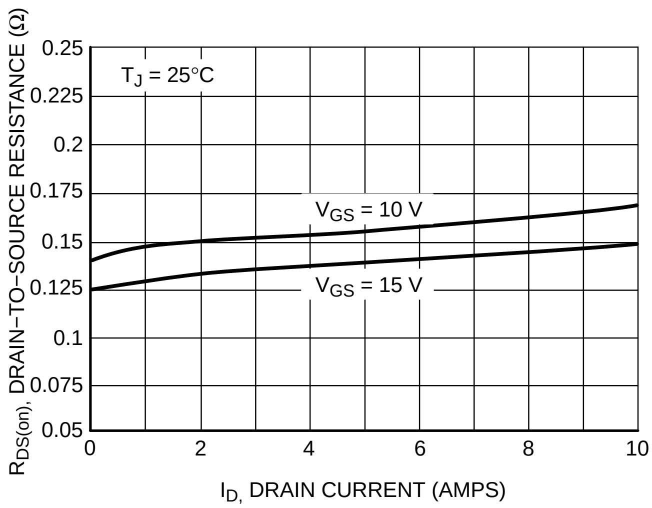


Figure 4. On−Resistance versus Drain Current and Gate Voltage

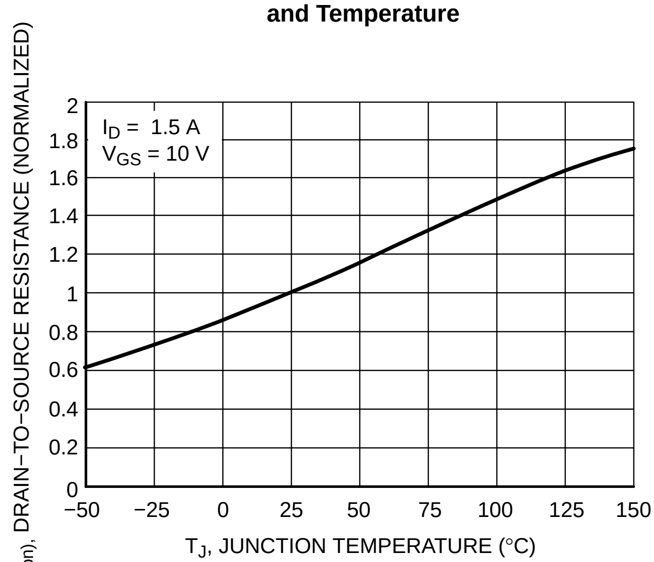


Figure 5. On−Resistance Variation with Temperature

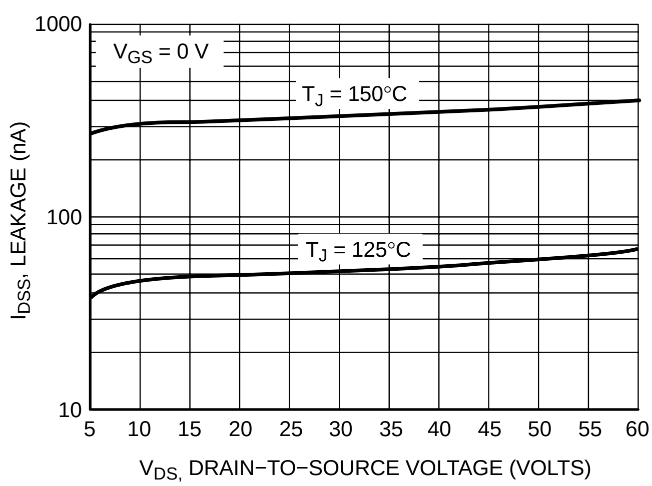


Figure 6. Drain−to−Source Leakage Current versus Voltage

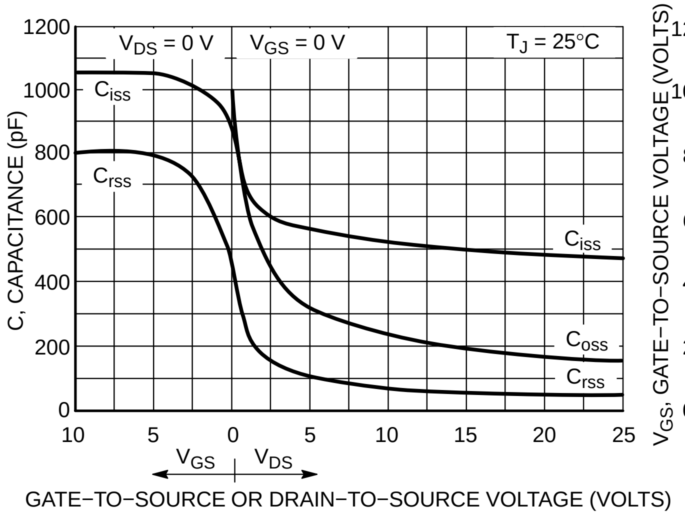


Figure 7. Capacitance Variation

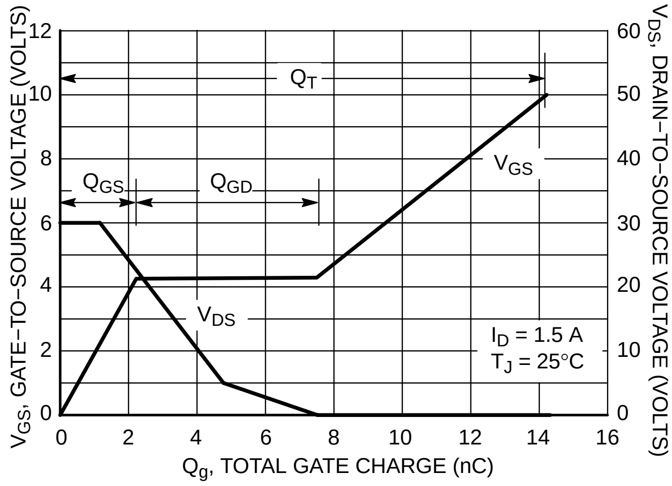


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

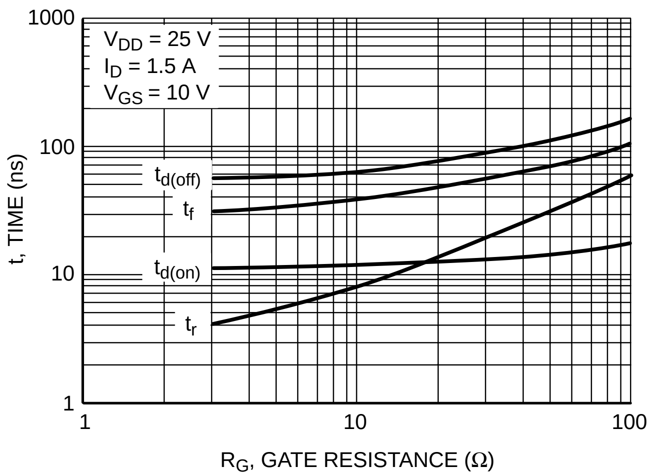


Figure 9. Resistive Switching Time Variation versus Gate Resistance

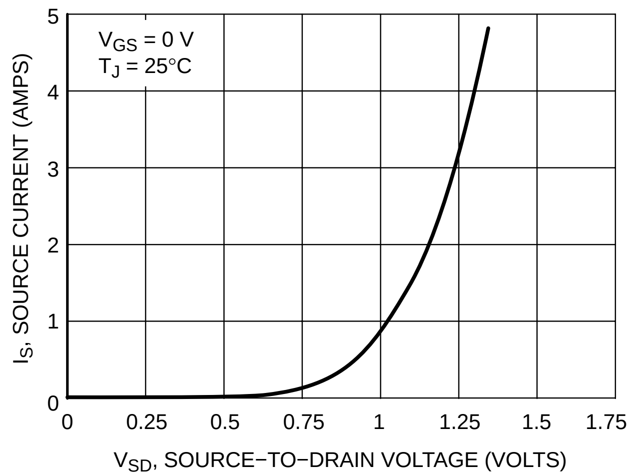


Figure 10. Diode Forward Voltage versus Current

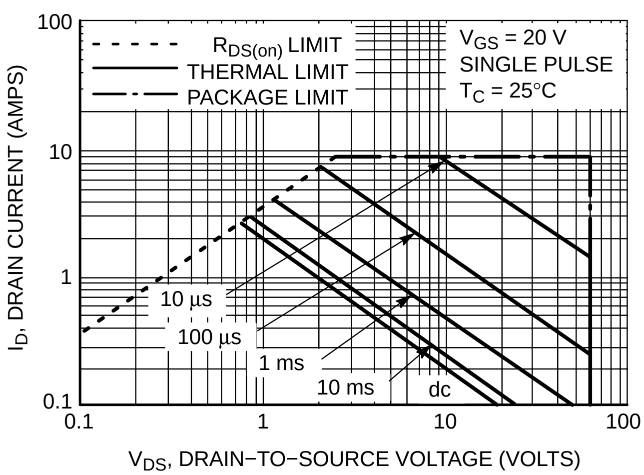


Figure 11. Maximum Rated Forward Biased Safe Operating Area

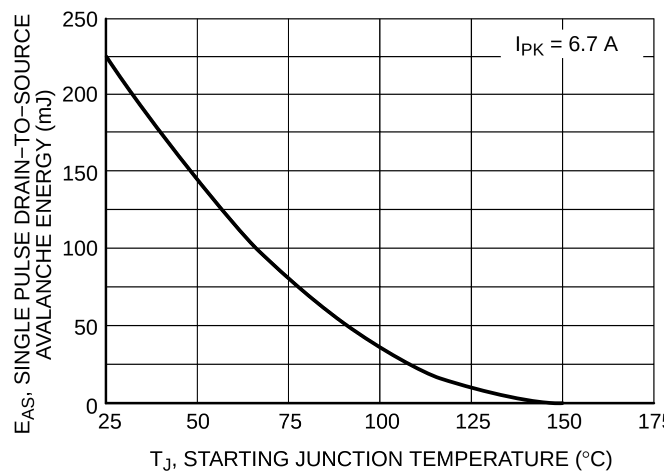
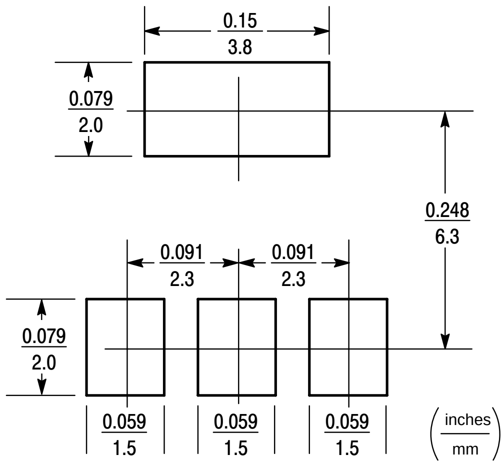


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

INFORMATION FOR USING THE SOT−223 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT−223 POWER DISSIPATION

The power dissipation of the SOT−223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT−223 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

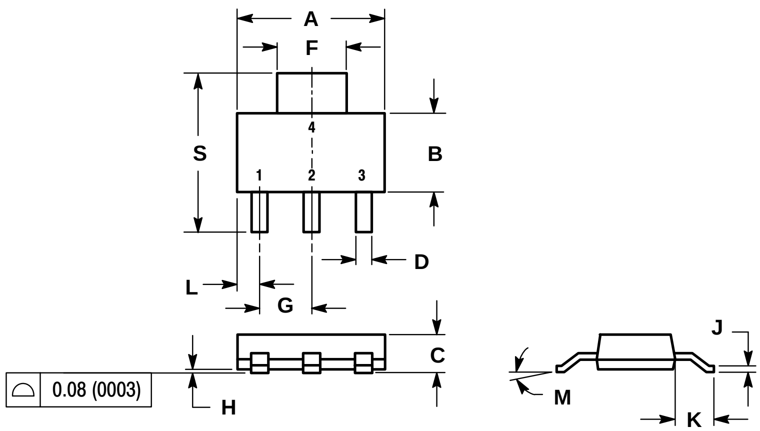
The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 833 milliwatts.

$$P_D = \frac{150°C - 25°C}{150°C/W} = 833 \text{ milliwatts}$$

The 150°C/W for the SOT−223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 833 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT−223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology.

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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