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Photon Vision Systems - PRELIMINARY

High Performance Linear CMOS Image Sensors
Low Power TSLIS 128

The Photon Vision Systems TSLIS 128 is a high performance linear image sensor designed for a wide variety of applications as a superior CCD replacement, including:

Portable/Handheld applications
Edge Detection
Contact Imaging
Bar Code Reading
Encoding and Positioning
Text Recognition

Description

The TSLIS 128 Linear Image Sensor consists of an array of low dark current photo-diode pixels with shutter and has excellent performance characteristics. The device operates with a single clock and a start pulse in standard mode for self shuttering. In addition, the device has two other shuttering modes, allowing for excellent exposure control. Operation is from 2.8 Volts to 5.0 Volts with 3.3 Volts as standard. The device also features a power down standby mode, making it ideal for portable devices.

A key feature over traditional CCD technology, is that the device can be read and reread Non-Destructively, allowing the user to maximize signal to noise and dynamic range.

The TSLIS 128 series are supplied in Chip Scale package or is available in die form. The packaged versions utilize an optically clear window, virtually eliminating distortion over that caused by traditional 'clear' plastic packages.

Key Features

- Low Cost
- Single Supply Operation 3.3V specified
- High Sensitivity
- High Signal to Noise
- Non-Destructive read capable
- 1.0 kHz. to 2.0 MHz Operation
- Extremely Low Dark Current for extra long integration time (elite^{SM})
- Optically clear package (Packaged Version) or Chip Scale
- Sequential or Sub-Frame Operation
- Completely integrated Timing and Control
- Replaces CCD systems, not just the sensor
- Power Down/Standby mode

MODEL	ARRAY SIZE	PIXEL SIZE h x w
LPLIS-128	1 x 128	63.5u X 63.5u

Array length is 8.128 mm. See Mechanical Dimension for Die layout.

PHYSICAL DESCRIPTION

Pixel Type	Active Column Photo-Diode
Array Size	1 row X 128
Pixel Size	63.5W X 63.5 µm pitch
Imaging Active Area	0.0635mm x 8.128 mm
Output	5K ohm @ 2 pF
Fill Factor approx.	≥97 %

IMAGER PIN I/O

Signal Name	**Pin Name**	**Function**	**PIN #**
Clock	CLK	Master Clock, 1X Pixel Rate	5
Serial Input	SI	Start frame readout	10
Standby	STBY	Standby Power Down Mode	7
Analog Power	AVDD	Analog circuits power	2, 12
Analog Ground	AGND	Analog circuits ground	1, 11
Digital Power	DVDD	Digital circuits power	4
Digital Ground	DGND	Digital circuits ground	3
Video Out	VOUT	Video Output port	13
Pixel Reset	!PR	Resets pixels when asserted	8
Charge Xfer	!CT	Charge Transfer from pixel to sample and hold	6
Mode Select	!MS	Select Standard or Independent mode	9

ELECTRO-OPTICAL SPECIFICATION

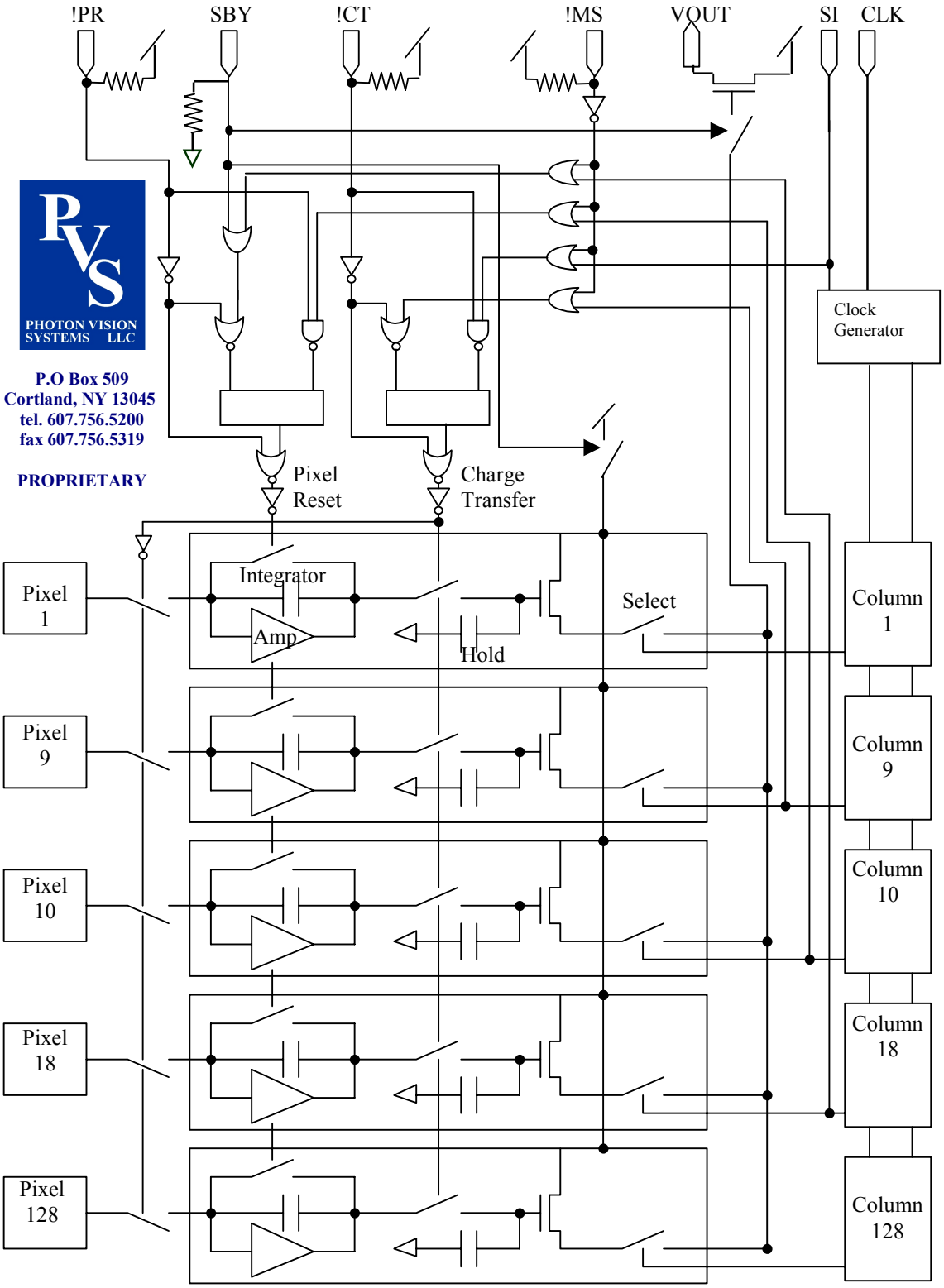
Specs given at 24 °C 3.3 Volts standard mode of operation at 512kHz, unless otherwise noted.

Parameter	**MIN**	**TYPICAL**	**MAX**	**Units**
Supply Voltage	3.00	3.3	5.0	V
Supply Current (see note 1)	<0.1	3.0	4	mA
Input High Logic Level	2.7			V
Input Low Logic Level			0.7	V
Input current				
Pixel Read Rate (note 2)			2.0	MHz
Analog Video Load			5000@ 2pF	Ohms
Output voltage at Saturation	1.8	2.0	3.3	V
Output voltage at Dark	0.01	0.1	0.2	V
Linearity (per Pixel 5%-70% average) (Note 5)	0.05	1.0		%Sat.
Dark Signal (1 sec. Integration time, note 3)		0.1	0.3	%Sat.
PRNU – Pixel Response Non-uniformity (Note 6)		±3.0	±6.0	%
Fill Factor		97		% area
Relative Humidity (non-condensing)			90	%
Operating Temperature	0	24	55	°C
Pixel Output Stability after 250 ns (Note 7)			2	%Sat.
Read Noise (note 4)			2	mV rms
Spectral Response	350		1100	nm
Quantum Efficiency @ 630 nm		50		%
Image Lag		0.25		%
Saturation Exposure @ 600 nm		88		nJ/cm^2
Signal to Noise RMS (note 4)		63		dB

Notes

1. Current draw varies with clock speed, ands temp. Minimum Value reflects ‘stand-by’ power mode of operation.
2. Specs. Given at pixel read rates of 512 kHz at 24 °C an 50% duty cycle
3. At 24 °C.
4. Temporal rms noise @ 512 kHz erc and 256 kHz video band width filter applied, Vsat/rms read noise.
5. Pixel linearity from 0.1 to 1.4 VDC (5% - 70% Vsat).
6. PRNU is the Maximum Difference between the average output voltage of all pixels of the imager under test and the output of a single pixel with even illumination across all pixels.
7. Stability is load dependant, specified into 5000 ohms with maximum 2pF load.

BLOCK DIAGRAM



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Timing and Operation

The device clock should be 50% duty cycle. The device has three modes of operation, Standard mode, Mixed Mode and Independent Control mode. Modes can be switched from mode to mode at any time by switching the !MS line. The mode is selected with the !MS input, when not connected or pulled to Vdd, the device is in Standard mode, when pulled to ground, the device switches to Independent Control mode. The device will power up or come out of standby in whichever mode is selected with the !MS line. Independent control mode makes use of two additional signals, !CT and !PR. !CT and !PR are true low inputs. The signals are true when pulled to ground.

Standard Mode Timing:

Requires that the !MS, !PR and !CT lines be held High or floating. SI pulse to go low before rising edge of next clock. Clock shown for 500 kHz Clock. CLK, SI, !CT, and !PR are real world I/O.

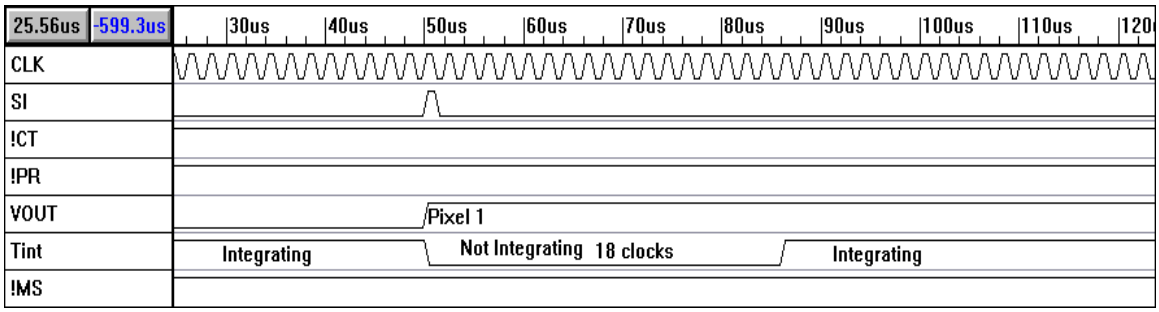


Figure 1a. Standard mode timing, beginning of frame.

Note that !PR and !CT signals are internally pulled up to VDD, and therefore can be unconnected.

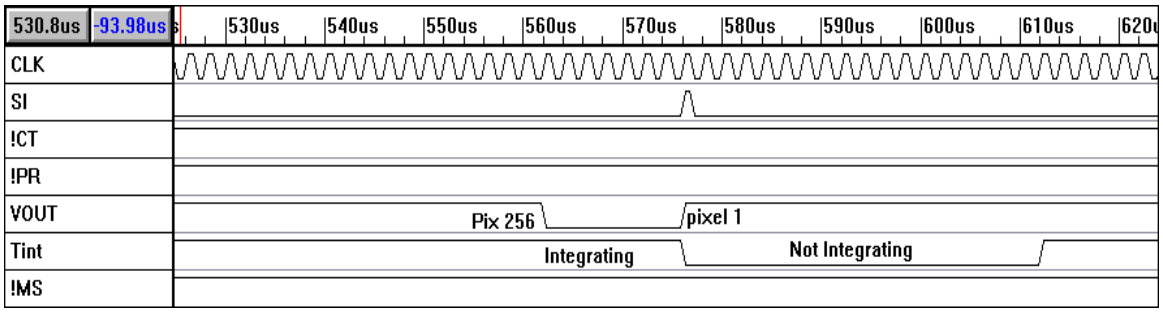


Figure 1b. Standard mode timing, end of frame and beginning of next frame.

MIXED MODE TIMING:

Mixed Mode timing is illustrated below. In mixed mode timing, !PR and or !CT can be asserted at anytime after eighteen clocks from the rising edge of SI. If !PR or !CT is asserted during this time, unpredictable results can occur. The integration time then becomes the time duration between rising edge of !PR and falling edge of !CT, and is therefore controllable by the user.

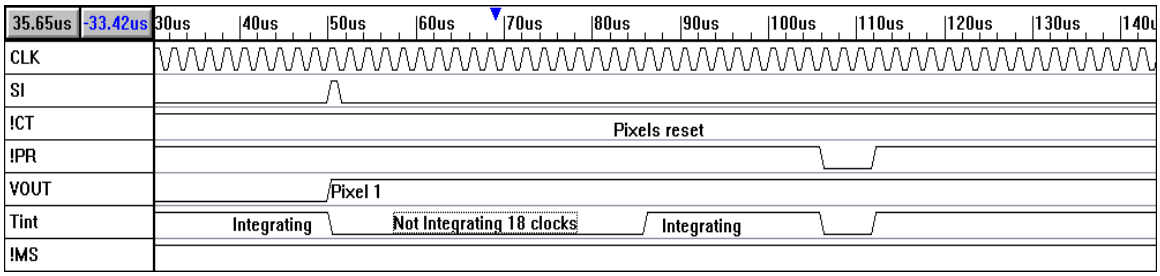


Figure 2a: Illustrating control of timing in Mixed mode.

Note that !PR and !CT cannot be asserted within eighteen clocks of the rising edge of SI. Asserting !PR simply causes the pixels to be reset, and the pixels are held in reset for the duration !PR is asserted. Asserting !CT cause the accumulated pixel charge to be transferred to the Sample and hold. If !CT is asserted during a frame read, the VOUT will reflect the accumulated charge from the pixel that !CT was asserted to the end of frame.

Independent Control Mode Timing:

Independent control mode timing allows independent control of integration time from readout. This is an asynchronous mode (except for SI, which works the same as for Standard Mode), allowing several read-out and integration options, including a non-destructive readout mode. !MS, !PR and !CT are level controlled signals. They perform the indicated action as long as they are true (pulled to ground).

Figures 3a and 3b indicates timing for two consecutive frames for a strobed application such as a pulsed LED. The user would fire the strobe during the time period that !PR is false or held high. The signal that controls the LED could be used to control !PR signal.

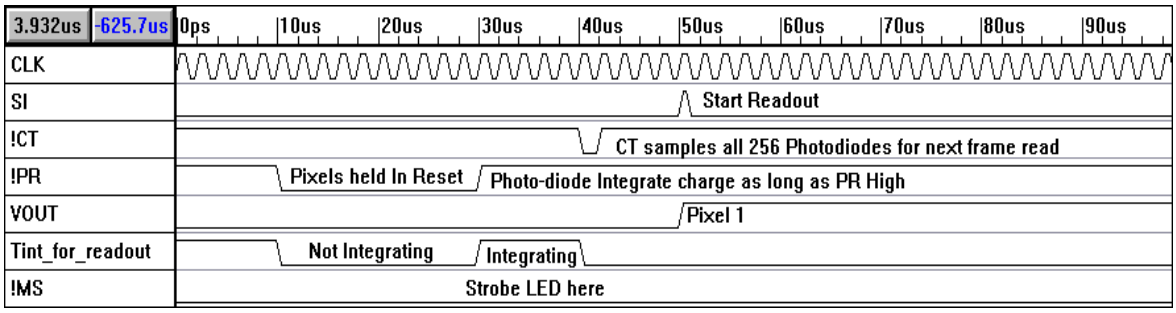


Figure 3a. First portion of timing diagram showing events at beginning of frame.

SI pulse to go low before rising edge of next clock. Clock shown for 500 kHz Clock. CLK, SI, !CT, !MS and !PR are real world I/O. Tint_for_readout represents the pixel integration time that has been captured by the Sample and hold when !CT is asserted and is not an I/O. Note that the photo-diodes themselves are actually still integrating while !PR is held high. Charge transfer or !CT is used to move the accumulated photon generated charge simultaneously from all 256 the photo-diode to their respective sample and holds for readout. !CT therefore should be asserted before the issuance of the SI pulse, and optionally can also be re-issued anytime during readout to re-sample the photo-diode accumulated charge for the reset of the frame.

Note that non-destructive read-out can occur if !CT then followed by SI are pulsed while !PR is held high. Minimum pulse width for !PR and !CT is one microsecond to allow enough time for pixels to reset or charge to transfer.

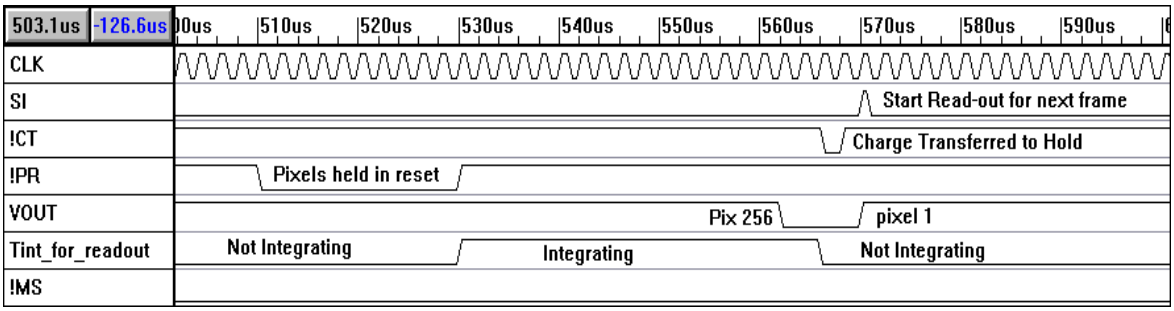


Figure 3b. End of frame events.

Note that the photo-diode integration time is controlled solely by the !PR signal. By holding !PR low the pixels are held in reset, thus shortening the integration time. Or on the other hand, minimizing the !PR pulse (minimum time 1 microsecond), can maximize integration time. User can balance !PR with light intensity pulse to maximize light source efficiency and power consumption. Also can be used to minimize effects of external or ambient light by keeping !PR high only while the light source is on.

Note that the timing of !PR can occur at any time, during frame read or after frame read. However doing so during a frame read may slightly increase image lag as the sample and hold is not reset as shown in the above timing diagram. Minimal image lag will occur if !PR and !CT are asserted simultaneously so that the sample and hold site is reset with the photo-diode.

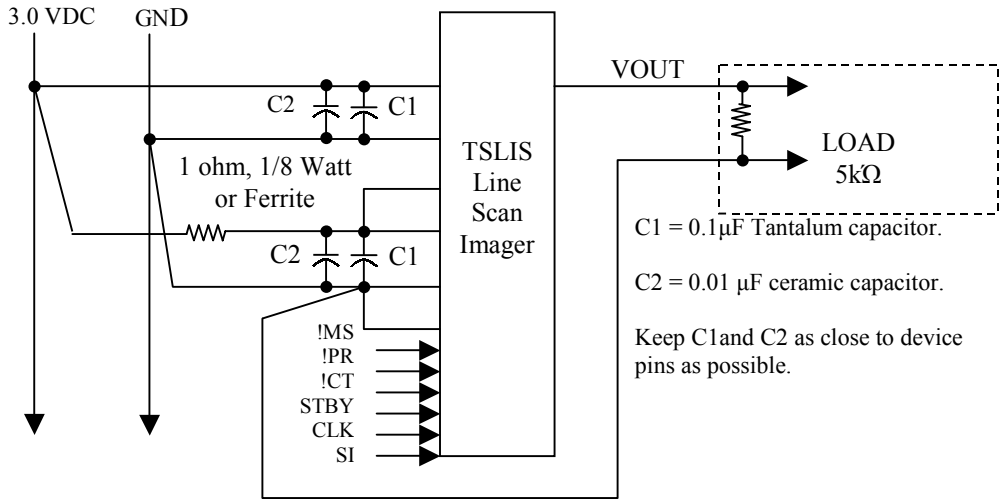
Timing !PR high with the light source pulse also eases timing constraints, especially with variable timing as caused during acceleration/deceleration of the scanner.

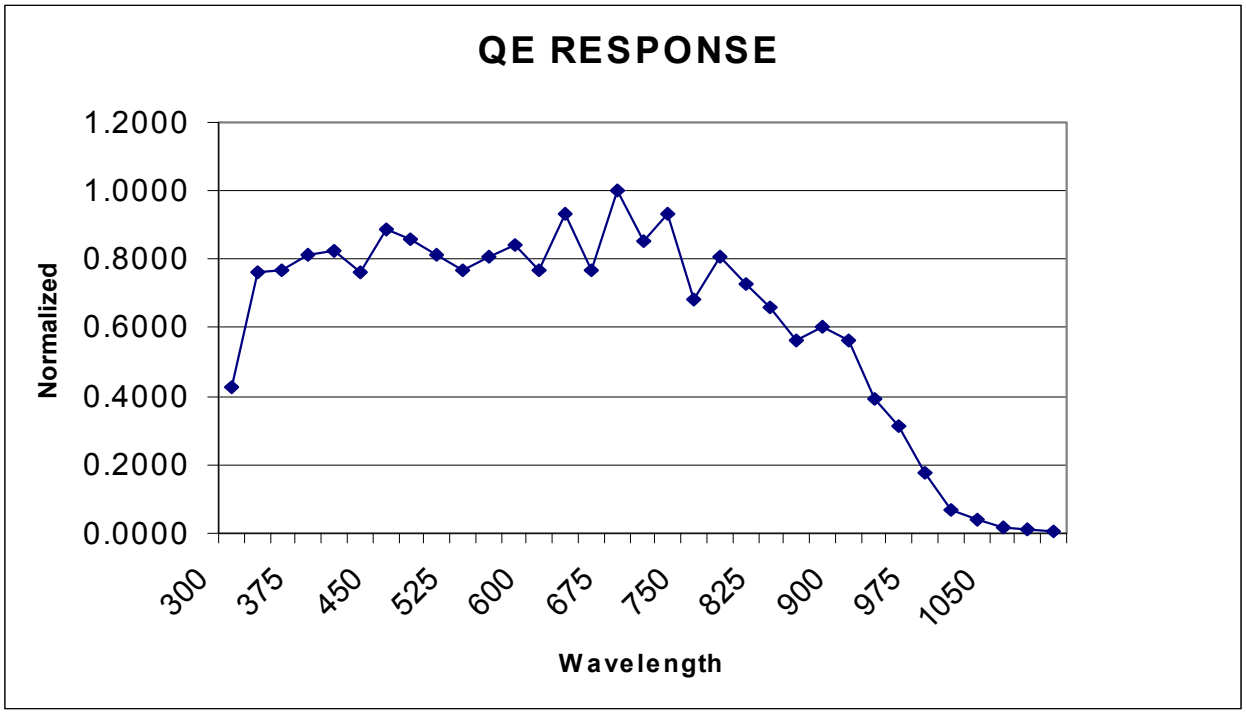
Because !CT, !MS, and !PR are asynchronous, asserting !CT simply transfers the charge of all 256 photo-diodes to the sample and hold, irregardless of frame read or not, however it is recommended to only assert !CT immediately before the next frame read as initiated by SI. !PR can also be asserted at any time, either during or before a frame read. !MS can also be asserted at any time to change from one mode to the other.

STANDBY POWER MODE:

The device has a true high input, SBY, that when pulled to VDD puts the device in SBY mode. SBY is internally pulled to ground, and thus can be left disconnected for default normal operation. This is a power saving mode, removing power from some internal circuits. Note that SBY should not be asserted during a frame read out. SBY does not affect the currently selected mode, Standard or Readout, as set with the !MS input.

TYPICAL HOOKUP





Note: Data below 350nm not measured, but device is sensitive to 200 nm. Shown for un-encapsulated device.

Absolute maximum ratings, T A = 25°C unless otherwise noted, see Note 1, below. †

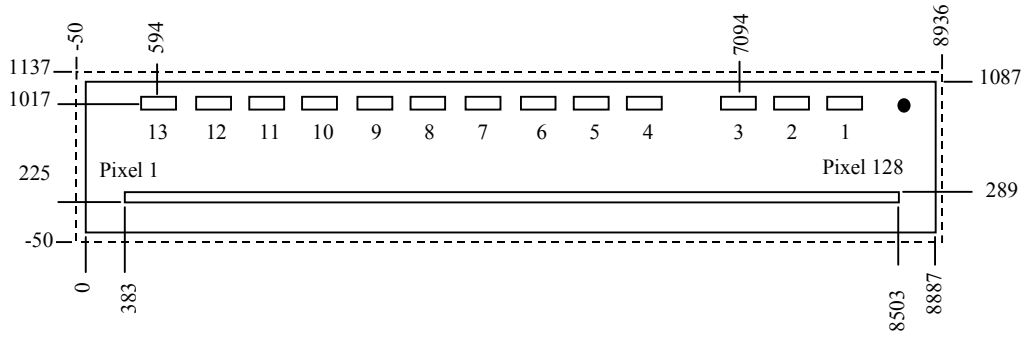
Supply voltage range, V_{DD}	0 V to 5.25 V
Digital input current range, I	–20 mA to 20 mA
Operating case temperature range, T C (see Note 2)	–10°C to 70°
Operating free-air temperature range, T A	0°C to 50°C
Storage temperature range	–20°C to 85°C
Humidity range, Rh	0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds	255°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under "recommended operating conditions" is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

NOTES: 1. Voltage values are with respect to the device GND terminal.

2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

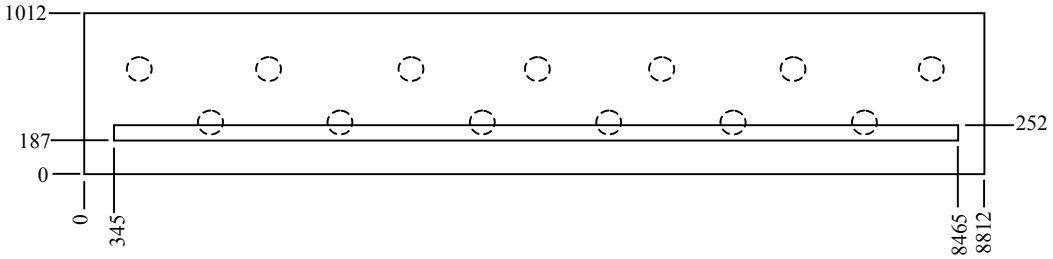
MECHANICAL DIMENSIONS – DIE AND CSP PACKAGE



Notes:

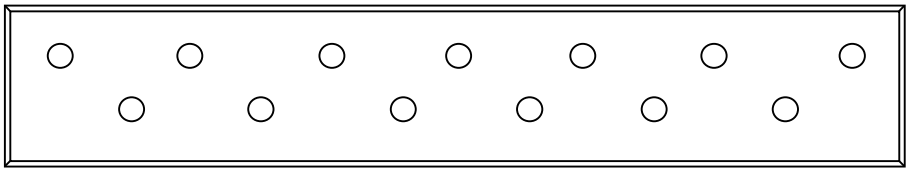
1. Dimension in microns, +/- 2, except die cut boundary which is +/- 25 and +/- 1 degree.
2. Bond pads are 60 x 250 microns on 400 micron pitch unless otherwise noted.
3. Die is 38 +/- 5 microns thick.

Figure 1 – TSLIS 128 Die top view. Dimensions in microns. FOR REFERENCE ONLY



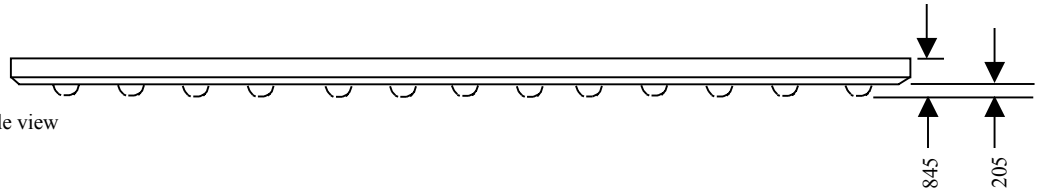
CSP Top view.

1. Dimensions in microns.
2. Tolerance is +/- 25 microns.



CSP Bottom view (bumps up)

1. Bump size and location is TBD



CSP Side view

Figure 2 - CSP Package. Dimensions in microns. FOR REFERENCE ONLY.

NOTICE

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This device may be covered under the following US patent: 6,084,229