National Semiconductor

MILITARY DATA SHEET

MNLMF90CM-X REV 0AL

Original Creation Date: 08/22/95
Last Update Date: 08/22/95
Last Major Revision Date: 08/22/95

4th ORDER LMCMOS PROGRAMMABLE ELLIPTIC NOTCH FILTER

Industry Part Number

LMF90CM

NS Part Numbers

LMF90CMJ/883

Prime Die

LMF90CM

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V, V- = -5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vos	Output Offset Voltage	W=D=V-, R=V+, fCLK = 167KHz			-120	120	mV	1, 2, 3
		W=D=R=Gnd, fCLK = 250KHz			-140	140	mV	1, 2, 3
		W=V+, D=Gnd, R=V-, fCLK = 500KHz			-170	170	mV	1, 2, 3
Is+	Supply Current	Vin1 = Vin2 = Gnd, fCLK = 500KHz				5	mA	1, 2, 3
Is-	Supply Current	Vin1 = Vin2 = Gnd, fCLK = 500KHz			-5		mA	1, 2, 3
Vout	Output Voltage Swing	Rl = 5K Ohm	3		-4	4	V	1, 2, 3
Vi1	Logical "Low" Input Voltage			1, 2, 3, 7 10		-4.0	V	1, 2, 3
Vi2	Logical "Gnd" Input Voltage			1, 2, 3, 7, 10	-1.0	1.0	V	1, 2, 3
Vi3	Logical "HIGH" Input Voltage			1, 2, 3, 7	4.0		V	1, 2, 3
Iin	Input Current			1, 2, 3, 7, 10	-10	10	uA	1, 2, 3
Vil	Logic "0" Input Voltage, Pins 5 & 6	Pin 5, XLS = V+, or Pin 6, XLS = Gnd	3, 4			-4.0	V	1, 2, 3
Vih	Logic "1" Input Voltage, Pins 5 & 6	Pin 5, XLS = V+, or Pin 6, XLS = Gnd	3, 4		4.0		V	1, 2, 3
Vil	Logic "0" Input Voltage, Pins 6	V+ - V- = 10V, XLS = V- or V+ = +5V, V- = 0V, XLS = +2.5V	3, 4			0.8	V	1, 2, 3
Vih	Logic "1" Input Voltage, Pin 6	V+ - V- = 10V, XLS = V- or V+ = +5V, V- = 0V, XLS = +2.5V	3, 4		2.0		V	1, 2, 3
Vol	Logic "0" Output Voltage, Pin 6	XLS = V+, |IOUT| = 4mA				-4.0	V	1, 2, 3
Voh	Logic "1" Output Voltage, Pin 6	XLS = V+, |IOUT| = 4mA			4.0		V	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5V, V- = -5V

fo	Center Frequency Range		1			30	KHz	4, 5, 6

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5V, V- = -5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
fCLK	Clock Frequency	Pin 6	2			1.5	MHz	4, 5, 6
		Pin 4 and 5	2			4.0	MHz	4, 5, 6
fCLK/f01	Clock to Center Frequency Ratio	W=D=V-, R=V+, fCLK = 167KHz			33.17	33.84		4
					33	34		5, 6
fCLK/f02	Clock to Center Frequency Ratio	W=D=R=Gnd, fCLK = 250KHz			49.75	50.75		4
					49.5	51		5, 6
fCLK/f03	Clock to Center Frequency Ratio	W=V+, D=Gnd, R=V-, fCLK = 500KHz			99.50	101.51		4
					99	102		5, 6
Hon	Passband Gain	DC and 20KHz, W=D=V-, R=V+, fCLK = 167KHz			-0.2	0.2	dB	4, 5, 6
		W=D=R=Gnd, fCLK = 250KHz			-0.2	0.2	dB	4, 5, 6
		W=V+, D=Gnd, R=V-, fCLK = 500KHz			-0.2	0.2	dB	4, 5, 6
Pbw	Ratio of Passband Width to Center Frequency	W=D=V-, R=V+, fCLK = 167KHz			0.11	0.145		4, 5, 6
		W=D=R=Gnd, fCLK = 250KHz			0.24	0.290		4, 5, 6
		W=V+, D=Gnd, R=V-, fCLK = 500KHz			0.50	0.600		4, 5, 6
AMin @ f01	Gain at Center Frequency	W=D=V-, R=V+, fCLK = 167KHz				-30	dB	4, 5, 6
AMin @ f02	Gain at Center Frequency	W=D=R=Gnd, fCLK = 250KHz				-36.5	dB	4, 5, 6
AMin @ f03	Gain at Center Frequency	W=V+, D=Gnd, R=V-, fCLK = 500KHz				-36.5	dB	4, 5, 6
	Additional Center Frequency Gain Test @ f01	W=Gnd, D=V-, R=V+, fCLK = 167KHz				-30	dB	4, 5, 6
		W=V+, D=V-, R=V+, fCLK = 167KHz				-30	dB	4, 5, 6
		W=V-, D=Gnd, R=V+, fCLK = 167KHz				-30	dB	4, 5, 6
		W=D=Gnd, R=V+, fCLK = 167KHz				-35	dB	4, 5, 6
		W=V+, D=Gnd, R=V+, fCLK = 167KHz				-35	dB	4, 5, 6

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5V, V- = -5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
	Additional Center Frequency Gain Test @ f02	W=V-, D=V-, R=Gnd, fCLK = 250KHz				-30	dB	4, 5, 6
		W=Gnd, D=V-, R=Gnd, fCLK = 250KHz				-30	dB	4, 5, 6
		W=V+, D=V-, R=Gnd, fCLK = 250KHz				-30	dB	4, 5, 6
		W=V-, D=R=Gnd, fCLK = 250KHz				-30	dB	4, 5, 6
		W=V+, D=R=Gnd, fCLK = 250KHz				-35	dB	4, 5, 6
	Additional Center Frequency Gain Test @ f03	W=D=R=V-, fCLK = 500KHz				-30	dB	4, 5, 6
		W=Gnd, D=V-, R=V-, fCLK = 500KHz				-30	dB	4, 5, 6
		W=V+, D=V-, R=V-, fCLK = 500KHz				-30	dB	4, 5, 6
		W=V-, D=Gnd, R=V-, fCLK = 500KHz				-30	dB	4, 5, 6
		W=D=Gnd, R=V-, fCLK = 500KHz				-35	dB	4, 5, 6
A3a	Gain at f3=0.995f01	W=D=V-, R=V+, fCLK = 167KHz				-30	dB	4, 5, 6
A4a	Gain at f4=1.005f01					-30	dB	4, 5, 6
A3b	Gain at f3=0.992f02	W=D=R=Gnd, fCLK = 250KHz				-35	dB	4, 5, 6
A4b	Gain at f4=1.008f02					-35	dB	4, 5, 6
A3c	Gain at f3=0.982f03	W=V+, D=Gnd, R=V-, fCLK = 500KHz				-35	dB	4, 5, 6
A4c	Gain at f4=1.018f03					-35	dB	4, 5, 6
Amax1	Passband Ripple	W=D=V-, R=V+, fCLK = 167KHz, f5=0.914f01			0	0.9	dB	4, 5, 6
		W=D=V-, R=V+, fCLK = 167KHz, f6=1.094f01			0	0.9	dB	4, 5, 6
Amax2	Passband Ripple	W=D=Gnd, fCLK = 250KHz, f5=0.830f02			0	0.9	dB	4, 5, 6
		W=D=R=Gnd, fCLK = 250KHz, f6=1.205f02			0	0.9	dB	4, 5, 6

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5V, V- = -5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Amax3	Passband Ripple	W=V+, D=Gnd, R=V-, fCLK = 500KHz, f5=0.700f03			0	0.9	dB	4, 5, 6
		W=V+, D=Gnd, R=V-, fCLK = 500KHz, f6=1.428f03			0	0.9	dB	4, 5, 6

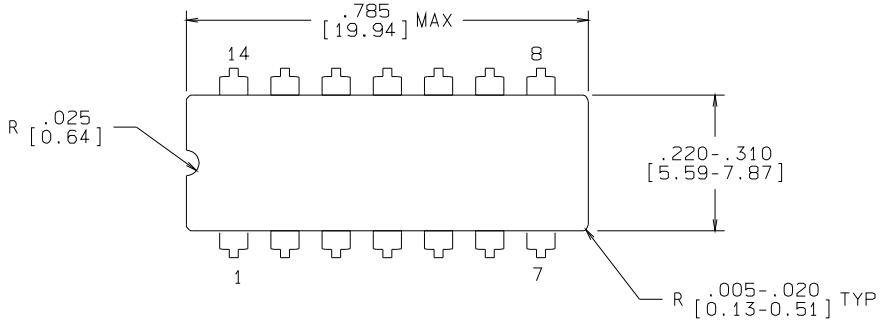
Note 1: Inversely tested
Note 2: Maximum clock frequency at Pin 6 when testing center frequency range.
Note 3: Parameter tested go-no-go only
Note 4: Indirect tests

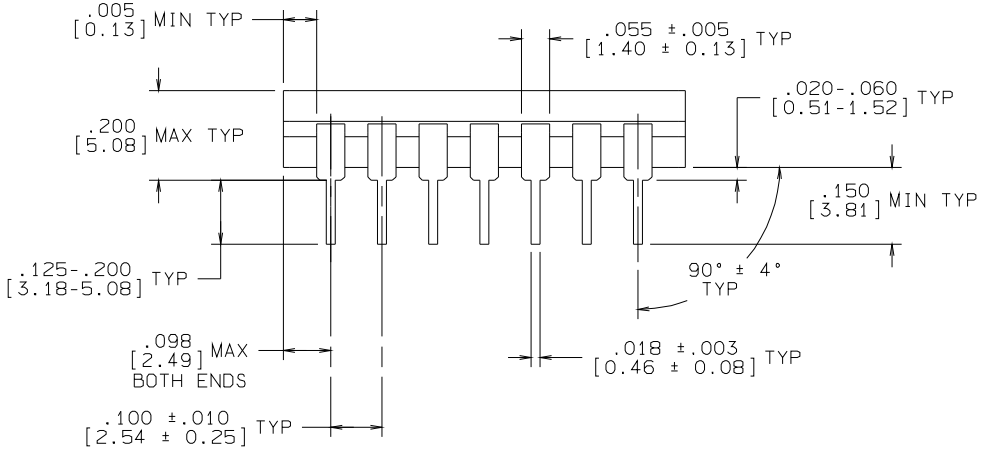
Graphics and Diagrams

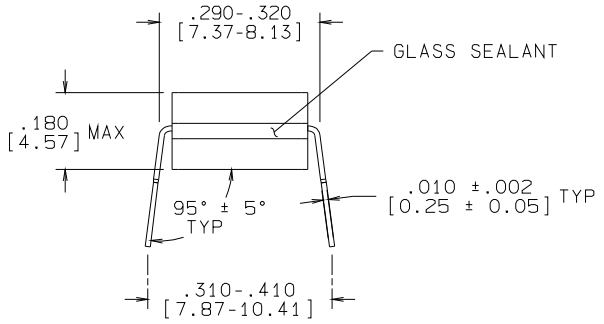
GRAPHICS#	DESCRIPTION
06094HR	(blank)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH [MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1