National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM6162-X REV 2A1

Original Creation Date: 08/03/95
Last Update Date: 06/17/98
Last Major Revision Date: 05/27/98

HIGH SPEED OPERATIONAL AMPLIFIER

General Description

The LM6162 high-speed amplifier exhibits an excellent speed-power product, delivering 300 V/uS and 100 MHz gain-bandwidth product (stable for gains as low as +2 or -1) with only 5mA of supply current. Further, power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

This amplifier is built with National's VIP[TM] (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advance junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Industry Part Number

LM6162

NS Part Numbers

LM6162J-QMLV*
LM6162J/883**
LM6162WG-QMLV***
LM6162WG/883****

Prime Die

LM6162B

Controlling Document

See Features Page

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- High slew rate 300 V/uS
- High gain-bandwidth product 100MHz
- Low supply current 5mA
- Fast settling time 120nS to 0.1%
- Low differential gain <0.1%
- Low differential phase <0.1 degrees
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply
- SMD : 9216501VPA*, MPA**, VXA***, MXA****

Applications

- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (V+ - V-)		36V
Differential Input Voltage Range (Note 3)		±8V
Common-Mode Input Voltage Range (Note 4)		(V+ - 0.7V) to (V- - 0.3V)
Output Short Circuit to Gnd (Note 5)		Continuous
Power Dissipation (Note 2)		400mW
Soldering Information (Soldering, 10 seconds)		260 C
Storage Temperature Range		-65 C ≤ TA ≤ +150 C
Maximum Junction Temperature		150 C
Thermal Resistance		
ThetaJA		
CERDIP	(Still Air)	113 C/W
	(500LF/Min Air flow)	51 C/W
CERAMIC SOIC	(Still Air)	228 C/W
	(500LF/Min Air flow)	140 C/W
ThetaJC		
CERDIP		21 C/W
CERAMIC SOIC		21 C/W
Package Weight (Typical)		
CERDIP		TBD
CERAMIC SOIC		220mg
ESD Tolerance (Note 6)		±500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 4: a) In addition, the voltage between the V+ pin and either input pin must not exceed 36V. b) When the voltage applied to an input pin is driven more than 0.3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20mA to limit damage from self-heating.

Note 5: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 C.

Note 6: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100pF in series with 1500 Ohms.

Recommended Operating Conditions

(Note 1)

Temperature Range	-55 C ≤ TA ≤ +125 C
Supply Voltage Range	4.75V to 32V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0V, Rl ≥ 100K Ohms, Rs = 10K Ohms.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-5	5	mV	1
					-8	8	mV	2, 3
Iib	Input Bias Current				-3	3	uA	1
					-6	6	uA	2, 3
Iio	Input Offset Current				-350	350	nA	1
					-800	800	nA	2, 3
+Vcmr	Positive Common-Mode Voltage Range	Vcc = ±15V			13.9		V	1
		Vcc = ±15V			13.8		V	2, 3
		Vcc = +5V	1		3.9		V	1
			1		3.8		V	2, 3
-Vcmr	Negative Common-Mode Voltage Range	Vcc = ±15V				-12.9	V	1
		Vcc = ±15V				-12.7	V	2, 3
		Vcc = +5V	1			1.8	V	1
			1			2.0	V	2, 3
CMRR	Common-Mode Rejection Ratio	-12.9V ≤ Vcm ≤ 13.9V			83		dB	1
		-12.7V ≤ Vcm = 13.8V			79		dB	2, 3
PSRR	Power Supply Rejection Ratio	±10V ≤ Vcc ≤ ±16V			83		dB	1
		±10V ≤ Vcc ≤ ±16V			79		dB	2, 3
Ios	Output Short Circuit Current	Source				-30	mA	1
						-20	mA	2, 3
		Sink			30		mA	1
					20		mA	2, 3
Icc	Supply Current					6.5	mA	1
						6.8	mA	2, 3
Avs	Large Signal Voltage Gain	Vout = ±10V, Rl = 2K Ohms	2		1000		V/V	4
		Vout = ±10V, Rl = 2K Ohms	2		500		V/V	5, 6
+Vop	Positive Voltage Swing	Vcc = ±15V, Rl = 2K Ohms			13.5		V	1
		Vcc = ±15V, Rl = 2K Ohms			13.3		V	2, 3
		Vcc = +5V, Rl = 2K Ohms	1		3.5		V	1
			1		3.3		V	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0V, Rl ≥ 100K Ohms, Rs = 10K Ohms.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Vop	Negative Voltage Swing	Vcc = ±15V, Rl = 2K Ohms				-13.0	V	1
		Vcc = ±15V, Rl = 2K Ohms				-12.7	V	2, 3
		Vcc = +5V, Rl = 2K Ohms	1			1.7	V	1
			1			2.0	V	2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±15V, Vcm = 0V, Rl ≥ 100K Ohms, Rs = 10K Ohms.

Gbw	Gain Bandwidth Product	f = 20Mhz			80		MHz	4
					55		MHz	5, 6
+Sr	Slew Rate	Output step = -4V to +4V, Av = 2, Vin = 8V step			200		V/uS	4, 5, 6
-Sr	Slew Rate	Output step = +4V to -4V, Av = 2, Vin = 8V step			200		V/uS	4, 5, 6
ts	Settling Time	10V step to 0.1% , Av = -1, Rl = 2K Ohms				300	nS	9
						325	nS	10, 11

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0V, Rl ≥ 100K Ohms, Rs = 10K Ohms. "Delta calculations performed on QMLV devices at Group B, Subgroup 5 ONLY"

Vio	Input Offset Voltage				-0.75	+0.75	mV	1
Iib	Input Bias Current				-0.5	+0.5	uA	1
Iio	Input Offset Current				-35	+35	nA	1
CMRR	Common-Mode Rejection Ratio	-12.9V ≤ Vcm ≤ 13.9V			-5	+5	dB	1

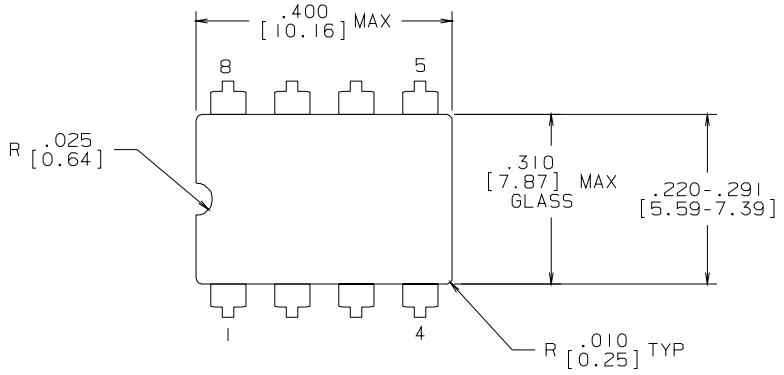
Note 1: For single supply operation, the following conditions apply: V+ = 5V, V- = 0V, Vcm = 2.5V, Vout = 2.5V. Pin 1 and Pin 8 (Vos adjust pins) are each connected to Pin 4 (V-) to realize maximum output swing. This connection will increase the offset voltage.
Note 2: Voltage gain is the total output swing (20V) divided by the signal required to produce that swing.

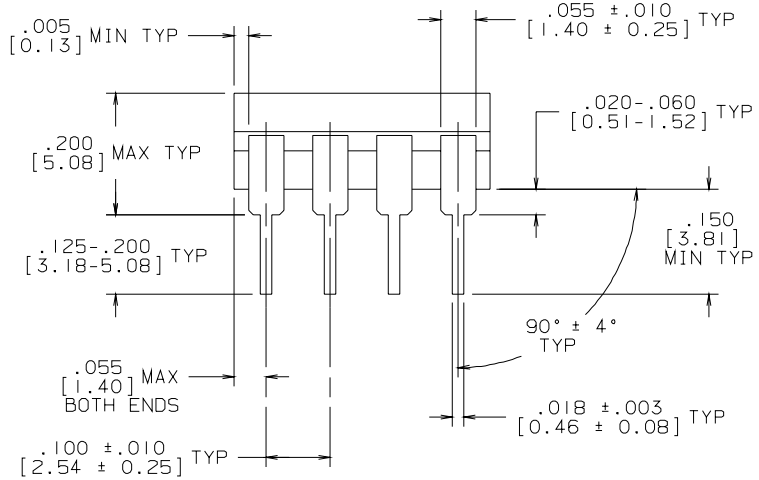
Graphics and Diagrams

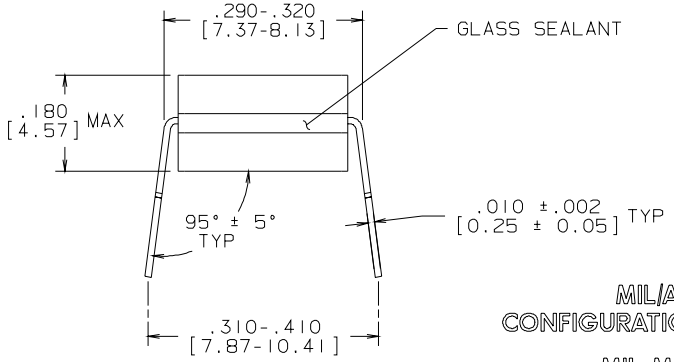
GRAPHICS#	DESCRIPTION
05885HRA4	CERDIP (J), 8 LEAD (B/I CKT)
06190HRA3	CERPACK (W, WG), 10LD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000242A	CERDIP (J), 8 LEAD (PINOUT)
P000361A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	I0002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

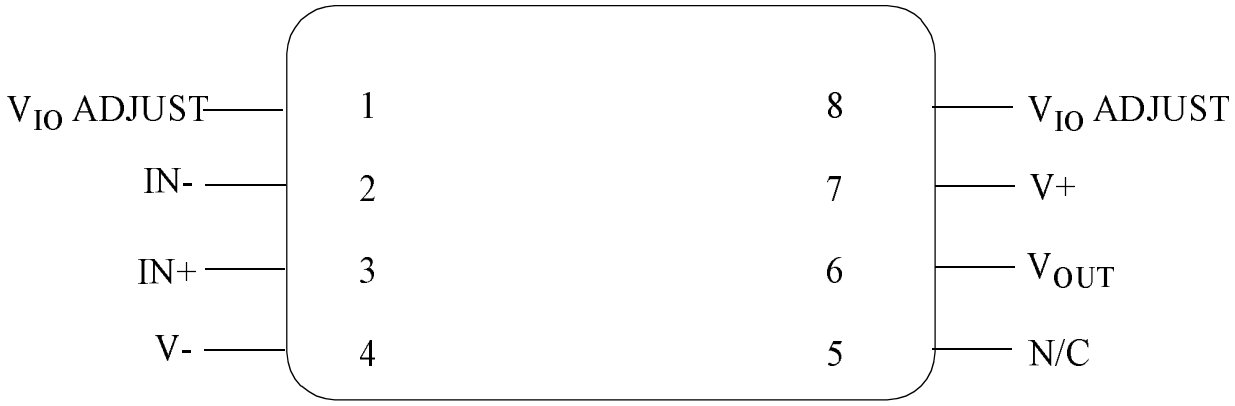
PROJECTION
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM6162J

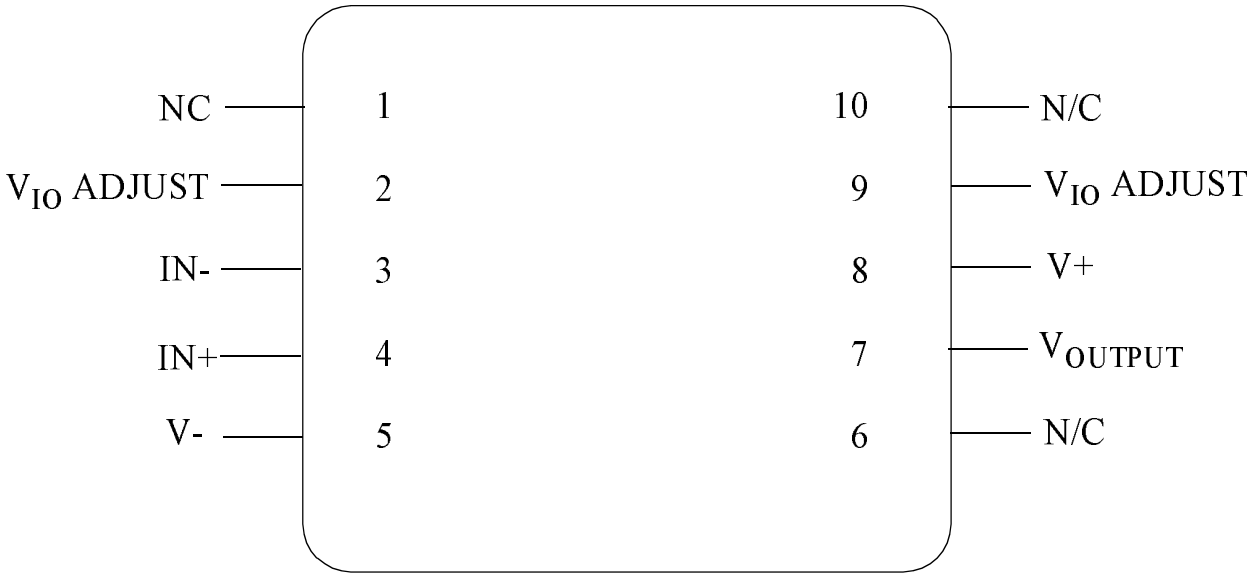
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000242A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM6162WG

10 - LEAD CERAMIC SOIC

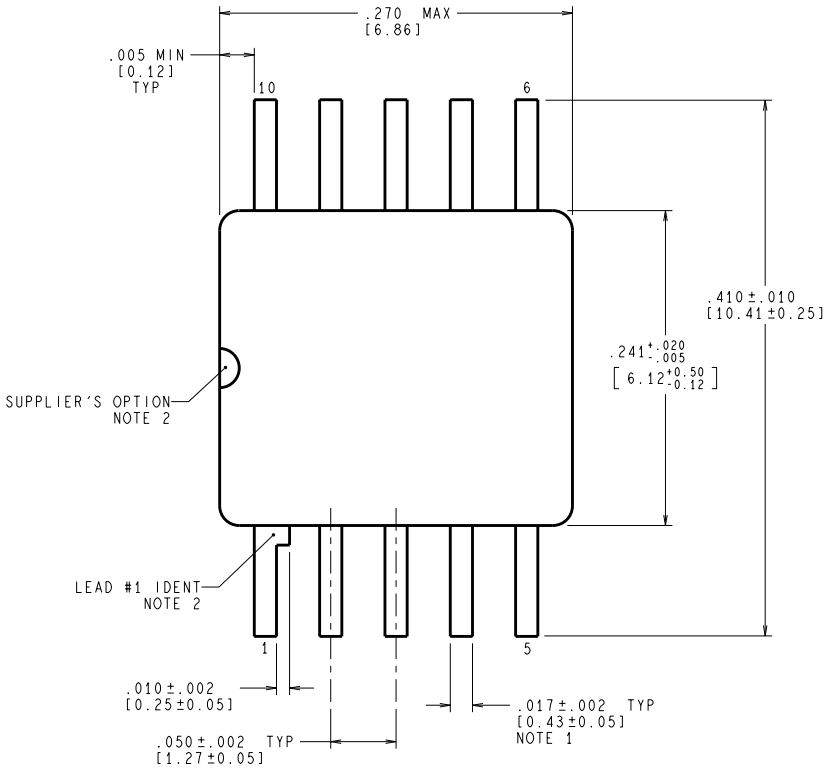
CONNECTION DIAGRAM

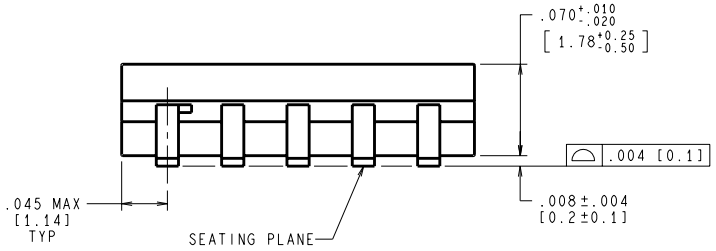
TOP VIEW

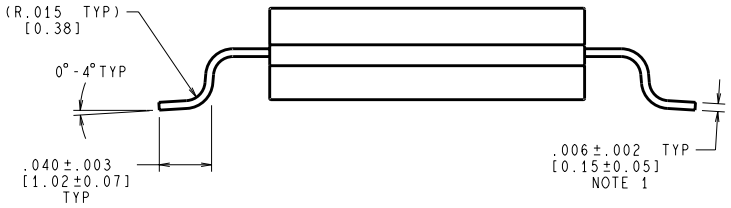
P000361A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0002855	06/17/98	Barbara Lopez	Update MDS: MNLM6162-X Rev. 0A0 to MNLM6162-X Rev. 1A1. Added WG package and SMD number for WG package. Updated thermal data to add WG package. Added package weights. Updated Subgroups to match SMD. Added power dissipation limits. Added B/I, MKT and Pinout graphics for all packages.
2A1	M0002905	06/17/98	Rose Malone	Updated MDS: MNLM6162-X, Rev. 1A1 to MNLM6162-X, Rev. 2A1. Package Weight for Ceramic SOIC, Drift Section and QMLV reference. Corrected CMRR typo. Arranged SMD references in Features section to match Main Table. Removed LCC and CERPACK references for low sales volume.